



U74HC2G32

CMOS IC

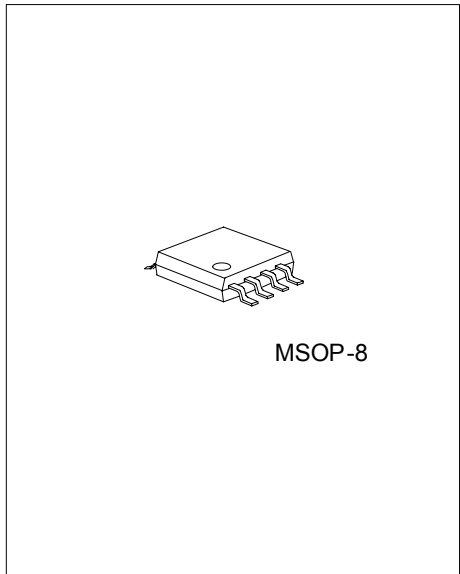
2-INPUT OR GATE

DESCRIPTION

The U74HC2G32 is a 2-input OR gate which provides the Function $Y=A+B$.

FEATURES

- * Operation Voltage Range: 2.0~6.0V
- * Low Power Dissipation: $I_{CC}=10\mu A(\text{Max})$
- * High Speed: $t_{pd}=9\text{ns}(V_{CC}=4.5\text{V}, C_L=50\text{pF})$
- * Specified from -40 to +85 and -40 to +125



*Pb-free plating product number:
U74HC2G32L

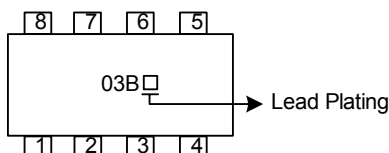
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ORDERING INFORMATION

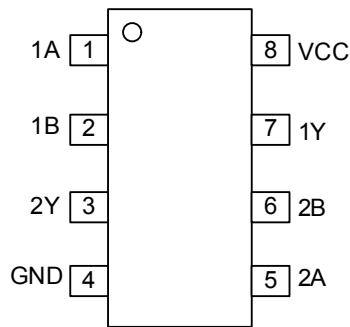
Order Number		Package	Packing
Normal	Lead Free Plating		
U74HC2G32-SM1-R	U74HC2G32L-SM1-R	MSOP-8	Tape Reel
U74HC2G32-SM1-T	U74HC2G32L-SM1-T	MSOP-8	Tube

<p>U74HC2G32L-SM1-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) SM1: MSOP-8 (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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MARKING



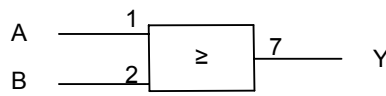
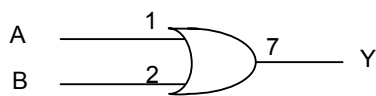
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Input Voltage	V_{IN}	-0.5~7	V
Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_{OUT}	25	mA
V_{CC} or GND Current	I_{CC}	50	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{STG}	-65 ~ +150	

Note 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0	5.0	6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Times	t_R, t_F	$V_{CC}=2.0V$			1000	ns
		$V_{CC}=4.5V$		6	500	
		$V_{CC}=6V$			400	
Operating Temperature	T_A		-40	25	125	

■ STATIC CHARACTERISTICS

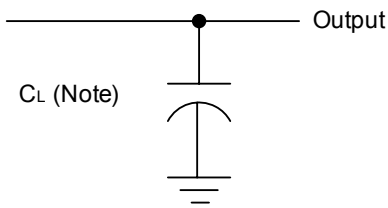
PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25$			-40~85		-40~125		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	V_{IH}	$V_{CC}=2.0V$	1.5	1.2		1.5		1.5		V
		$V_{CC}=4.5V$	3.15	2.4		3.15		3.15		
		$V_{CC}=6.0V$	4.2	3.2		4.2		4.2		
Low-Level Input Voltage	V_{IL}	$V_{CC}=2.0V$		0.8	0.5		0.5		0.5	V
		$V_{CC}=4.5V$		2.1	1.35		1.35		1.35	
		$V_{CC}=6.0V$		2.8	1.8		1.8		1.8	
High-Level Output Voltage	V_{OH}	$V_{CC}=2.0V, I_{OH}=-20\mu A$	1.9	2.0		1.9		1.9		V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.5		4.4		4.4		
		$V_{CC}=6.0V, I_{OH}=-20\mu A$	5.9	6.0		5.9		5.9		
		$V_{CC}=4.5V, I_{OH}=-4mA$	4.18	4.32		4.13		3.7		
		$V_{CC}=6.0V, I_{OH}=-5.2mA$	5.68	5.81		5.63		5.2		
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.0V, I_{OL}=20\mu A$		0	0.1		0.1		0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$		0	0.1		0.1		0.1	
		$V_{CC}=6.0V, I_{OL}=20\mu A$		0	0.1		0.1		0.1	
		$V_{CC}=4.5V, I_{OH}=4mA$		0.15	0.26		0.33		0.4	
		$V_{CC}=6.0V, I_{OH}=5.2mA$		0.16	0.26		0.33		0.4	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND			±0.1		±1		±1	µA
Quiescent Supply Current	I_Q	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			1		10		20	µA
Input Capacitance	C_{IN}	$V_{CC}=5.0V, V_{IN}=V_{CC}$ or GND		1.5						pF

■ DYNAMIC CHARACTERISTICS (Input: $t_R, t_F \leq 6\text{ns}$; $\text{PRR} \leq 1\text{MHz}$)

See Fig-1 and Fig-2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25$			-40~85		-40~125		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay From Input (A and B) to Output(Y)	t_{PHL} / t_{PLH}	$V_{CC}= 2.0, C_L= 50\text{pF}$		24	75		95		110	ns
		$V_{CC}= 4.5, C_L= 50\text{pF}$		9	15		19		22	
		$V_{CC}= 6.0, C_L= 50\text{pF}$		7	13		16		20	
Output Transition Time	t_{THL} / t_{TLH}	$V_{CC}= 2.0, C_L= 50\text{pF}$		18	75		95		125	ns
		$V_{CC}= 4.5, C_L= 50\text{pF}$		6	15		19		25	
		$V_{CC}= 6.0, C_L= 50\text{pF}$		5	13		16		20	
Operating Characteristics										
PARAMETER	SYMBOL	TEST CONDITIONS						TYP	UNIT	
Power Dissipation Capacitance	Cpd	No load, $f=1\text{MHz}, V_{CC}=5$						10	pF	

■ TEST CIRCUIT AND WAVEFORMS



Note: CL includes probe and jig capacitance.

Fig.1 Load circuitry for switching times.

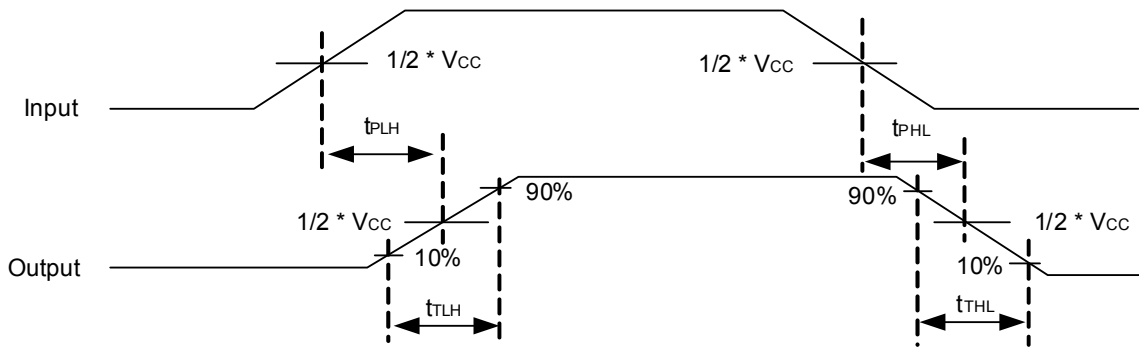


Fig. 2 Propagation delay from input(A and B) to output(Y) and Output transition time.

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