



U74HC590

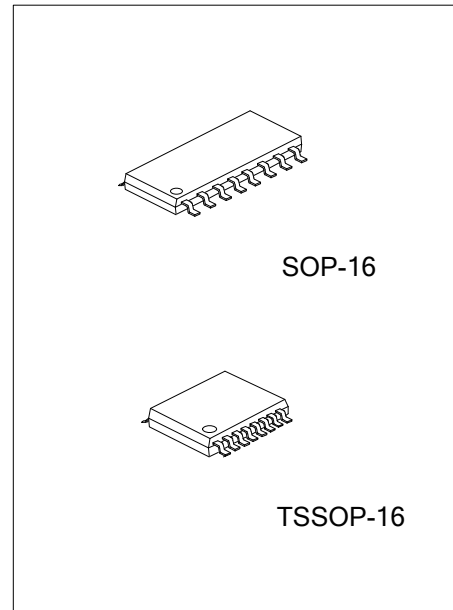
CMOS IC

8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

DESCRIPTION

The UTC **74HC590** contains an 8-bit binary counter that feeds an 8-bit storage register and 3-state outputs.. The storage register has parallel ($Q_A \sim Q_H$) outputs.

The binary counter features direct clear (\overline{CCLR}) and count-enable (\overline{CCKEN}) inputs. A ripple-carry output (\overline{RCO}) is provided for cascading. Expansion is accomplished easily for two stages by connecting (\overline{RCO}) of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting (\overline{RCO}) of each stage to the counter clock (CCLK) input of the following stage.



FEATURES

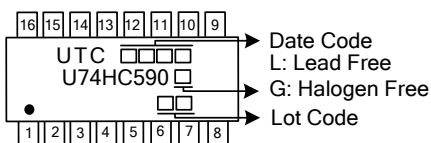
- * Wide supply voltage range from 2.0V to 6.0V
- * Low static power consumption; $I_{CC} = 8\mu A$ (Max.)
- * 8 bit counter with register

ORDERING INFORMATION

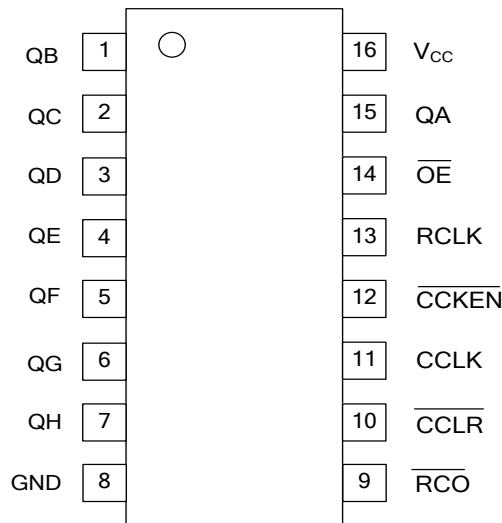
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC590L-S16-R	U74HC590G-S16-R	SOP-16	Tape Reel
U74HC590L-P16-R	U74HC590G-P16-R	TSSOP-16	Tape Reel

<p>U74HC590G-S16-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S16: SOP-16, P16: TSSOP-16</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
---	--

MARKING



■ PIN CONFIGURATION



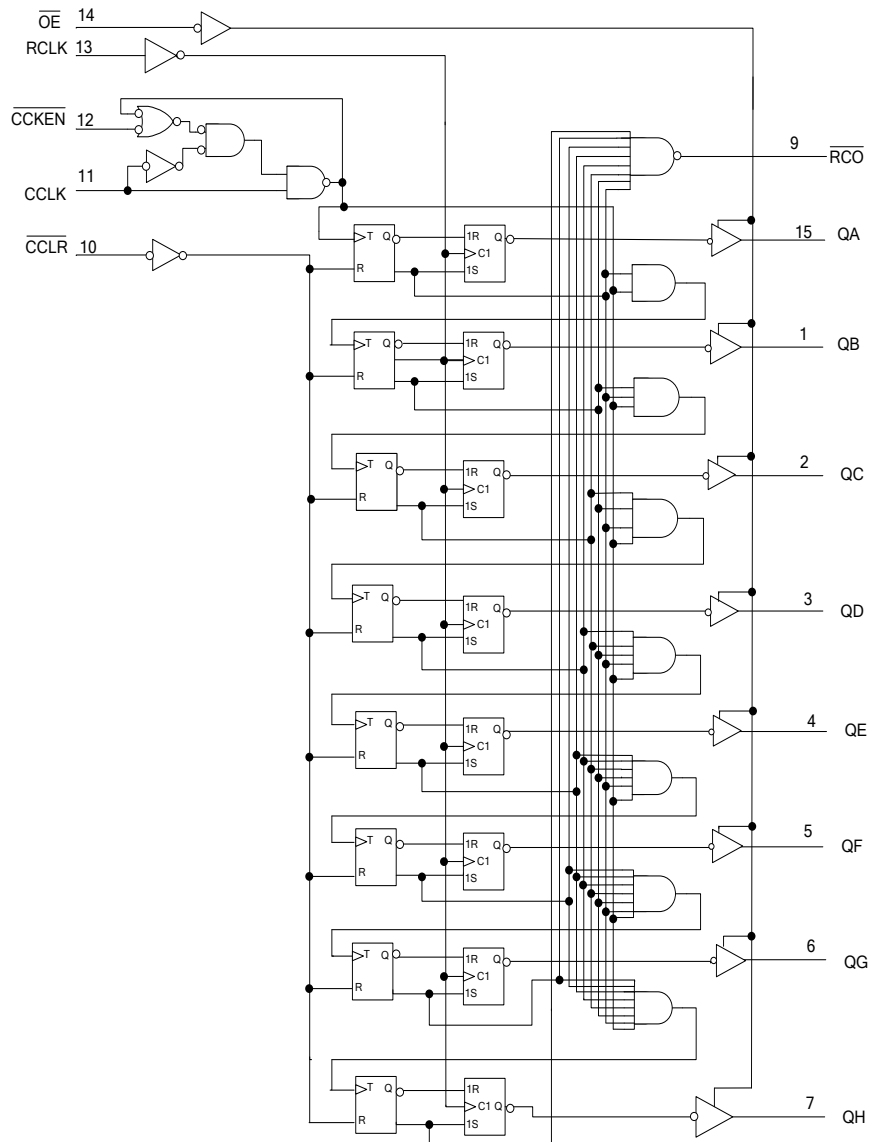
■ FUNCTION TABLE

INPUTS					FUNCTION
\overline{OE}	RCLK	\overline{CCLR}	\overline{CCKEN}	CCLK	
H	X	X	X	X	Outputs Q_A - Q_H are disabled.
L	X	X	X	X	Outputs Q_A - Q_H are enabled.
X	↑	X	X	X	Counter data stored into register
X	↓	X	X	X	Register stage is not changed.
X	X	L	X	X	Counter clear.
X	X	H	L	↑	Advance one count.
X	X	H	L	↓	No count
X	X	H	H	X	No count

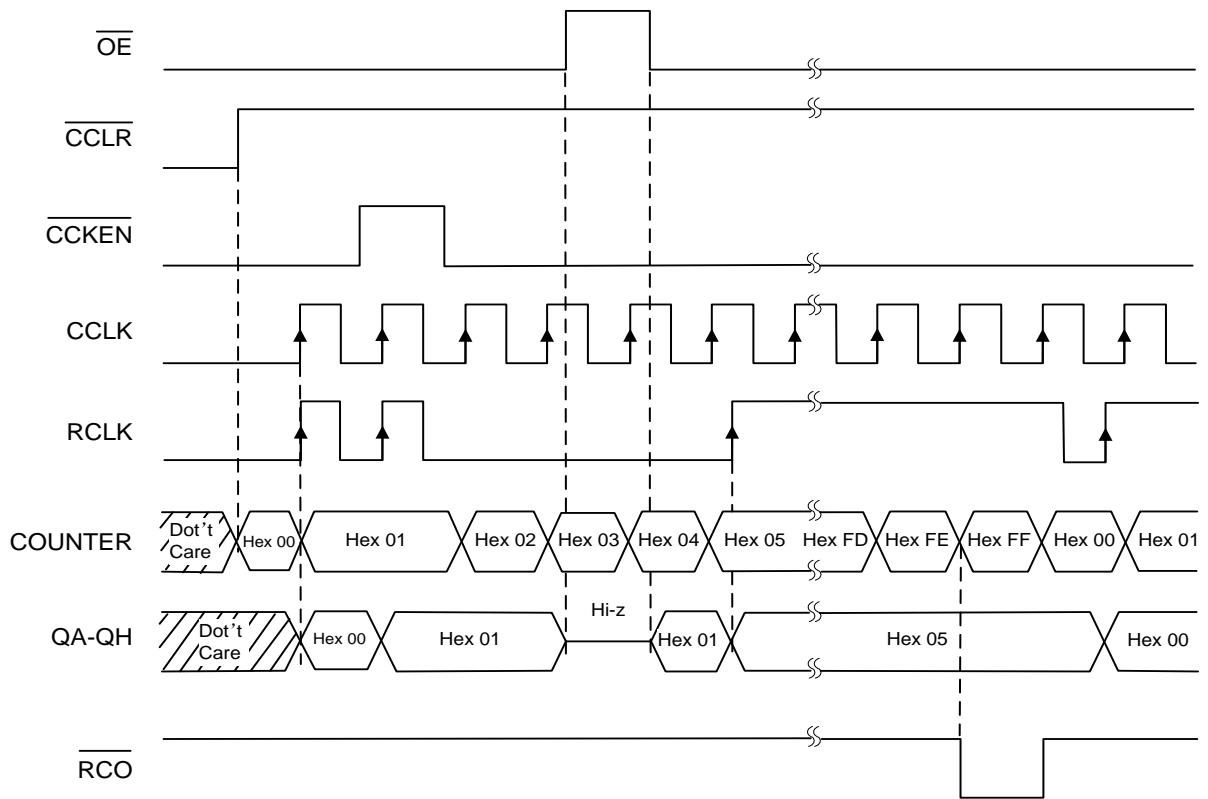
Notes: 1. H: High voltage level; L: Low voltage level; ↑: Low-to-High; X: Don't care

2. $\overline{RCO} = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{Q_4} \cdot \overline{Q_5} \cdot \overline{Q_6} \cdot \overline{Q_7}$ (Q_0' to Q_7' are internal outputs of the counter)

■ LOGIC DIAGRAM (positive logic)



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Continuous V_{CC} or GND Current	I_{CC}		±75	μA
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	±35	mA
Input Clamp Current	I_{IK}	$V_{IN}<0V$ or $V_{IN}>V_{CC}$	±20	mA
Output Clamp Current	I_{OK}	$V_{OUT}>V_{CC}$ or $V_{OUT}<0V$	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0	5.0	6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		85	°C
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=2.0V$			1000	ns
		$V_{CC}=4.5V$			500	ns
		$V_{CC}=6.0V$			400	ns

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High-level Input Voltage	V_{IH}	$V_{CC}=2.0V$	1.5			V	
		$V_{CC}=4.5V$	3.15			V	
		$V_{CC}=6.0V$	4.2			V	
Low-level Input Voltage	V_{IL}	$V_{CC}=2.0V$			0.5	V	
		$V_{CC}=4.5V$			1.35	V	
		$V_{CC}=6.0V$			1.8	V	
High-Level Output Voltage	V_{OH}	$V_{CC}=2.0V$	$I_{OH}=-20\mu A$, $V_{IN}=V_{CC}$ or GND	1.9	1.998		V
		$V_{CC}=4.5V$		4.4	4.499		V
		$V_{CC}=6.0V$		5.9	5.999		V
		$V_{CC}=4.5V$	RCO , $I_{OH}=-4mA$ $V_{IN}=V_{CC}$ or GND	3.98	4.3		V
			$QA-Q_H$, $I_{OH}=-6mA$ $V_{IN}=V_{CC}$ or GND	3.98	4.3		V
		$V_{CC}=6.0V$	RCO , $I_{OH}=-5.2mA$ $V_{IN}=V_{CC}$ or GND	5.48	5.8		V
$QA-Q_H$, $I_{OH}=-7.8mA$ $V_{IN}=V_{CC}$ or GND	5.48		5.8		V		
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.0V$	$I_{OL}=20\mu A$, $V_{IN}=V_{CC}$ or GND		0.002	0.1	V
		$V_{CC}=4.5V$			0.001	0.1	V
		$V_{CC}=6.0V$			0.001	0.1	V
		$V_{CC}=4.5V$	RCO , $I_{OL}=4mA$ $V_{IN}=V_{CC}$ or GND		0.17	0.26	V
			$QA-Q_H$, $I_{OL}=6mA$ $V_{IN}=V_{CC}$ or GND		0.17	0.26	V
		$V_{CC}=6.0V$	RCO , $I_{OL}=5.2mA$ $V_{IN}=V_{CC}$ or GND		0.15	0.26	V
$QA-Q_H$, $I_{OL}=7.8mA$ $V_{IN}=V_{CC}$ or GND			0.15	0.26	V		

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND			±0.1	μA
3-state Output OFF-state Current	I_{OZ}	$V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=V_{CC}$ or GND, $V_{CC}=6.0V$			±0.5	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or 0V, $I_{OUT}=0A$			8	μA
Input Capacitance	C_I	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND		3.5	10	pF

■ SWITCHING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Maximum clock pulse frequency	f_{MAX}	$C_L=50pF$	$V_{CC}=2.0V$	4	8		MHz
			$V_{CC}=4.5V$	20	35		MHz
			$V_{CC}=6.0V$	24	40		MHz
Propagation delay from input ($\overline{CCLK}\uparrow$) to output(\overline{RCO})	t_{PD}	$C_L=50pF$	$V_{CC}=2.0V$		80	150	ns
			$V_{CC}=4.5V$		20	30	ns
			$V_{CC}=6.0V$		15	26	ns
Propagation delay from input ($\overline{RCLK}\uparrow$) to output(Qn)	t_{PD}	$C_L=50pF$	$V_{CC}=2.0V$		70	140	ns
			$V_{CC}=4.5V$		18	28	ns
			$V_{CC}=6.0V$		14	24	ns
		$C_L=150pF$	$V_{CC}=2.0V$		100	300	ns
			$V_{CC}=4.5V$		24	60	ns
			$V_{CC}=6.0V$		20	51	ns
Propagation delay from input ($\overline{CCLR}\downarrow$) to output(\overline{RCO})	t_{PLH}	$C_L=50pF$	$V_{CC}=2.0V$		70	130	ns
			$V_{CC}=4.5V$		18	26	ns
			$V_{CC}=6.0V$		14	22	ns
Propagation delay from input ($\overline{OE}\downarrow$) to output(Qn)	t_{en}	$C_L=50pF$	$V_{CC}=2.0V$		80	125	ns
			$V_{CC}=4.5V$		20	25	ns
			$V_{CC}=6.0V$		15	21	ns
		$C_L=150pF$	$V_{CC}=2.0V$		90	200	ns
			$V_{CC}=4.5V$		23	40	ns
			$V_{CC}=6.0V$		19	34	ns
Propagation delay from input ($\overline{OE}\uparrow$) to output(Qn)	t_{dis}	$C_L=50pF$	$V_{CC}=2.0V$		80	125	ns
			$V_{CC}=4.5V$		20	25	ns
			$V_{CC}=6.0V$		15	21	ns

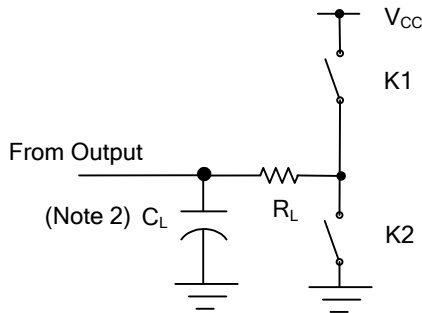
■ TIMING REQUIREMENTS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f _{CLOCK}	V _{CC} =2.0V			4	MHz
		V _{CC} =4.5V			20	MHz
		V _{CC} =6.0V			24	MHz
Pulse duration, CCLK or RCLK high or low	t _w	V _{CC} =2.0V	125			ns
		V _{CC} =4.5V	25			ns
		V _{CC} =6.0V	21			ns
Pulse duration, $\overline{\text{CCLR}}$ Low	t _w	V _{CC} =2.0V	100			ns
		V _{CC} =4.5V	20			ns
		V _{CC} =6.0V	17			ns
Setup Time, $\overline{\text{CCKEN}}$ Low Before CCLK↑	t _{SU}	V _{CC} =2.0V	100			ns
		V _{CC} =4.5V	20			ns
		V _{CC} =6.0V	17			ns
Setup Time, $\overline{\text{CCLR}}$ High (Inactive) Before CCLK↑	t _{SU}	V _{CC} =2.0V	100			ns
		V _{CC} =4.5V	20			ns
		V _{CC} =6.0V	17			ns
Setup Time, CCLK↑ Before RCLK↑	t _{SU}	V _{CC} =2.0V	100			ns
		V _{CC} =4.5V	20			ns
		V _{CC} =6.0V	17			ns
Hold Time, $\overline{\text{CCKEN}}$ Low After CCLK↑	t _H	V _{CC} =2.0V	50			ns
		V _{CC} =4.5V	10			ns
		V _{CC} =6.0V	9			ns

■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

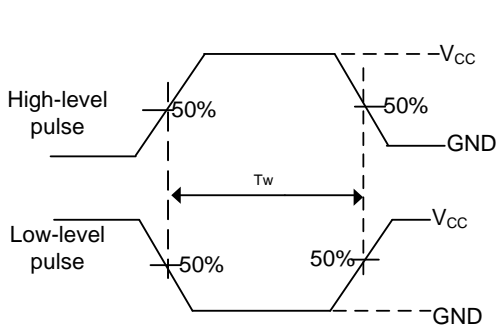
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C _{PD}	No load.		250		pF

TEST CIRCUIT AND WAVEFORMS

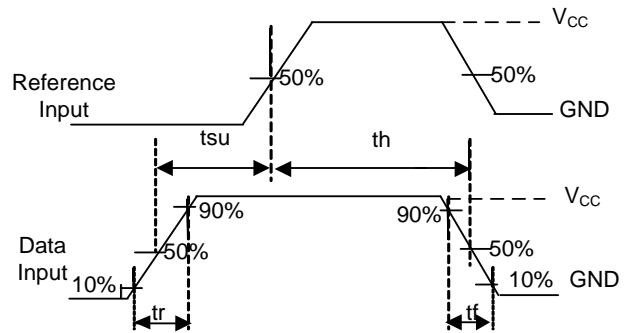


TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PLZ}/t_{PZL}	Close	Open
t_{PHZ}/t_{PZH}	Open	Close

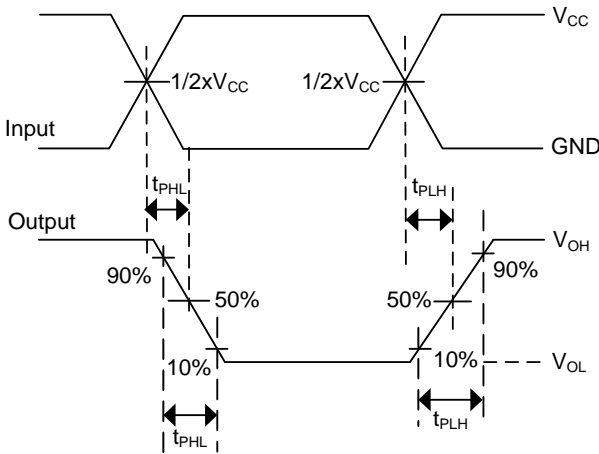
Note: C_L includes probe and jig capacitance. $C_L=50\text{pF}$, $R_L=1\text{K}\Omega$.



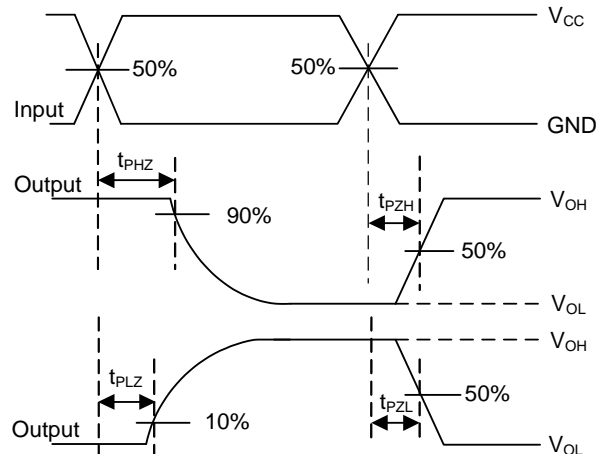
PULSE WIDTH



SETUP TIME AND HOLD TIME



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10\text{MHz}$, $Z_0 = 50\Omega$.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.