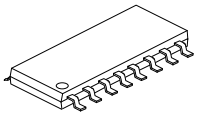
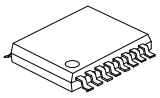
U74HC594

CMOS IC

8-BIT SERIAL-IN SHIFT REGISTER WITH OUTPUT REGISTERS



SOP-16



TSSOP-16

■ DESCRIPTION

The UTC **U74HC594** contains an 8-bit serial-in parallel-out register. The Serial Data Input (SER) input will shift into the internal shift register during every LOW-to-HIGH transition on the ($\overline{\text{SRCLR}}$) input. The storage register will storage the 8-bit data from the shift register during the LOW-to-HIGH transition on the ($\overline{\text{RCLR}}$) input. A serial (QH') output is provided for cascading purposes.

■ FEATURES

* Wide supply voltage range from 2.0V to 6.0V
* Low static power consumption; I_{CC}=8μA (Max.)
* 8 bit counter with register

■ ORDERING INFORMATION

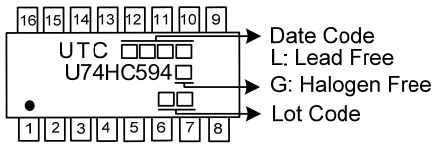
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC594L-S16-R	U74HC594G-S16-R	SOP-16	Tape Reel
U74HC594L-P16-R	U74HC594G-P16-R	TSSOP-16	Tape Reel

U74HC594G-S16-R

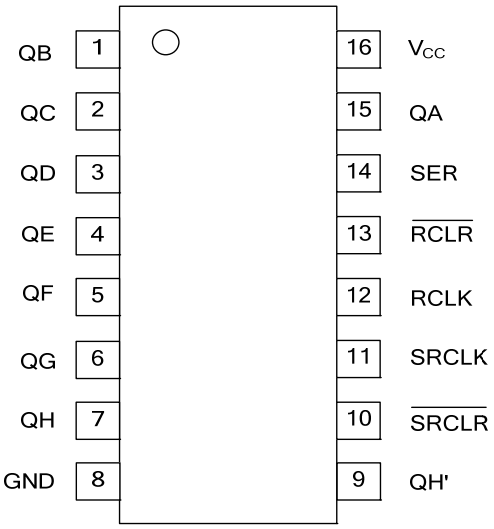
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S16: SOP-16, P16: TSSOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

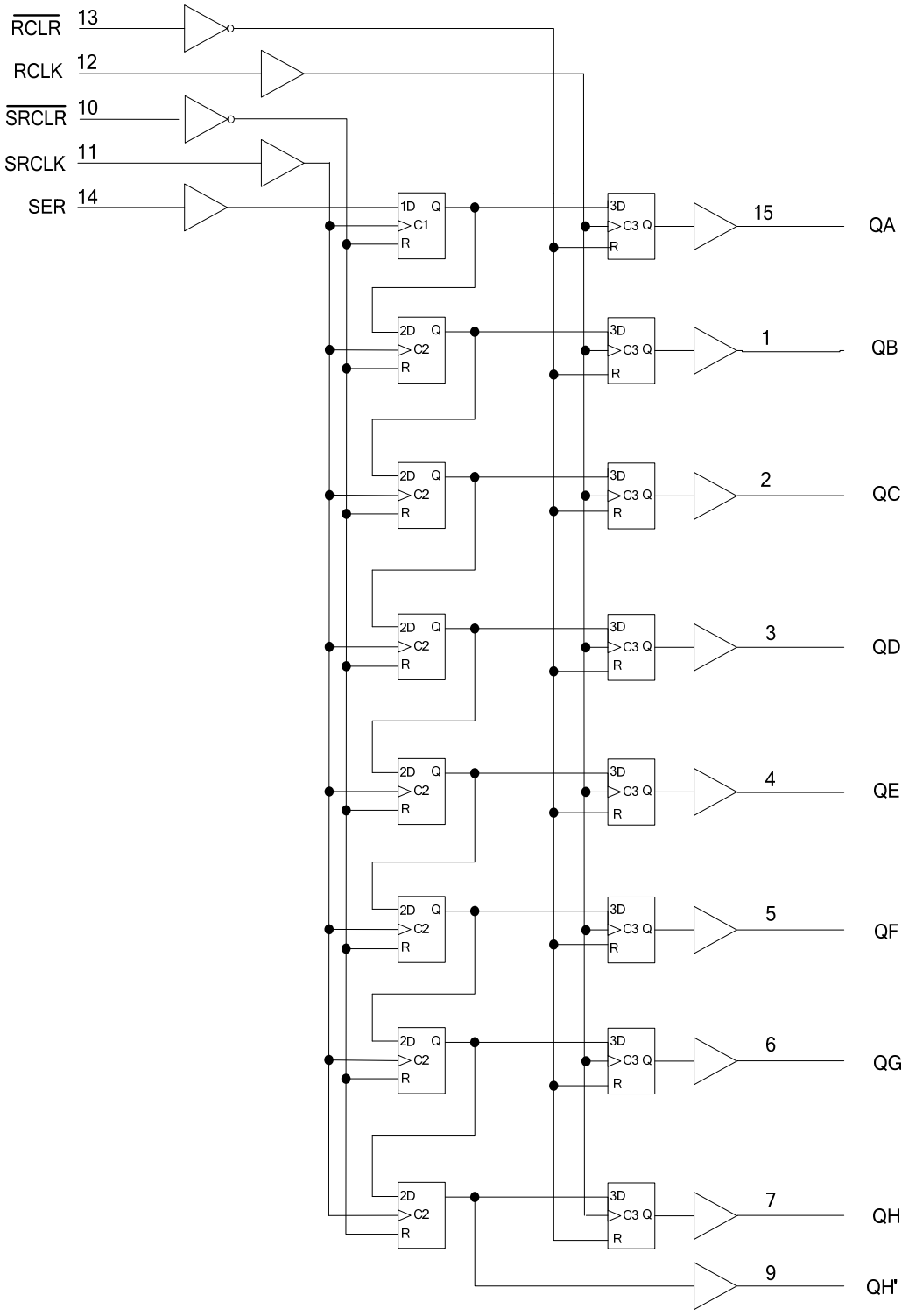


■ FUNCTION TABLE

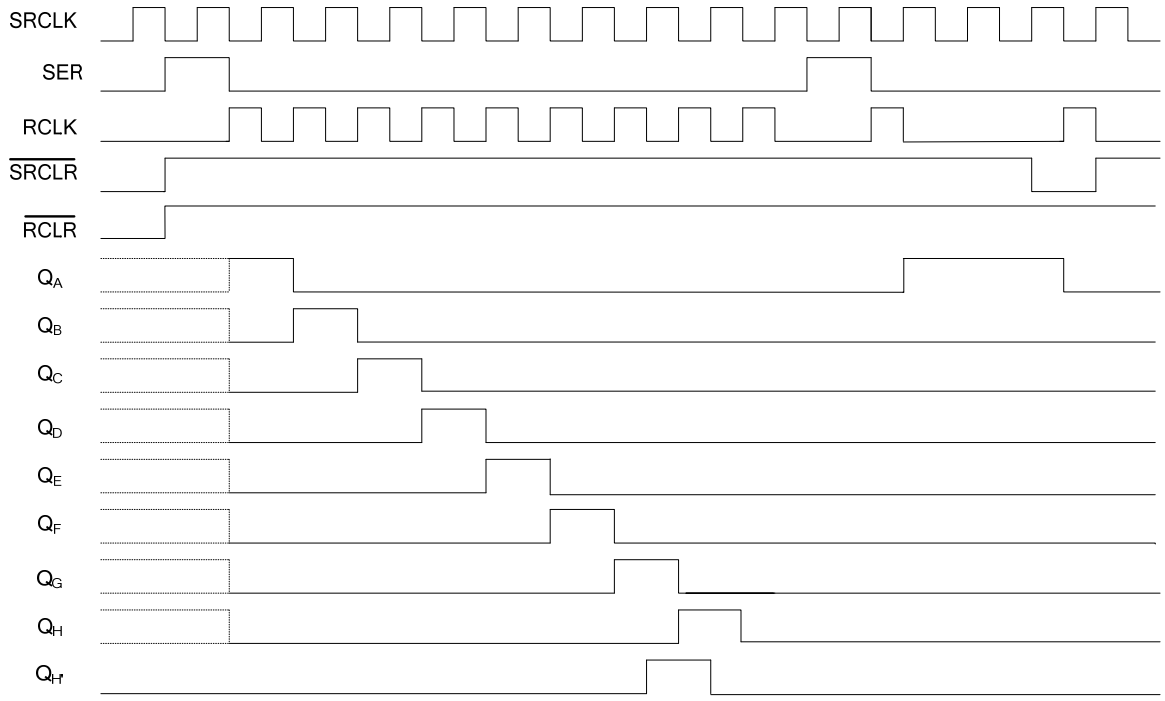
INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift-register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

Note: L: low voltage level; H: high voltage level; ↑: low-to-high; X: don't care

■ LOGIC DIAGRAM (positive logic)



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Continuous V_{CC} or GND Current	I_{CC}		±75	μA
Continuous Output Current	I_{OUT}	V_{OUT}=0V ~ V_{CC}	±35	mA
Input Clamp Current	I_{IK}	V_{IN}<0V or V_{IN}>V_{CC}	±20	mA
Output Clamp Current	I_{OK}	V_{OUT}>V_{CC} or V_{OUT}<0V	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0		6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=2.0V			1000	ns
		V_{CC}=4.5V			500	ns
		V_{CC}=6.0V			400	ns
Operating Temperature	T_A		-40		+85	°C

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=2.0V	1.5			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6.0V	4.2			V
Low-level Input Voltage	V_{IL}	V_{CC}=2.0V			0.5	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6.0V			1.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=2.0V, I_{OH}=-20μA	1.9	1.998		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		V
		V_{CC}=6.0V, I_{OH}=-20μA	5.9	5.999		V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98			V
		V_{CC}=6V, I_{OH}=-7.8mA	5.48			V
Low-Level Output Voltage	V_{OL}	V_{CC}=2.0V, I_{OL}=20μA		0.002	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=6.0V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=4.5V, I_{OL}=6mA			0.26	V
		V_{CC}=6.0V, I_{OL}=7.8mA			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6.0V, V_{IN}= V_{CC} or GND			±0.1	μA
3-state Output OFF-state Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL}, V_{OUT}=V_{CC} or GND, V_{CC} =6.0V			±0.5	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6.0V, V_{IN}=V_{CC} or 0V, I_{OUT}=0A			8	μA
Input Capacitance	C_I	V_{CC}=6.0V, V_{IN}=V_{CC} or GND		3	10	pF

■ SWITCHING CHARACTERISTICS (C_L=50pF, T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{MAX}	C_L=50pF	V_{CC}=2.0V	5	8		MHz
			V_{CC}=4.5V	25	35		MHz
			V_{CC}=6.0V	29	40		MHz
Propagation delay from input (SRCLK) to output (QH')	t_{PD}	C_L=50pF	V_{CC}=2.0V		50	150	ns
			V_{CC}=4.5V		20	30	ns
			V_{CC}=6.0V		15	25	ns
Propagation delay from input (RCLK) to output (Q_A-Q_H)			V_{CC}=2.0V		50	150	ns
			V_{CC}=4.5V		20	30	ns
			V_{CC}=6.0V		15	25	ns
		C_L=150pF	V_{CC}=2.0V		90	200	ns
			V_{CC}=4.5V		23	40	ns
			V_{CC}=6.0V		19	34	ns
Propagation delay from input ($\overline{\text{SRCLK}}$) to output (QH')	t_{PHL}	C_L=50pF	V_{CC}=2.0V		50	150	ns
			V_{CC}=4.5V		20	30	ns
			V_{CC}=6.0V		15	25	ns
Propagation delay from input ($\overline{\text{RCLR}}$) to output (Q_A-Q_H)			V_{CC}=2.0V		50	125	ns
			V_{CC}=4.5V		20	25	ns
			V_{CC}=6.0V		15	21	ns
		C_L=150pF	V_{CC}=2.0V		90	200	ns
			V_{CC}=4.5V		23	40	ns
			V_{CC}=6.0V		19	34	ns
Propagation delay to output (QH')	t_t	C_L=50pF	V_{CC}=2.0V		38	75	ns
			V_{CC}=4.5V		8	15	ns
			V_{CC}=6.0V		6	13	ns
Propagation delay to output (Q_A-Q_H)			V_{CC}=2.0V		38	60	ns
			V_{CC}=4.5V		8	12	ns
			V_{CC}=6.0V		6	10	ns
		C_L=150pF	V_{CC}=2.0V		45	210	ns
			V_{CC}=4.5V		17	42	ns
			V_{CC}=6.0V		13	36	ns

■ TIMING REQUIREMENTS (T_A=25°C, unless otherwise specified)

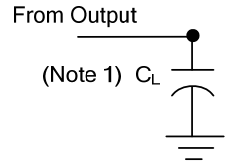
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f_{CLOCK}	V_{CC}=2.0V			5	MHz
		V_{CC}=4.5V			25	MHz
		V_{CC}=6.0V			29	MHz
Pulse duration, SRCLK or RCLK high or low	t_W	V_{CC}=2.0V	100			ns
		V_{CC}=4.5V	20			ns
		V_{CC}=6.0V	17			ns
Pulse duration, $\overline{SRCLK}$ or $\overline{RCLR}$ Low		V_{CC}=2.0V	100			ns
		V_{CC}=4.5V	20			ns
		V_{CC}=6.0V	17			ns
Setup Time Before CLK↑, SER before SRCLK↑	t_{SU}	V_{CC}=2.0V	90			ns
		V_{CC}=4.5V	18			ns
		V_{CC}=6.0V	15			ns
Setup Time Before CLK↑ SRCLK↑ before RCLK↑ (Note)		V_{CC}=2.0V	90			ns
		V_{CC}=4.5V	18			ns
		V_{CC}=6.0V	15			ns
Setup Time Before CLK↑ $\overline{SRCLK}$ low before RCLK↑		V_{CC}=2.0V	50			ns
		V_{CC}=4.5V	10			ns
		V_{CC}=6.0V	9			ns
Setup Time Before CLK↑ $\overline{SRCLK}$ high (inactive) before SRCLK↑		V_{CC}=2.0V	20			ns
		V_{CC}=4.5V	10			ns
		V_{CC}=6.0V	10			ns
Setup Time Before CLK↑ $\overline{RCLR}$ high (inactive) before SRCLK↑		V_{CC}=2.0V	5			ns
		V_{CC}=4.5V	5			ns
		V_{CC}=6.0V	5			ns
Setup Time Before CLK↑ Hold time, SER after SRCLK↑	t_H	V_{CC}=2.0V	5			ns
		V_{CC}=4.5V	5			ns
		V_{CC}=6.0V	5			ns

Note: This setup time ensures that the output register receives stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

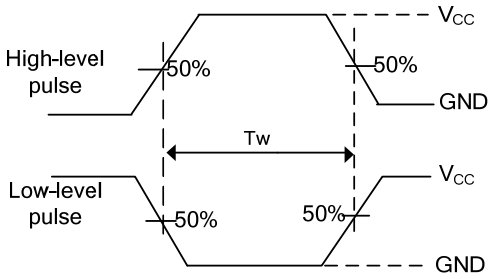
■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load.		395		pF

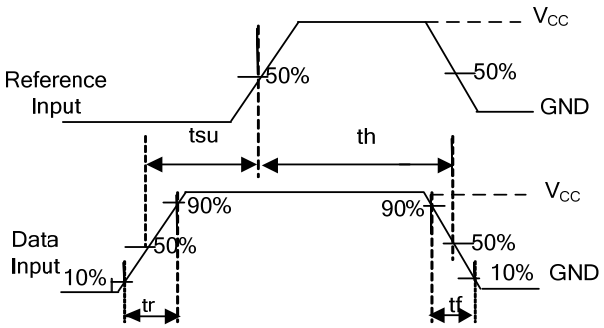
■ TEST CIRCUIT AND WAVEFORMS



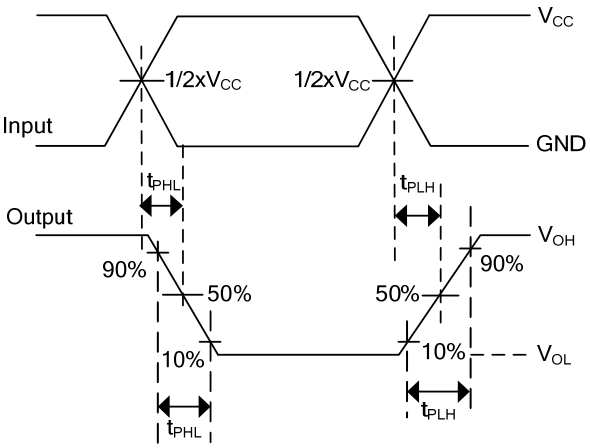
TEST CIRCUIT



PULSE WIDTH



SETUP TIME AND HOLD TIME



PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Notes: 1. C_L includes probe and jig capacitance. C_L=50pF, R_L=1KΩ.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.
3. The outputs are measured one at a time, with one input transition per measurement.