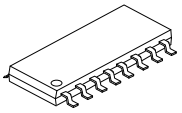
U74HCT7046

CMOS IC

PHASE LOCKED LOOP WITH VCO & LOCK DETECTOR



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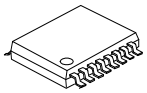


TSSOP-16

■ DESCRIPTION

The **U74HCT7046** is phase-locked-loop circuit that comprise a linear voltage-controlled oscillator (VCO), two-phase comparators (PC1, PC2), a lock detector, a common signal input amplifier and a common comparator input.

The lock detector capacitor should be connected between pin 15(CLD) and pin 8(GND).For a frequency range of 100kHz to 10MHz,the lock detector capacitor must be 1000pF to 10pF,respectively.

The signal can be directly coupled to large voltage signals, or with a series capacitor coupled to small signals. Small voltage signals can be kept within the linear region of the input amplifiers with a self-bias input circuit. The **U74HCT7046** and a passive low-pass filter form a second-order loop PLL. With a linear op-amp, the VCO achieves excellent linearity.

The VCO requires external capacitor and resistor. R1 (between R1 and GND) and capacitor C1 (between C1A and C1B) determine the frequency range of the VCO. R2 (between R2 and GND) enables the VCO to have a frequency offset if required.

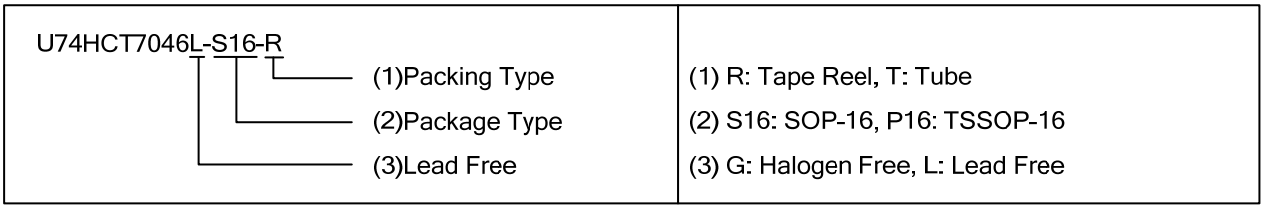
For the high input impedance of the VCO, the design of low-pass filters is simplified, and the designer has a wide choice of resistor/capacitor ranges. At pin 10 (DEM_{OUT}), a demodulator output of the VCO input voltage is provided in order not to load the low-pass filter. In conventional techniques, the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, but the DEM_{OUT} voltage of U74HCT7046 equals the VCO input voltage. When DEM_{OUT} is used, a load resistor (RS) should be connected from DEM_{OUT} to GND; but if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly or via a frequency-divider to the comparator input ($COMP_{IN}$). If the VCO input is held at a constant DC level, the VCO output signal has a duty factor of 50% (maximum expected deviation 1%). A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

■ FEATURES

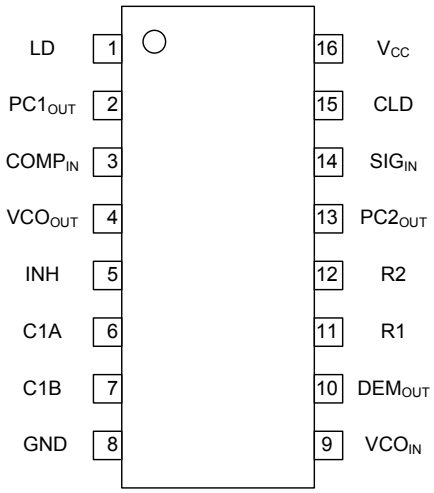
* Operating Power Supply Voltage Range: Digital Section 4.5 to 5.5 V
  VCO Section 4.5 to 5.5 V
* Up to 18 MHz (typ.) Centre Frequency at V_{CC} = 5V
* Excellent V_{CO} Frequency Linearity
* VCO-Inhibit Control For ON/OFF Keying and for Low Standby Power Consumption
* Minimal Frequency Drift
* Zero Voltage Offset due to OP-Amp Buffering

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT7046L-S16-R	U74HCT7046G-S16-R	SOP-16	Tape Reel
U74HCT7046L-S16-T	U74HCT7046G-S16-T	SOP-16	Tube
U74HCT7046L-P16-R	U74HCT7046G-P16-R	TSSOP-16	Tape Reel
U74HCT7046L-P16-T	U74HCT7046G-P16-T	TSSOP-16	Tube



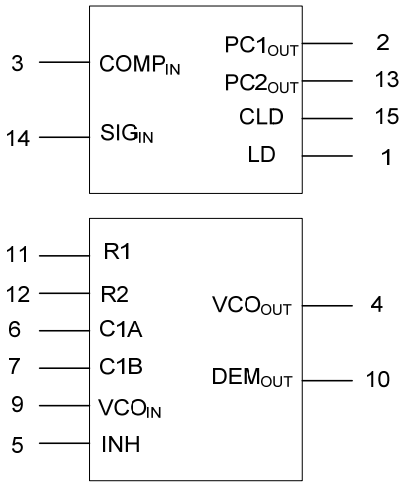
■ PIN CONFIGURATION



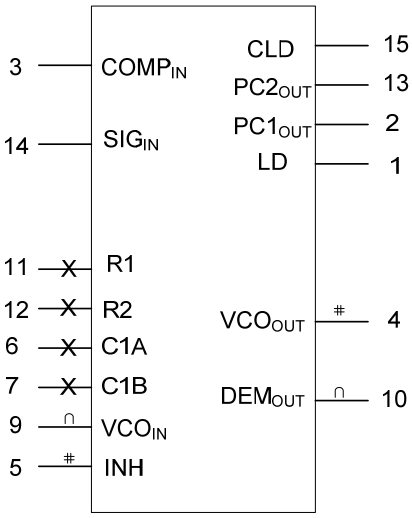
■ PIN DESCRIPTION

PIN NO	SYMBOL	FUNCTION
1	LD	Lock Detector Output(Active High)
2	$PC1_{OUT}$	Phase comparator 1output
3	$COMP_{IN}$	Comparator input
4	VCO_{OUT}	VCO output
5	INH	Inhibit input
6	$C1_A$	Capacitor C1 connection A
7	$C1_B$	Capacitor C1 connection B
8	GND	Ground(0V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	Demodulator output
11	R1	Resistor R1 connection
12	R2	Resistor R2 connection
13	$PC2_{OUT}$	Phase comparator 2 output
14	SIG_{IN}	Signal input
15	C_{LD}	Lock Detector Capacitor Input
16	V_{CC}	Positive supply voltage

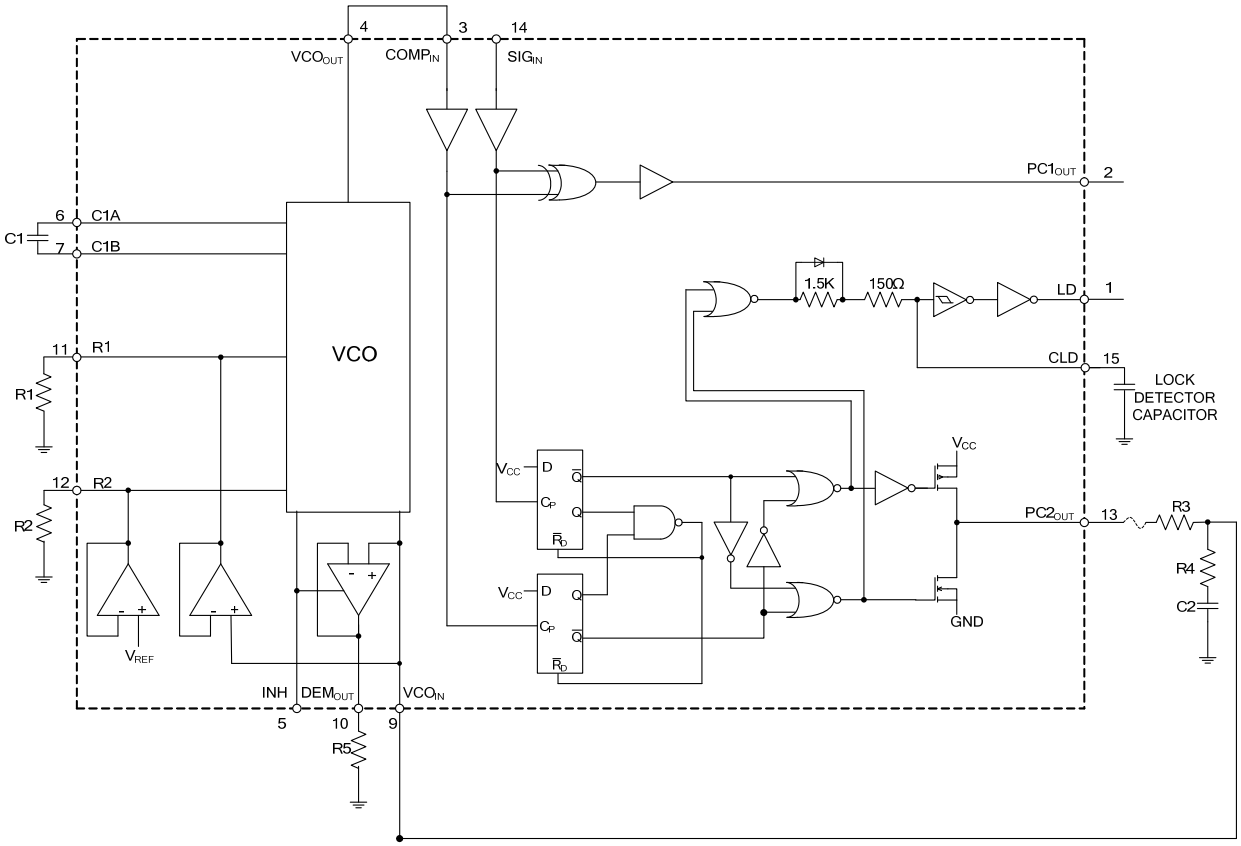
■ LOGIC SYMBOL



■ IEC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage	V_{CC}		-0.5		+7	V
DC Input Diode Current	$\pm I_{IK}$	for $V_{IN}<-0.5V$ or $V_{IN}>V_{CC}+0.5V$			20	mA
DC Output Diode Current	$\pm I_{OK}$	for $V_{OUT}<-0.5V$ or $V_{OUT}>V_{CC}+0.5V$			20	mA
DC Output Source or Sink Current	$\pm I_O$	for $-0.5V<V_{OUT}<V_{CC}+0.5V$			25	mA
DC VCC or GND Current	$\pm I_{CC}$ / I_{GND}				50	mA
Storage Temperature Range	T_{STG}		-65		+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage	V_{CC}		4.5	5.0	5.5	V
DC Supply Voltage if VCO Section is not used	V_{CC}		4.5	5.0	5.5	V
DC Input Voltage Range	V_{IN}		0		V_{CC}	V
DC Output Voltage Range	V_{OUT}		0		V_{CC}	V
Input Rise and Fall Times (pin 5)	t_R, t_F	V_{CC} = 4.5V		6.0	500	ns
Ambient Operating Temperature	T_{OPR}	see DC and AC CHARACTERISTICS	-40		+85	°C
			-40		+125	°C

■ DC CHARACTERISTICS (T_A =25°C , unless otherwise specified)

Quiescent Supply Current (Voltages are referenced to GND, Ground = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_I= V_{CC} or GND			8.0	μA
Additional Quiescent Device Current Per Input Pin:1 Unit Load	ΔI_{CC}	V_{CC}=4.5V~ 5.5V, V_I= V_{CC} -2.1V (Pin 5 is excluded)		100	360	uA

Phase Comparator Section

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Coupled (HIGH Level Input Voltage SIG_{IN}, $COMP_{IN}$)	V_{IH}	V_{CC}=4.5V	3.15	2.4		V
DC Coupled (LOW Level Input Voltage SIG_{IN}, $COMP_{IN}$)	V_{IL}	V_{CC}=4.5V		2.1	1.35	V
HIGH Level Output Voltage (LD,PC_{nOUT}) CMOS Loads	V_{OH}	V_I=V_{IH} or V_{IL}, V_{CC}=4.5V, $-I_{OUT}$ = 20μA	4.4	4.5		V
HIGH Level Output Voltage (LD,PC_{nOUT}) CMOS Loads	V_{OH}	V_I=V_{IH} or V_{IL}, V_{CC}=4.5V, $-I_{OUT}$ =4.0 mA	3.98	4.32		V
LOW Level Output Voltage (LD,PC_{nOUT}) TTL Loads	V_{OL}	V_I=V_{IH} or V_{IL}, V_{CC}=4.5V, $-I_{OUT}$ = 20μA		0	0.1	V
LOW Level Output Voltage (LD,PC_{nOUT}) TTL Loads	V_{OL}	V_I=V_{IH} or V_{IL}, V_{CC}=4.5V, $-I_{OUT}$ =4.0 mA		0.15	0.26	V
Input Leakage Current (SIG_{IN}, $COMP_{IN}$)	$\pm I_{IN}$	V_I =GND to V_{CC}, V_{CC}=5.5V			±30	μA
3-State (OFF-state current $PC2_{OUT}$)	$\pm I_{OZ}$	V_{OUT} = V_{CC} or GND, V_I=V_{IH} or V_{IL}, V_{CC}=5.5V			±0.5	μA
Input Resistance (SIG_{IN}, $COMP_{IN}$)	R_{IN}	V_{CC}=4.5V, V_{IN} at self-bias operating point, ΔV_I = 0.5V(Fig. 7)		250		kΩ

■ DC CHARACTERISTICS (Cont.)

VCO Section (Voltages are Referenced to GND, Ground=0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH Level Input Voltage INH	V_{IH}	V_{CC}=4.5V~5.5V	2	1.6		V
LOW Level Input Voltage INH	V_{IL}	V_{CC}=4.5V~5.5V		1.2	0.8	V
HIGH Level Output Voltage VCO_{OUT}	V_{OH}	V_I=V_{IH} or V_{IL} V_{CC}=4.5V, -I_{OUT} = 20μA	4.4	4.5		V
HIGH Level Output Voltage VCO_{OUT}	V_{OH}	V_{CC}=4.5V, -I_{OUT} = 4.0 Ma V_I=V_{IH} or V_{IL}	3.9	4.3		V
LOW Level Output Voltage VCO_{OUT}	V_{OL}	V_I=V_{IH} or V_{IL} V_{CC}=4.5V, I_{OUT} = 20μA		0	0.1	V
LOW Level Output Voltage VCO_{OUT}	V_{OL}	V_I=V_{IH} or V_{IL} V_{CC}=4.5V, I_{OUT} = 4.0 mA		0.15	0.26	V
LOW Level Output Voltage $C1_A$, $C1_B$	V_{OL}	V_I=V_{IH} or V_{IL} V_{CC}=4.5V, I_{OUT} = 4.0 mA			0.4	V
Input Leakage Current(INH, VCO_{IN})	±I_{IN}	V_{CC}=5.5V, V_I=GND to V_{CC}			±0.1	μA
Resistance Range	R1 / R2	V_{CC}=4.5V (Note1)	3.0		300	kΩ
Capacitor Range	C1	V_{CC}=4.5V (no limit Max.)	40			pF
Operating Voltage Range at VCO_{IN}	V_{VCOIN}	V_{CC}=4.5V, Over the range specified for R1; for linearity (Fig10)	1.1		3.4	V

Note: 1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/ or R2 are/is>10 kΩ.

Demodulator Section (Voltages are Referenced to GND (Ground=0V))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resistor Range	R_S	V_{CC}=4.5V, At R_S>300kΩ the leakage current can influence V_{DEMOUT}	50		300	kΩ
Offset Voltage VCO_{IN} to V_{DEMOUT}	V_{OFF}	V_{CC}=4.5V, V_I = V_{VCOIN} =1/2 V_{CC}, values taken over R_S range		±20		mV
Dynamic Output Resistance at DEM_{OUT}	R_D	V_{CC}=4.5V, V_{DEMOUT} = 1/2 V_{CC}		25		Ω

■ AC CHARACTERISTICS (T_A =25°C , unless otherwise specified)

Phase Comparator Section (GND=0V, t_R=t_F=6ns, C_L=50pF)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$	t_{PHL}/ t_{PLH}	V_{CC}=4.5V (Fig.8)		21	40	ns
Output Transition time	t_{THL}/ t_{TLH}	V_{CC}=4.5V (Fig.8)		7	15	ns
3-State Output Enable Time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PZH}/ t_{PZL}	V_{CC}=4.5V (Fig.9)		27	56	ns
3-State Output Disable Time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PHZ}/ t_{PLZ}	V_{CC}=4.5V (Fig.9)		35	65	ns
AC Coupled Input Sensitivity (Peak-To-Peak Value) at SIG_{IN} or $COMP_{IN}$	$V_{IN(P-P)}$	V_{CC}=4.5V (f_i = 1MHz)		15		mV

VCO Section (GND=0V, t_R=t_F=6ns, C_L=50pF)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Stability with Temperature Change	Δf/T	V_{CC}=4.5V, V_{IN}=V_{VCOIN}=1/2 V_{CC}, R1=100 KΩ; R2=∞; C1=100pF		0.15		%/K
VCO Centre Frequency (duty Factor = 50%)	f_o	V_{CC}=4.5V, V_{VCOIN} = 1/2 V_{CC}, R1=3KΩ, R2 =∞, C1=40pF	11	17		MHz
VCO Frequency Linearity	Δf_{VCO}	V_{CC}=4.5V, R1=100kΩ, R2=∞,C1=100pF (Fig.10)		0.4		%
Duty factor at VCO_{OUT}	δ_{VCO}	V_{CC}=4.5V		50		%

■ PHASE COMPARATORS.

If the signal swing is between the standard HC family input logic levels, the signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. To obtain the maximum locking range, the signal and comparator input frequencies (f_I) must have a 50% duty factor.

The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

Where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The phase comparator gain is: $K_P = \frac{V_{CC}}{\pi}$ (V / r)

As shown in Fig.1, the average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}) is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$). The average of V_{DEMOUT} is equal to $V_{CC}/2$ when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_O). As shown in Fig.2 it is the typical waveforms for the PC1 loop locked at f_O.

$$V_{DEMOUT} = V_{PC1OUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

$$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$$

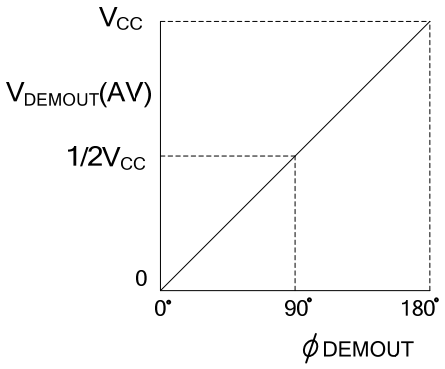


Fig.1 Phase comparator 1: average output voltage versus input phase difference.

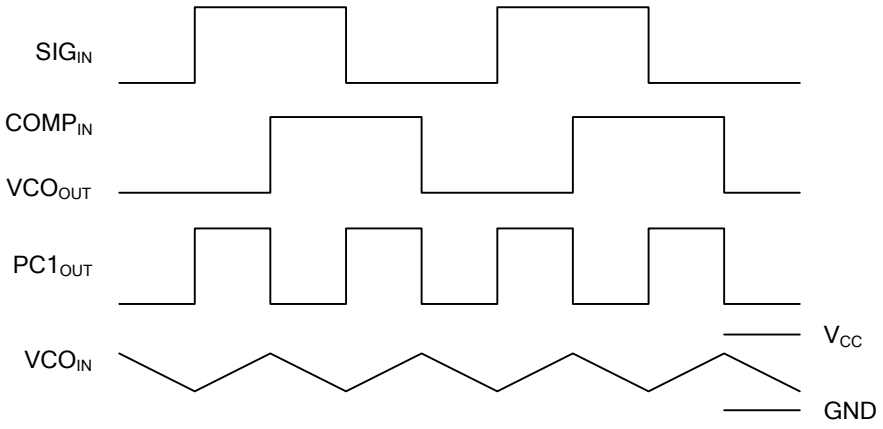


Fig.2 Typical waveforms for PLL using phase comparator 1, loop locked at f_O.

The frequency capture range ($2f_c$) is he frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the low-pass filter characteristics determine the capture range which can be made as large as the lock range.

This configuration retains lock even with very noisy input signals. Typical behavior of this type of phase

comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

■ PHASE COMPARATORS (Cont.)

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. If the PLL is using the comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 is comprised of two D-type flip-flops, control-gating and a 3-state output stage. The circuit function is as an up-down counter (Logic Diagram) for SIG_{IN} causes an up-count and $COMP_{IN}$ causes a down-count.

The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is: $K_P = \frac{V_{CC}}{4\pi}$ (V / r)

As shown in Fig.3, V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$. Typical waveforms for the PC2 loop locked at f_o are shown in Fig.4.

$$V_{DEMOUT} = V_{PC2OUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

$$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$$

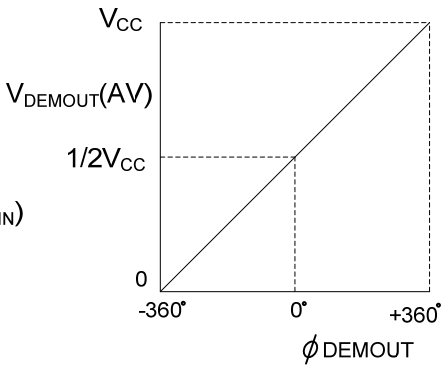


Fig.3 Phase comparator 2: average output voltage versus input phase difference.

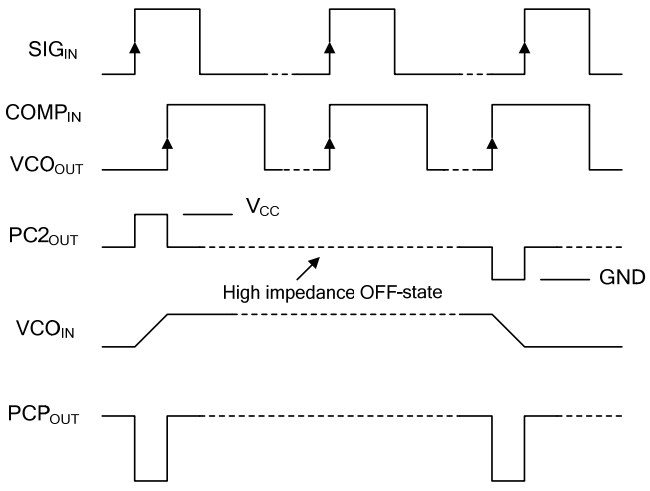


Fig.4 Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

■ PHASE COMPARATORS (Cont.)

If the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held “ON” for a time corresponding to the phase difference (φ_{DEMOUT}). If the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held “ON”.

If the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held “ON” for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are “OFF” (3-state). If the frequency of SIG_{IN} is lower than that of $COMP_{IN}$, the n-type driver that is held “ON” for most of the cycle. Then the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable state the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in the condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level, and it indicates a locked condition.

For PC2, there is no phase difference between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. And as the low-pass filter, the power dissipation is reduced because both p and n-type drivers are “OFF” for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and this is independent of the low-pass filter. The VCO adjusts to its lowest frequency via PC2 when no signal present at SIG_{IN}.

■ LOCK DETECTOR THEORY OF OPERATION

Detection of a locked condition is accomplished by a NOR gate and an envelope detector.When the PLL is in Lock, the output of the NOR gate is High and the lock detector output (Pin 1) is at a constant high level. As the loop tracks the signal on Pin 14 (signal in), the NOR gate outputs pulses whose widths represent the phase differ-ences between the VCO and the input signal. The time between pulses will be approximately equal to the time constant of the VCO center frequency. During the rise time of the pulse, the diode across the 1.5kΩ resistor is forward biased and the time constant in the path that charges the lock detector capacitor is T = (150Ω x CLD).

During the fall time of the pulse the capacitor discharges through the 1.5kΩ and the 150Ω resistors and the channel resistance of the n-device of the NOR gate to ground (T = (1.5kΩ + 150Ω + Rn-channel) x CLD).

The waveform preset at the capacitor resembles a sawtooth.The lock detector capacitor value is determined by the VCO center frequency. The typical range of capacitor for a frequency of 10MHz is about 10pF and for a frequency of 100kHz is about 1000pF. As long as the loop remains locked and tracking, the level of the sawtooth will not go below the switching threshold of the Schmitt-trigger inverter. If the loop breaks lock, the width of the error pulse will be wide enough to allow the sawtooth waveform to go below threshold and a level change at the output of the Schmitt trigger will indicate a loss of lock. The lock detector capacitor also acts to filter out small glitches that can occur when the loop is either seeking or losing lock.

■ FIGURE REFERENCES FOR DC CHARACTERISTICS

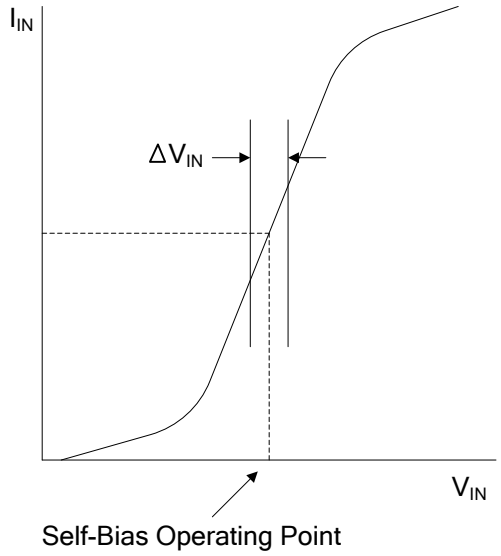


Fig.7 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

■ AC WAVEFORMS

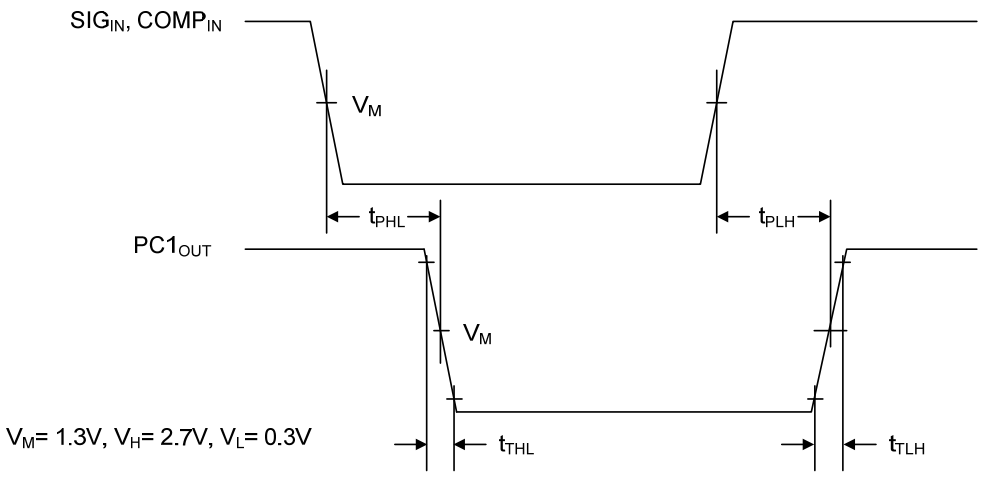


Fig.8 Waveforms showing input (SIG$_{IN}$, COMP$_{IN}$) to output (PC1$_{OUT}$) propagation delays and the output transition times.

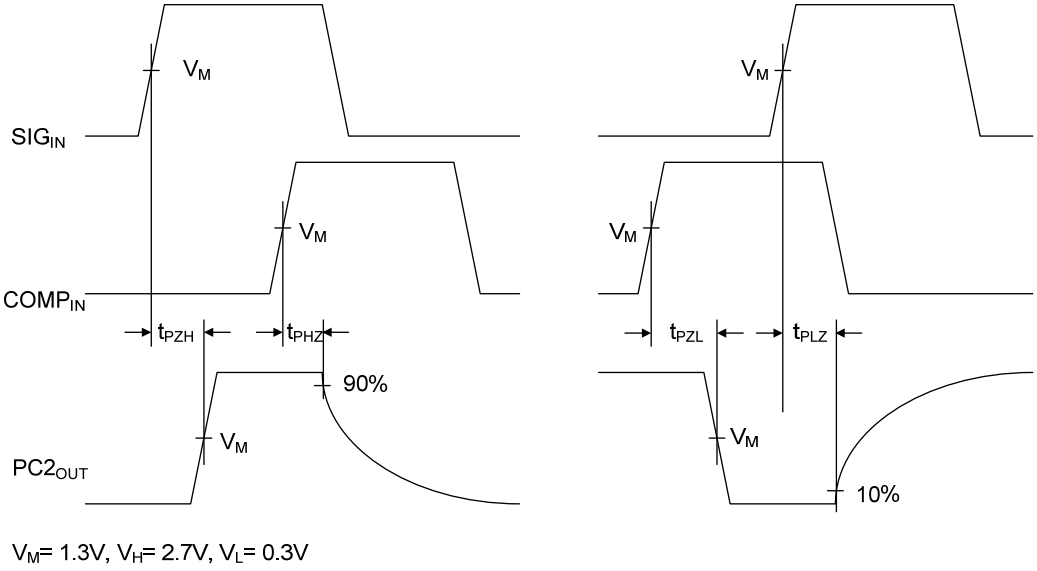


Fig.9 Waveforms showing the 3-state enable and disable times for PC2$_{OUT}$.

■ AC WAVEFORMS(Cont.)

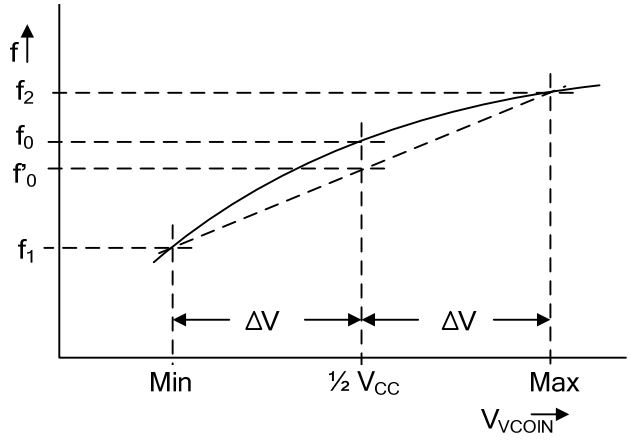


Fig.10 Definition of VCO frequency linearity: ΔV = 0.5 V over the VCC range:
for VCO linearity $f'_0 = (f_1+f_2)/2$, linearity $(f'_0+f_0)/f'_0 \times 100\%$

■ APPLICATION INFORMATION

This is a reference for the values of external components to be used with the **U74HCT7046** in a PLL system. The ranges of the values of the components:

Component	Value
R1	3 kΩ ~ 300 kΩ
R2	3 kΩ ~ 300 kΩ
R1+R2	Parallel value > 2.7 kΩ
C1	Greater than 40 pF

VCO Frequency Without Extra Offset (Phase comparator: PC1, PC2)
Frequency Characteristic:
With R2 = ∞ and R1 between 3 kΩ and 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.11 (Due to R1, C1 time constant a small offset remains when R2=∞).

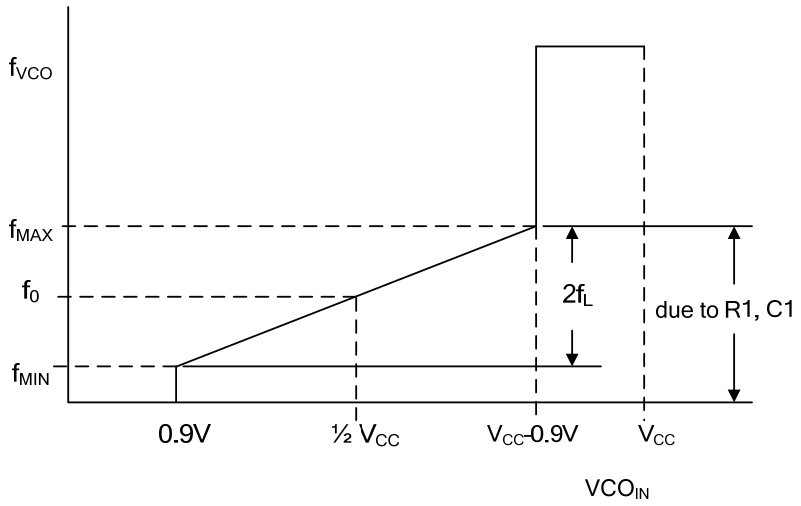


Fig.11 Frequency characteristic of VCO operating without offset:
f_0 = centre frequency; $2f_L$ = frequency lock range.

■ APPLICATION INFORMATION(Cont.)

VCO Frequency with Extra Offset (Phase Comparator: PC1, PC2)
Frequency characteristic:
With R1 and R2 between 3 kΩ and 300 kΩ, the characteristics of the VCO operation will be as shown in Fig.12.

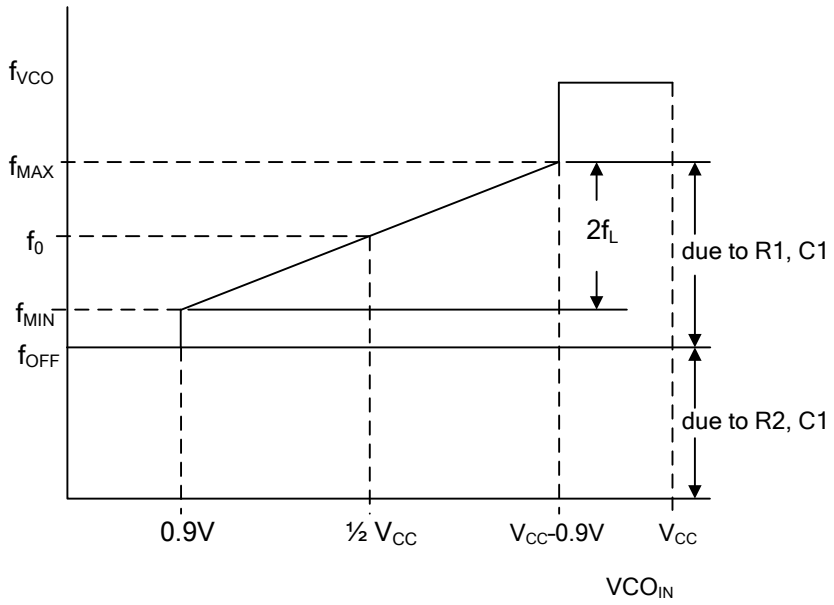
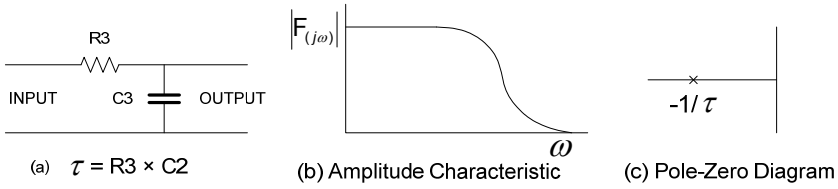


Fig.12 Frequency characteristic of VCO operating with offset:
f_0 = centre frequency; $2f_L$ = frequency lock range.
PC1, PC2
Selection of R1, R2 and C1
Given f_o and f_L, determine the value of R1×C1
Calculate f_{OFF} from the equation $f_{OFF} = f_O - 1.6f_L$
Obtain the values of C1 and R2
Calculate the value of R1 from the value of C1 and R1×C1.

Subject	Phase comparator	Design considerations
PLL Conditions with no Signal at the SIG_{IN} Input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCONIN} = 1/2 V_{CD} (Fig.1).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = -360° and V_{VCONIN} = min. (Fig.3).

■ APPLICATION INFORMATION(Cont.)

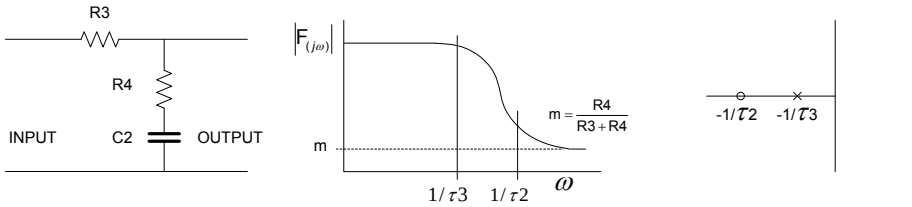
PLL Frequency Capture Range (Phase comparator: PC1, PC2)
Loop filter component selection



(a) τ = R3 × C2 (b) Amplitude Characteristic (c) Pole-Zero Diagram

A small capture range ($2f_C$) is obtained if $2f_C \approx \frac{1}{\pi}\sqrt{2\pi\, f_L / \tau}$

Fig.13 Simple loop filter for PLL without offset; R3 ⩾ 500 Ω.



(a) $\tau 1$ = R3 × C2
$\tau 2$ = R4 × C2
$\tau 3$ = (R3 + 4)× C2

(b) Amplitude Characteristic (c) Pole-Zero Diagram

Fig.14 Simple loop filter for PLL with offset; R3 + R4 ⩾ 500 Ω.

Subject	Phase comparator	Design considerations
PLL Locks on Harmonics at Centre Frequency	PC1	Yes
	PC2	No
Noise Rejection at Signal Input	PC1	High
	PC2	Low
AC Ripple Content when PLL is Locked	PC1	$f_r = 2f_i$, large ripple content at φ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at φ_{DEMOUT} = 0°