



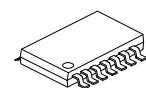
U74LV164

CMOS IC

8-BIT SERIAL-IN/ PARALLEL-OUT SHIFT REGISTER

■ DESCRIPTION

The **U74LV164** is an 8-bit serial-in/parallel-out shift register. The logical AND of the A and B enters into Qn and shifts one place to right on each LOW-to-HIGH transition of the clock (CLK). A low level on the reset (\bar{CLR}) input clears all the register asynchronously and force all output LOW.



TSSOP-14

■ FEATURES

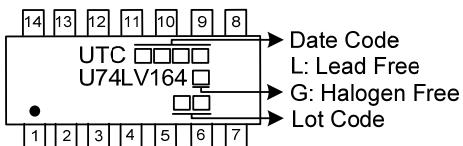
- * Wide supply voltage range from 2V to 5.5V
- * Inputs accept voltages up to 5.5V
- * Low static power consumption; $I_{CC}=20\mu A$ (Max.)
- * Optimized for 3.3V Operation
- * Support Mixed-Mode Voltage Operation on All Ports

■ ORDERING INFORMATION

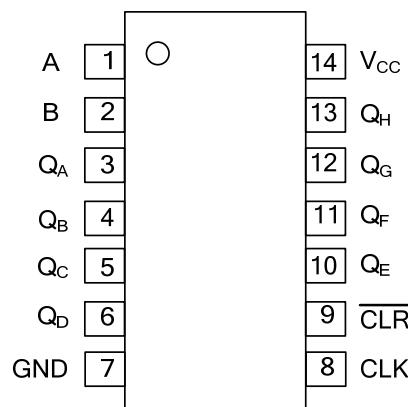
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LV164L-P14-R	U74LV164G-P14-R	TSSOP-14	Tape Reel

U74LV164G-P14-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ PIN CONFIGURATION

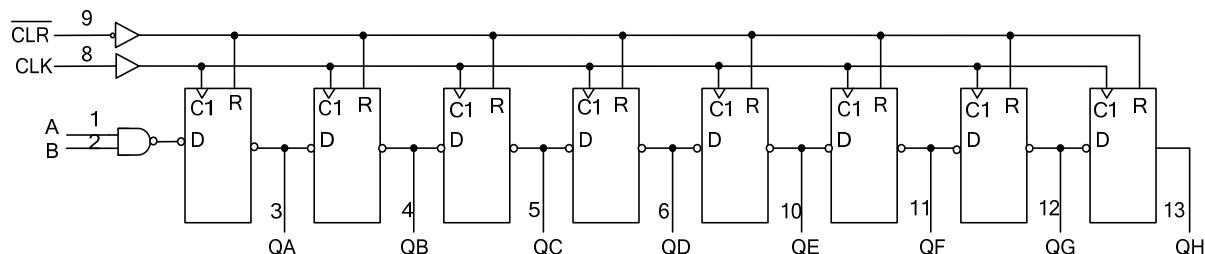


■ FUNCTION TABLE (each gate)

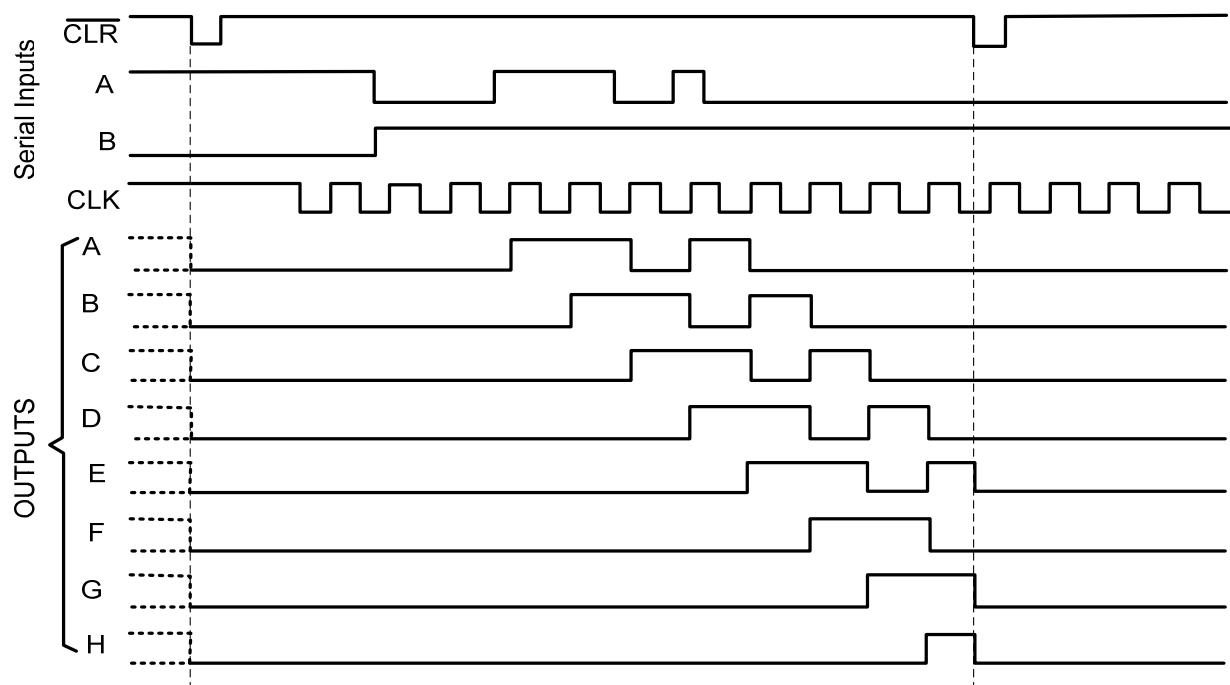
INPUTS				OUTPUTS			
$\overline{\text{CLR}}$	CLK	A	B	Q_A	Q_B	Q_H	
L	X	X	X	L	L	L	
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}	
H	↑	H	H	H	Q_{An}	Q_{Gn}	
H	↑	L	X	L	Q_{An}	Q_{Gn}	
H	↑	X	L	L	Q_{An}	Q_{Gn}	

H = High voltage level ; L = Low voltage level ; X = Don't care

■ LOGIC DIAGRAM (positive gate)



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage (Note 2)	V_{IN}		-0.5 ~ +7.0	V
Output Voltage	V_{OUT}		-0.5 ~ +7.0	V
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	± 25	mA
Input Clamp Current	I_{IK}	$V_{IN} < 0$ or $V_{IN} > V_{CC}$	-20	mA
Output Clamp Current	I_{OK}	$V_{OUT} < 0$ or $V_{OUT} > V_{CC}$	-50	mA
Continuous Current Through V_{CC} or GND	I_{CC}		± 50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=2.5V \pm 0.2V$			200	ns/V
		$V_{CC}=3.3V \pm 0.3V$			100	ns/V
		$V_{CC}=5.0V \pm 0.5V$			20	ns/V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High Level Input Voltage	V _{IH}	V _{CC} =2V	1.5			1.5			V
		V _{CC} =2.5V±0.2V	0.7			0.7			V
		V _{CC} =3.3V±0.3V	0.7	xV _{CC}		0.7	xV _{CC}		V
		V _{CC} =5.0V±0.5V	0.7	xV _{CC}		0.7	xV _{CC}		V
Low Level Input Voltage	V _{IL}	V _{CC} =2.0V			0.5			0.5	V
		V _{CC} =2.5V±0.2V			0.3xV _{CC}			0.3xV _{CC}	V
		V _{CC} =3.3V±0.3V			0.3xV _{CC}			0.3xV _{CC}	V
		V _{CC} =5.0V±0.5V			0.3xV _{CC}			0.3xV _{CC}	V
High-Level Output Voltage	V _{OH}	V _{CC} =2V ~ 5.5V, I _{OH} =-50μA	V _{CC} -0.1			V _{CC} -0.1			V
		V _{CC} =2.3V, I _{OH} =-2mA	2			2			V
		V _{CC} =3V, I _{OH} =-6mA	2.48			2.2			V
		V _{CC} =4.5V, I _{OH} =-12mA	3.8			3.5			V
Low-Level Output Voltage	V _{OL}	V _{CC} =2V ~ 5.5V, I _{OL} =50μA			0.1			0.1	V
		V _{CC} =2.3V, I _{OL} =2mA			0.4			0.4	V
		V _{CC} =3V, I _{OL} =6mA			0.44			0.5	V
		V _{CC} =4.5V, I _{OL} =12mA			0.55			0.65	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0~5.5V, V _{IN} =V _{CC} or GND			±1			±1	μA
Quiescent Supply Current	I _{CC}	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0A			20			160	μA
Additional Quiescent Supply Current Per Input Pin	ΔI _{CC}	V _{CC} =5.5V, One input at 0.6V, Other inputs at V _{CC} or GND			500			850	μA

■ TIMING REQUIREMENTS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Pulse duration CLK High or Low	t _w	V _{CC} =2.5±0.2V	9			11			ns
		V _{CC} =3.3±0.3V	8			10			ns
		V _{CC} =5±0.5V	8			10			ns
Pulse duration CLR Low	t _w	V _{CC} =2.5±0.2V	9.5			12			ns
		V _{CC} =3.3±0.3V	8			10			ns
		V _{CC} =5±0.5V	8			10			ns
Setup Time A and B to CLK ↑	t _{su}	V _{CC} =2.5±0.2V	9.5			12			ns
		V _{CC} =3.3±0.3V	8			10			ns
		V _{CC} =5±0.5V	7.5			10			ns
Setup Time CLR inactive	t _{su}	V _{CC} =2.5±0.2V	6			8			ns
		V _{CC} =3.3±0.3V	5.5			7.5			ns
		V _{CC} =5±0.5V	5.5			7.5			ns
Hold Time A and B to CLK ↑	t _h	V _{CC} =2.5±0.2V	0			2			ns
		V _{CC} =3.3±0.3V	0			2			ns
		V _{CC} =5±0.5V	1			3			ns

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

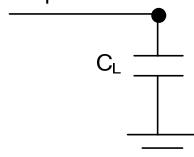
PARAMETER	SYMBOL	TEST CONDITIONS			$T_A=25^\circ C$			$T_A=-40^\circ C \sim +125^\circ C$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Maximum frequency	f_{MAX}	$C_L=15pF, R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$	45	90		35				MHz
			$V_{CC}=3.3\pm0.3V$	65	110		55				MHz
			$V_{CC}=5\pm0.5V$	95	140		75				MHz
		$C_L=50pF, R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$	35	75		25				MHz
			$V_{CC}=3.3\pm0.3V$	50	100		40				MHz
			$V_{CC}=5\pm0.5V$	80	120		65				MHz
Propagation delay from input (CLK) to output(Q)	t_{PD}	$C_L=15pF, R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$		11	20	1		23	ns	
			$V_{CC}=3.3\pm0.3V$		9	15	1		18	ns	
			$V_{CC}=5\pm0.5V$		7	10	1		13	ns	
		$C_L=50pF, R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$		13	25	1		28	ns	
			$V_{CC}=3.3\pm0.3V$		10	19	1		22	ns	
			$V_{CC}=5\pm0.5V$		8	12	1		15	ns	
Propagation delay from input (\overline{CLR}) to output(Q)	t_{PHL}	$C_L=15pF, R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$		10	16	1		19	ns	
			$V_{CC}=3.3\pm0.3V$		8	13	1		16	ns	
			$V_{CC}=5\pm0.5V$		6	9	1		12	ns	
		$C_L=50pF, R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$		11	20	1		23	ns	
			$V_{CC}=3.3\pm0.3V$		9	17	1		20	ns	
			$V_{CC}=5\pm0.5V$		7	11	1		14	ns	

■ OPERATING CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=3.3V, f=10MHz$		48		pF
Input Capacitance	C_{IN}	$V_{CC}= 3.3V, V_{IN}= V_{CC} \text{ or GND}$		2.2		pF

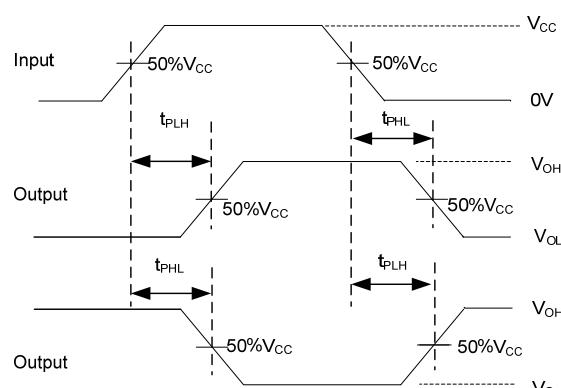
■ TEST CIRCUIT AND WAVEFORMS

From Output

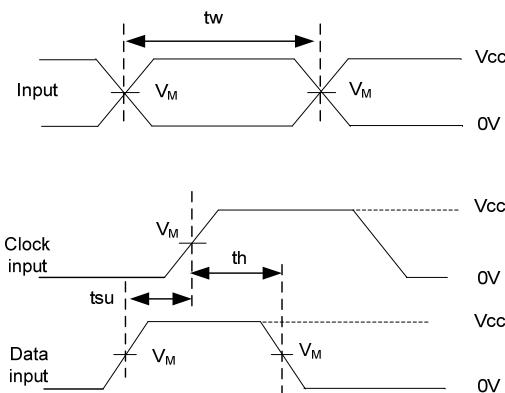


TEST CIRCUIT

Note : C_L includes probe and jig capacitance.



PROPAGATION DELAY TIMES



PROPAGATION DELAY FROM INPUT TO OUTPUT AND
INPUT VOLTAGE WAVEFORMS.

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{MHz}$, $Z_O = 50\Omega$.

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