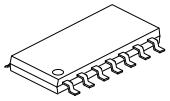
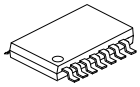
U74LVC125A

CMOS IC

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS



SOP-14



TSSOP-14

■ DESCRIPTION

The **U74LVC125A** consists of four bus buffers with 3-state output controlled by enable input ($\overline{OE}$), when $\overline{OE}$ is high, the output is disable.

Inputs can be driven from either 3.3V or 5V devices, so the device can be used in a mix 3.3V/5V system.

■ FEATURES

* Operation Voltage Range: 1.65~3.6V
* Low Power Dissipation
* Input Accept Voltage to 5.5V

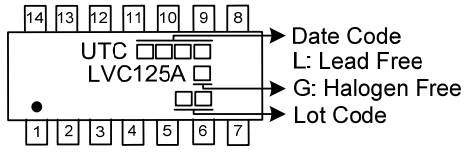
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC125AL-S14-R	U74LVC125AG-S14-R	SOP-14	Tape Reel
U74LVC125AL-P14-R	U74LVC125AG-P14-R	TSSOP-14	Tape Reel

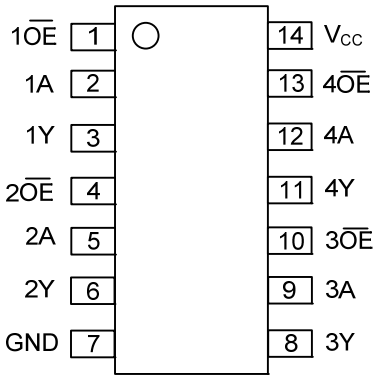
U74LVC125AG-S14-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S14: SOP-14, P14: TSSOP-14
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



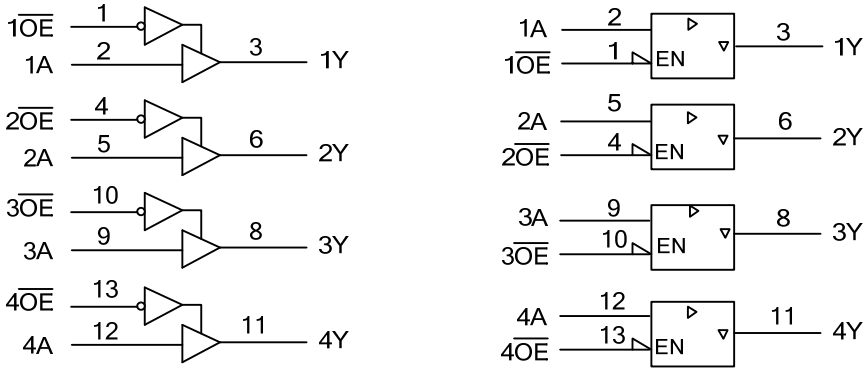
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT		OUTPUT
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 6.5	V
Input Voltage	V_{IN}	-0.5 ~ 6.5	V
Output Voltage(active mode)	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Clamp Current(V_{iN}<0)	I_{IK}	-50	mA
Output Clamp Current(V_O<0)	I_{OK}	-50	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
		Data retention only	1.5			
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Rise or Fall Times	t_R, t_F				8	ns/V
Operating Temperature	T_A		-40		+125	°C

■ STATIC CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=1.65V ~ 1.95V	0.65× V_{CC}			V
		V_{CC}=2.3V ~ 2.7V	1.7			V
		V_{CC}=2.7V ~ 3.6V	2			V
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V ~ 1.95V			0.35× V_{CC}	V
		V_{CC}=2.3V ~ 2.7V			0.7	V
		V_{CC}=2.7V ~ 3.6V			0.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=1.65V ~ 3.6V, I_{OH}=-100μA	V_{CC}-0.2			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.29			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9			V
		V_{CC}=2.7V, I_{OH}=-12mA	2.2			V
		V_{CC}=3V, I_{OH}=-12mA	2.4			V
		V_{CC}=3V, I_{OH}=-24mA	2.3			V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65V ~ 3.6V, I_{OL}=100μA			0.1	V
		V_{CC}=1.65V, I_{OL}=4mA			0.24	V
		V_{CC}=2.3V, I_{OL}=8mA			0.3	V
		V_{CC}=2.7V, I_{OL}=12mA			0.4	V
		V_{CC}=3V, I_{OL}=24mA			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=3.6V, V_{IN}=5.5V or GND			±1	μA
Output OFF-State current	I_{OZ}	V_{CC}=3.6V, V_{OUT}=V_{CC} or GND			±1	μA
Quiescent Supply Current	I_Q	V_{CC}=3.6V, V_{IN}=V_{CC} or GND I_{OUT}=0			1	μA
Additional Quiescent Supply Current	Δ I_Q	V_{CC}=2.7V~3.6V, One input at V_{CC}-0.6V, other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	V_{CC}=3.3V, V_{IN}=V_{CC} or GND		5		pF

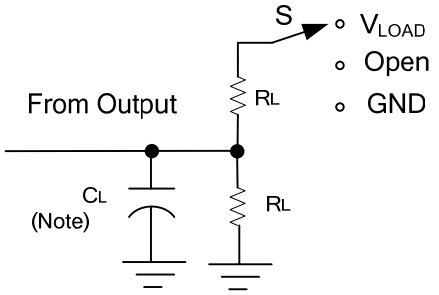
■ DYNAMIC CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output (Y)	t_{PLH}/t_{PHL}	V_{CC}=1.8V±0.15V	1	4.5	11.8	ns
		V_{CC}=2.5V±0.2V	1	2.7	5.8	ns
		V_{CC}=2.7V	1	3	5.3	ns
		V_{CC}=3.3V±0.3V	1	2.5	4.6	ns
Output enable time from input ($\overline{OE}$) to output (Y)	t_{PZL}/t_{PZH}	V_{CC}=1.8V±0.15V	1	4.3	13.8	ns
		V_{CC}=2.5V±0.2V	1	2.7	6.9	ns
		V_{CC}=2.7V	1	3.3	6.4	ns
		V_{CC}=3.3V±0.3V	1	2.4	5.2	ns
Output disable time from input ($\overline{OE}$) to output (Y)	t_{PLZ}/t_{PHZ}	V_{CC}=1.8V±0.15V	1	4.3	10.6	ns
		V_{CC}=2.V5±0.2V	1	2.2	5.1	ns
		V_{CC}=2.7V	1	2.5	4.8	ns
		V_{CC}=3.3V±0.3V	1	2.4	4.4	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=1.8V, f=10MHz		7.4		pF
		V_{CC}=2.5V, f=10MHz		11.3		pF
		V_{CC}=3.3V, f=10MHz		15		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

Note: C_L includes probe and jig capacitance.

V_{CC}	V_{IN}	$t_R,/t_F$	V_M	V_{LOAD}	C_L	R_L	$V_\triangle$
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2* V_{CC}	30pF	1KΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2* V_{CC}	30pF	500Ω	0.15V
2.7V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
3.3V±0.3V	2.7 V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V