



U74LVC2G06

CMOS IC

INVERTERS WITH OPEN-DRAIN OUTPUTS

DESCRIPTION

The **U74LVC2G06** is a dual inverting gate CMOS with open drain output and provides the Boolean function $Y = \overline{A}$ in positive logic device.

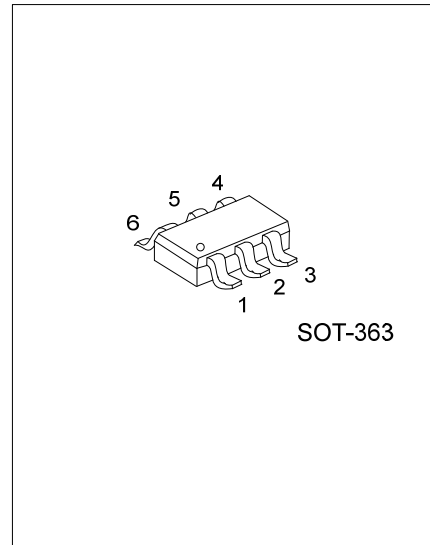
This device has a power-down protective circuit to prevent the device from destruction when it is powered down.

FEATURES

- * Operate From 1.65V to 5.5V
- * Inputs Accept Voltages to 5.5V
- * High Noise Immunity
- * Low Power Dissipation
- * Direct Interface with TTL Level

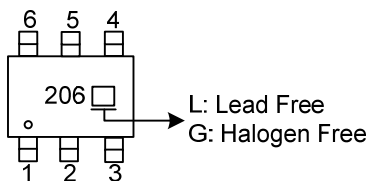
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC2G06L-AL6-R	U74LVC2G06G-AL6-R	SOT-363	Tape Reel

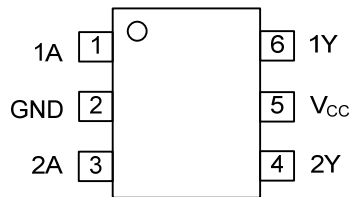


<p>U74LVC2G06G-AL6-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) AL6: SOT-363</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION

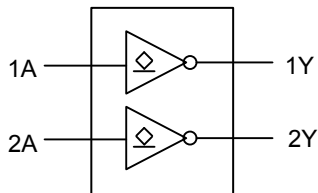


■ FUNCTION TABLE

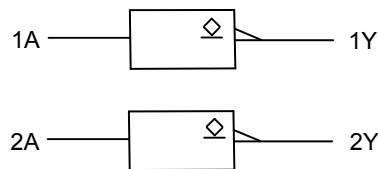
INPUT(nA)	OUTPUT(nY)
H	L
L	Z

Note: H: HIGH voltage level; L: LOW voltage level; Z: High impedance OFF-state.

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ +6.5	V
Input Voltage	V_{IN}	-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	Active mode	-0.5 ~ +6.5
		Power-down mode	-0.5 ~ +6.5
V_{CC} or GND Current	I_{CC}	±100	mA
Continuous Output Current ($V_{OUT}=0$ to V_{CC})	I_{OUT}	±50	mA
Input Clamp Current ($V_{IN}<0$)	I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}>V_{CC}$ or $V_{OUT}<0$)	I_{OK}	±50	mA
Power Dissipation ($T_A=-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$)	P_D	300	mW
Storage Temperature Range	T_{STG}	-65 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		1.65		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	Active mode	0		V_{CC}	V
		Power-down mode	0		5.5	V
Operating Temperature	T_A		-40		125	$^{\circ}\text{C}$
Input Transition Rise or Fall Rate	t_R / t_F	$V_{CC}=1.65\text{V to }2.7\text{V}$	0		20	ns/V
		$V_{CC}=2.7\text{V to }5.5\text{V}$	0		10	ns/V

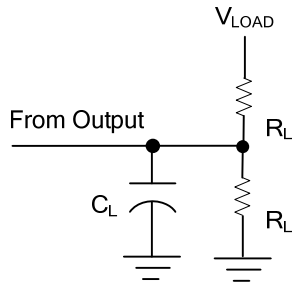
■ ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65\text{V} \sim 1.95\text{V}$	$0.65 \cdot V_{CC}$			V
		$V_{CC}=2.3\text{V} \sim 2.7\text{V}$	1.7			V
		$V_{CC}=2.7\text{V} \sim 3.6\text{V}$	2			V
		$V_{CC}=4.5\text{V} \sim 5.5\text{V}$	$0.7 \cdot V_{CC}$			V
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65\text{V} \sim 1.95\text{V}$			$0.35 \cdot V_{CC}$	V
		$V_{CC}=2.3\text{V} \sim 2.7\text{V}$			0.7	V
		$V_{CC}=2.7\text{V} \sim 3.6\text{V}$			0.8	V
		$V_{CC}=4.5\text{V} \sim 5.5\text{V}$			$0.3 \cdot V_{CC}$	V
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65 \sim 5.5\text{V}$	$I_{OL}=100\mu\text{A}$		0.1	V
		$V_{CC}=1.65\text{V}$	$I_{OL}=4\text{mA}$		0.45	V
		$V_{CC}=2.3\text{V}$	$I_{OL}=8\text{mA}$		0.3	V
		$V_{CC}=2.7\text{V}$	$I_{OL}=12\text{mA}$		0.4	V
		$V_{CC}=3.0\text{V}$	$I_{OL}=24\text{mA}$		0.55	V
		$V_{CC}=4.5\text{V}$	$I_{OL}=32\text{mA}$		0.55	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=5.5\text{V}$ or GND, $V_{CC}=5.5\text{V}$		±0.1	±5	μA
Power OFF Leakage Current	I_{OFF}	V_{IN} or $V_{OUT}=5.5\text{V}$, $V_{CC}=0\text{V}$		±0.1	±10	μA
3-state Output OFF-state Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=V_{CC}$ or GND, $V_{CC}=5.5\text{V}$		±0.1	±10	μA
Quiescent Supply Current	I_Q	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$, $V_{CC}=5.5\text{V}$		0.1	10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=2.3 \sim 5.5\text{V}$, One input at $V_{CC}-0.6\text{V}$, Other inputs at V_{CC} or GND		5	500	μA

■ SWITCHING CHARACTERISTICS (T_A=25°C)

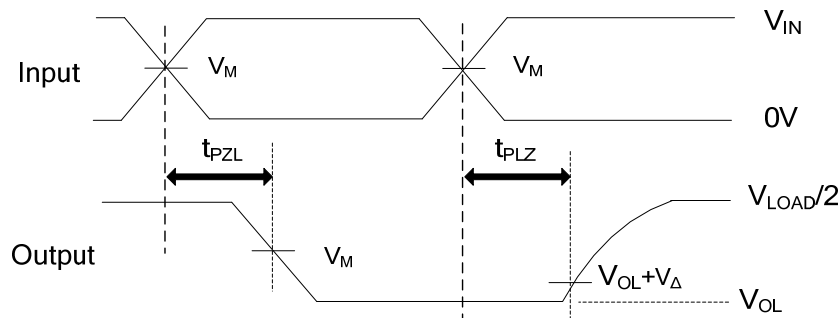
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Propagation delay from input (A) to output(Y)	t _{PLZ} / t _{PZL}	V _{CC} =1.8±0.15V, R _L =1KΩ	C _L =30pF	1.0	3.2	6.5	ns
		V _{CC} =2.5±0.2V, R _L =500Ω		0.5	2.0	3.9	ns
		V _{CC} =2.7V	R _L =500Ω, C _L =50pF	1.0	2.6	4.2	ns
		V _{CC} =3.3±0.3V		0.5	2.3	3.4	ns
		V _{CC} =5±0.5V		0.5	1.6	2.9	ns

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V _{CC}	Inputs		V _M	V _{LOAD}	V _Δ	C _L	R _L
	V _{IN}	t _R , t _F					
1.8V±0.15V	V _{CC}	≤2ns	V _{CC} /2	2 x V _{CC}	0.15V	30pF	1KΩ
2.5V±0.2V	V _{CC}	≤2ns	V _{CC} /2	2 x V _{CC}	0.15V	30pF	500Ω
2.7V	2.7V	≤2.5ns	1.5V	6V	0.3V	50pF	500Ω
3.3V±0.3V	2.7V	≤2.5ns	1.5V	6V	0.3V	50pF	500Ω
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	2 x V _{CC}	0.3V	50pF	500Ω



PROPAGATION DELAY TIMES

Note: C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_o = 50Ω.

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