

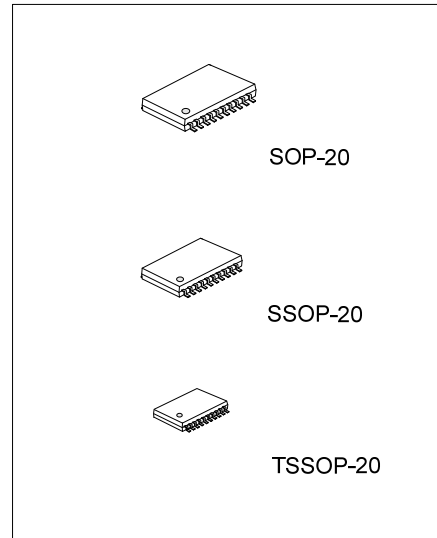


U74LVC574

Preliminary

CMOS IC

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



DESCRIPTION

The **U74LVC574** is a octal edge-triggered D-type flip-flop with 3-state outputs, and it has 8 channels.

FEATURES

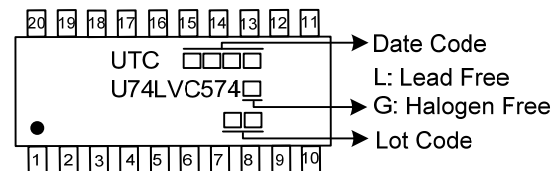
- * Operate from 1.65V to 3.6V
- * Max t_{pd} of 7ns at 3.3 V
- * Typical $V_{OL} < 0.8V$ at $V_{CC}=3.3V, T_A=25^\circ C$
- * Typical $V_{OH} > 2V$ at $V_{CC}=3.3V, T_A=25^\circ C$
- * Power off disables outputs, permitting live insertion

ORDERING INFORMATION

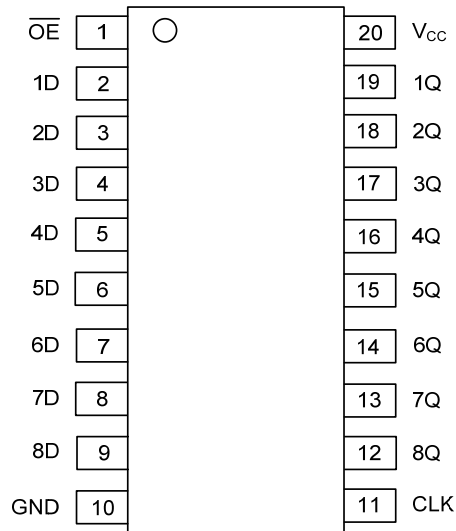
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC574L-P20-R	U74LVC574G-P20-R	TSSOP-20	Tape Reel
U74LVC574L-R20-R	U74LVC574G-R20-R	SSOP-20	Tape Reel
U74LVC574L-S20-R	U74LVC574G-S20-R	SOP-20	Tape Reel

<p>U74LVC574G-R20-R</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) P20: TSSOP-20, R20: SSOP-20, S20:SOP-20 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION

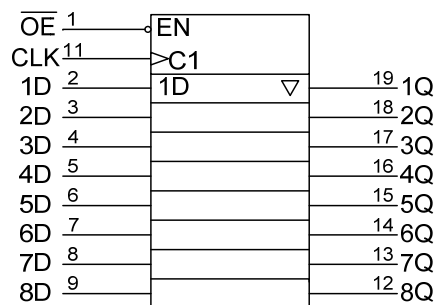


■ FUNCTION TABLE

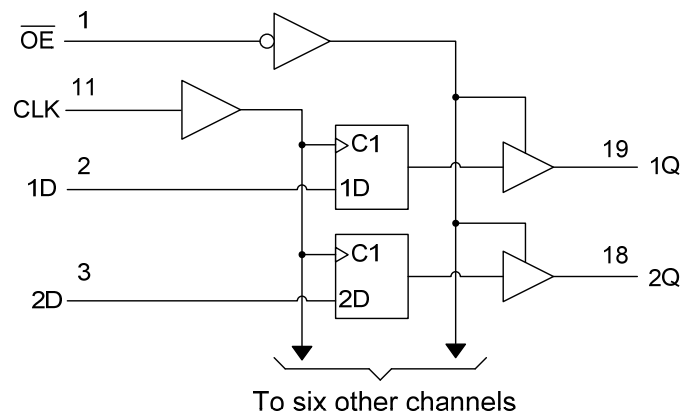
INPUTS(OE)	INPUTS(CLK)	INPUTS(D)	OUTPUT(Q)
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 6.5	V
Input Voltage	V_{IN}	-0.5 ~ 6.5	V
Output Voltage	V_{OUT}	-0.5 ~ 6.5 (Note 2)	V
		-0.5 ~ $V_{CC} + 0.5$ (Note 3)	V
V_{CC} or GND Current	I_{CC}	± 100	mA
Output Current	I_{OUT}	± 50	mA
Input Clamp Current	I_{IK}	-50	mA
Output Clamp Current	I_{OK}	-50	mA
Storage Temperature	T_{STG}	-65 ~ + 150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Voltage range applied to any output in the high-impedance or power-off state.

3. Voltage range applied to any output in the high or low state, and V_{CC} is provided in the recommended operating conditions table.

■ RECOMMENDED OPERATING CONDITIONS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
		3 state	0		5.5	V
High-level Output Current	I_{OH}	$V_{CC}=1.65\text{V}$			-4	mA
		$V_{CC}=2.3\text{V}$			-8	mA
		$V_{CC}=2.7\text{V}$			-12	mA
		$V_{CC}=3\text{V}$			-24	mA
Low-level Output Current	I_{OL}	$V_{CC}=1.65\text{V}$			4	mA
		$V_{CC}=2.3\text{V}$			8	mA
		$V_{CC}=2.7\text{V}$			12	mA
		$V_{CC}=3\text{V}$			24	mA
Input Rise or Fall Times	t_R, t_F		0		6	ns/V
Operating Temperature	T_A		-40		+125	$^\circ\text{C}$

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^\circ\text{C}$			$T_A=-40^\circ\text{C}\sim+125^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-level Input Voltage	V_{IH}	$V_{CC}=1.65\text{V}$ to 1.95V	0.65			0.65			V
		$V_{CC}=2.3\text{V}$ to 2.7V	1.7			1.7			V
		$V_{CC}=2.7\text{V}$ to 3.6V	2			2			V
Low-level Input Voltage	V_{IL}	$V_{CC}=1.65\text{V}$ to 1.95V			0.35			0.35	V
		$V_{CC}=2.3\text{V}$ to 2.7V			0.7			0.7	V
		$V_{CC}=2.7\text{V}$ to 3.6V			0.8			0.8	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage High-Level	V _{OH}	V _{CC} =1.65~3.6V, I _{OH} =-100μA	V _{CC} -0.2			V _{CC} -0.3			V
		V _{CC} =1.65V, I _{OH} =-4mA	1.2			1.05			V
		V _{CC} =2.3V, I _{OH} =-8mA	1.7			1.65			V
		V _{CC} =2.7V, I _{OH} =-12mA	2.2			2.05			V
		V _{CC} =3V, I _{OH} =-12mA	2.4			2.25			V
		V _{CC} =3V, I _{OH} =-24mA	2.2			2			V
Output Voltage Low-Level	V _{OL}	V _{CC} =1.65~3.6V, I _{OL} =100μA			0.2			0.3	V
		V _{CC} =1.65V, I _{OL} =4mA			0.45			0.65	V
		V _{CC} =2.3V, I _{OL} =8mA			0.7			0.8	V
		V _{CC} =2.7V, I _{OL} =12mA			0.4			0.6	V
		V _{CC} =3V, I _{OL} =24mA			0.55			0.8	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =3.6V, V _{IN} =0 to 5.5V			±5			±20	μA
Power OFF Leakage Current	I _{OFF}	V _{CC} =0V, V _{IN} or V _{OUT} =5.5V			±10			±20	μA
Disable Output Leakage Current	I _{OZ}	V _{CC} =3.6V, V _{OUT} =0 to 5.5V			±10			±20	μA
Quiescent Supply Current	I _Q	V _{CC} =3.6V, V _{IN} =V _{CC} or GND, I _{OUT} =0			10			40	μA
		V _{CC} =3.6V, 3.6V≤V _{IN} ≤5.5V, I _{OUT} =0(Note)			10			40	μA
Additional Quiescent Supply Current	Δ I _Q	V _{CC} =2.7~3.6V, One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			500			5000	μA

Note: This applies in the disabled state only.

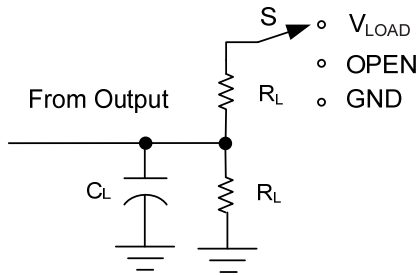
■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From Input (CLK) to Output (Q)	t _{PLH} /t _{PHL}	V _{CC} =2.7V			8			10	ns
		V _{CC} =3.3V±0.3V	2.2		7			9	ns
Propagation Delay From Input (\overline{OE}) to Output (Q)	t _{PZL} /t _{PZH}	V _{CC} =2.7V			9.5			11	ns
		V _{CC} =3.3V±0.3V	1.5		8.5			10	ns
Propagation Delay From Input (\overline{OE}) to Output (Q)	t _{PLZ} /t _{PHZ}	V _{CC} =2.7V			7			11	ns
		V _{CC} =3.3V±0.3V	1.7		6.4			7.5	ns
Maximum Clock Frequency	f _{MAX}	V _{CC} =2.7V	150			100			MHz
		V _{CC} =3.3V±0.3V	150			100			MHz
Pulse Width	t _w	V _{CC} =2.7V	3.3			3.3			ns
		V _{CC} =3.3V±0.3V	3.3			2			ns
Setup Time	t _{SU}	V _{CC} =2.7V	2			2			ns
		V _{CC} =3.3V±0.3V	2			2			ns
Hold Time	t _H	V _{CC} =2.7V	1.5			2			ns
		V _{CC} =3.3V±0.3V	1.5			2			ns

■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

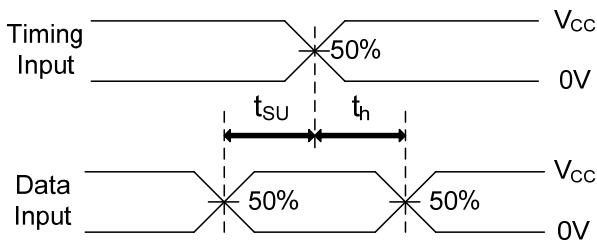
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	$V_{CC}=3.3\text{V}$, $V_{IN}=V_{CC}$ or GND		4		pF
Output Capacitance	C_O	$V_{CC}=3.3\text{V}$, $V_{OUT}=V_{CC}$ or GND		5.5		pF
Power Dissipation Capacitance	C_{PD}	$\overline{OE}=0$, $f=10\text{MHz}$, $V_{CC}=3.3\text{V}\pm 0.3\text{V}$		43		pF
		$\overline{OE}=1$, $f=10\text{MHz}$, $V_{CC}=3.3\text{V}\pm 0.3\text{V}$		15		pF

■ TEST CIRCUIT AND WAVEFORMS

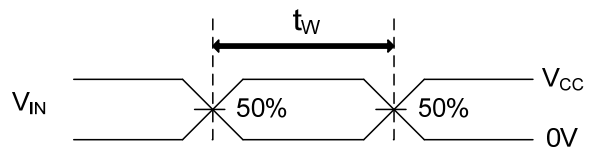


TEST CIRCUIT

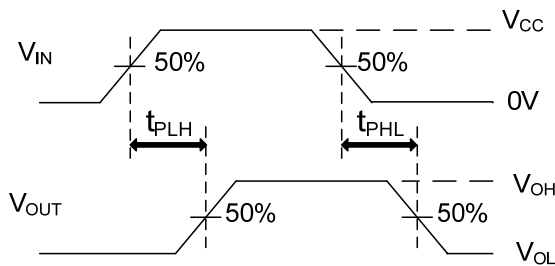
V _{CC}	V _{IN}	t _{PLZ} /t _{PZL} (V _{LOAD})	t _{PLH} /t _{PHL}	t _{PHZ} /t _{PZH}	C _L	R _L (Note 1)	ΔV
1.8V±0.15V	V _{CC}	2×V _{CC}	OPEN	OPEN	30pF	1kΩ	0.15V
2.5V±0.2V	V _{CC}	2×V _{CC}	OPEN	GND	30pF	500Ω	0.15V
2.7V	2.7V	6V	OPEN	GND	50pF	500Ω	0.3V
3.3V±0.3V	2.7V	6V	OPEN	GND	50pF	500Ω	0.3V



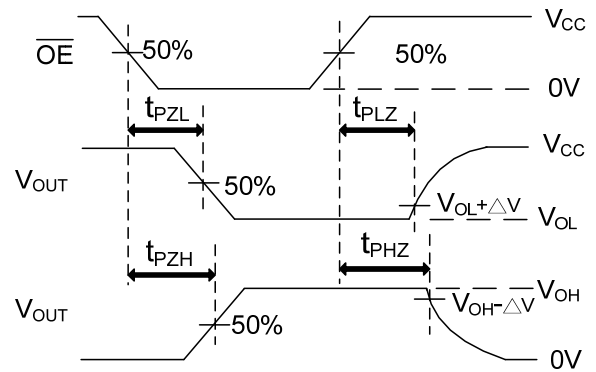
SETUP TIME AND HOLD TIME



PULSE WIDTH



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: 1. C_L includes probe and jig capacitance.
 Note: 2. PRR≤10MHz, Z_O=50Ω, t_{THL}≤2ns, t_{TLH}≤2ns.

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