



## U74LVC74A

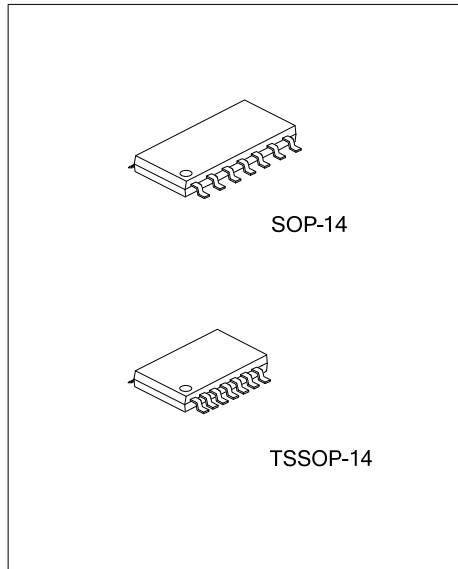
CMOS IC

### DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

#### DESCRIPTION

The **U74LVC74A** is a dual positive-edge-triggered D-type flip-flop.

The preset ( $\overline{PRE}$ ) and clear ( $\overline{CLR}$ ) input can set or reset the output, regardless of the levels of others inputs. When the  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data input meeting the set-up time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold-time interval, data D can be changed without affecting the levels at the outputs.



#### FEATURES

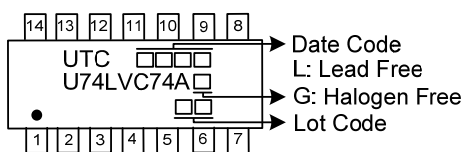
- \* 1.65V to 3.6V  $V_{CC}$  Operation
- \* Inputs Accept Voltages to 5.5V
- \* Max tpd at 5.2ns of 3.3V
- \* Typical  $V_{OLP} < 0.8V$  at  $V_{CC} = 3.3V, T_A = 25^\circ C$
- \* Typical  $V_{OHV} > 2V$  at  $V_{CC} = 3.3V, T_A = 25^\circ C$

#### ORDERING INFORMATION

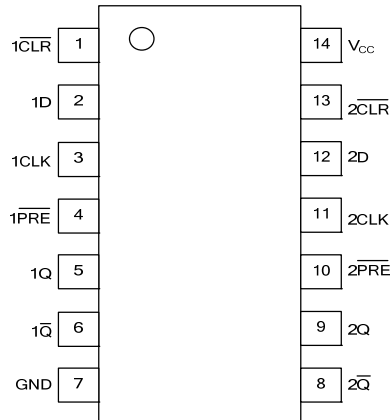
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC74AL-S14-R	U74LVC74AG-S14-R	SOP-14	Tape Reel
U74LVC74AL-P14-R	U74LVC74AG-P14-R	TSSOP-14	Tape Reel

<p>U74LVC74AG-S14-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) S14: SOP-14, P14: TSSOP-14</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING



■ PIN CONFIGURATION

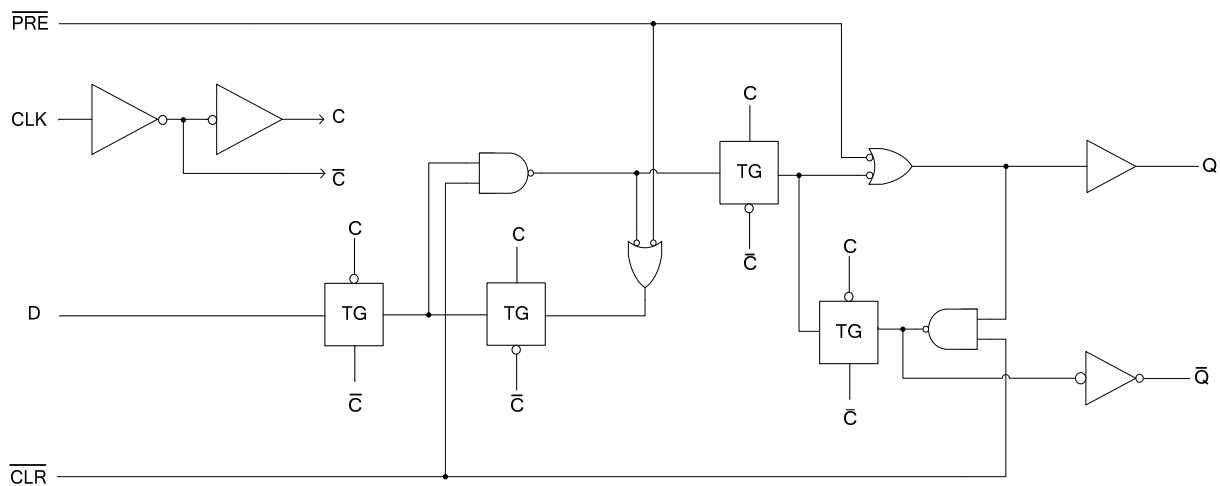


■ FUNCTION TABLE (each gate)

INPUT				OUTPUT	
PRE	CLR	CLK	D	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>+</sup>	H <sup>+</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	Q <sub>0</sub> -bar

+: This configuration is unstable, as it is not persist when either PRE or CLR return to high level.

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-0.5 ~ 6.5	V
Input Voltage	$V_{IN}$	-0.5 ~ 6.5	V
Output Voltage(active mode)	$V_{OUT}$	-0.5 ~ $V_{CC}+0.5$	V
Input Clamp Current( $V_{IN}<0$ )	$I_{IK}$	-50	mA
Output Clamp Current( $V_{OUT}<0$ )	$I_{OK}$	-50	mA
Output Current	$I_{OUT}$	$\pm 50$	mA
$V_{CC}$ or GND Current	$I_{CC}$	$\pm 100$	mA
Storage Temperature	$T_{STG}$	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$		1.65		3.6	V
Input Voltage	$V_{IN}$		0		5.5	V
Output Voltage	$V_{OUT}$		0		$V_{CC}$	V
High-level input voltage	$V_{IH}$	$V_{CC} = 1.65V \sim 1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC} = 2.3V \sim 2.7V$	1.7			
		$V_{CC} = 2.7V \sim 3.6V$	2			
Low-level input voltage	$V_{IL}$	$V_{CC} = 1.65V \sim 1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3V \sim 2.7V$			0.7	
		$V_{CC} = 2.7V \sim 3.6V$			0.8	
High-level Output Current	$I_{OH}$	$V_{CC} = 1.65V$			-4	mA
		$V_{CC} = 2.3V$			-8	
		$V_{CC} = 2.7V$			-12	
		$V_{CC} = 3V$			-24	
Low-level Output Current	$I_{OL}$	$V_{CC} = 1.65V$			4	mA
		$V_{CC} = 2.3V$			8	
		$V_{CC} = 2.7V$			12	
		$V_{CC} = 3V$			24	
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$				10	ns/V
Operating Temperature	$T_A$		-40		+85	°C

### ■ STATIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	$V_{OH}$	$V_{CC}=1.65V\sim 3.6V, I_{OH}=-100\mu A$	$V_{CC}-0.2$			V
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.7			
		$V_{CC}=2.7V$	2.2			
		$V_{CC}=3V$				
		$V_{CC}=3V, I_{OH}=-24mA$	2.2			
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=1.65V\sim 3.6V, I_{OL}=100\mu A$			0.2	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	
		$V_{CC}=2.3V, I_{OL}=8mA$			0.7	
		$V_{CC}=2.7V, I_{OL}=12mA$			0.4	
		$V_{CC}=3V, I_{OL}=24mA$			0.55	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0V\sim 3.6V$ $V_{IN}=5.5V$ or GND			$\pm 5$	$\mu A$
Quiescent Supply Current	$I_Q$	$V_{CC}=3.6V$ $V_{IN}=V_{CC}$ or GND $I_{OUT}=0$			10	$\mu A$
Additional Quiescent Supply Current	$\Delta I_Q$	$V_{CC}=2.7V$ to 3.6V One input at $V_{CC}-0.6V$ , Other inputs at $V_{CC}$ or GND			500	$\mu A$
Input Capacitance	$C_{IN}$	$V_{CC}=3.3V, V_{IN}=V_{CC}$ or GND		5		pF

### ■ DYNAMIC CHARACTERISTICS (Input: $t_R, t_F \leq 2.5ns$ ; $PRR \leq 1MHz$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Fclock Clock frequency	$f_{CLOCK}$	$V_{CC}=1.8V \pm 0.15V$			83	MHZ
		$V_{CC}=2.5V \pm 0.2V$			83	
		$V_{CC}=2.7V$			83	
		$V_{CC}=3.3V \pm 0.3V$			150	
Pulse duration	$t_W$	$V_{CC}=1.8V \pm 0.15V$	PRE or CLR Low	4.1		ns
			CLK High or Low	4.1		
		$V_{CC}=2.5V \pm 0.2V$	PRE or CLR Low	3.3		
			CLK High or Low	3.3		
		$V_{CC}=2.7V$	PRE or CLR Low	3.3		
			CLK High or Low	3.3		
		$V_{CC}=3.3V \pm 0.3V$	PRE or CLR Low	3.3		
			CLK High or Low	3.3		
Setup time before CLK $\uparrow$	$t_{SU}$	$V_{CC}=1.8V \pm 0.15V$	Data	3.6		ns
			PRE or CLR Inactive	2.7		
		$V_{CC}=2.5V \pm 0.2V$	Data	2.3		
			PRE or CLR Inactive	1.9		
		$V_{CC}=2.7V$	Data	3.4		
			PRE or CLR Inactive	2.2		
		$V_{CC}=3.3V \pm 0.3V$	Data	3		
			PRE or CLR Inactive	2		
Hold time ,data after CLK $\uparrow$	$t_H$	$V_{CC}=1.8V \pm 0.15V$	1		ns	
		$V_{CC}=2.5V \pm 0.2V$	1			
		$V_{CC}=2.7V$	1			
		$V_{CC}=3.3V \pm 0.3V$	0			

### ■ DYNAMIC CHARACTERISTICS

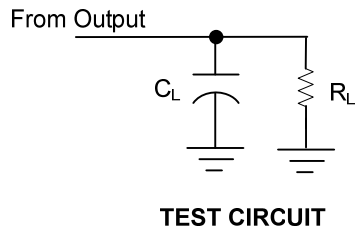
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Clock Pulse Frequency	$f_{max}$	$V_{CC}=1.8V\pm0.15V$	83			MHz
		$V_{CC}=2.5V\pm0.2V$	83			
		$V_{CC}=2.7V$	83			
		$V_{CC}=3.3V\pm0.3V$	150			
Propagation delay from input (CLK) to output(Q or Q)	$t_{PLH}/t_{PHL}$	$V_{CC}=1.8V\pm0.15V, C_L=30pF, R_L=1K\Omega$	1		7.1	ns
		$V_{CC}=2.5V\pm0.2V, C_L=30pF, R_L=500\Omega$	1		4.4	
		$V_{CC}=2.7V, C_L=50pF, R_L=500\Omega$	1		6	
		$V_{CC}=3.3V\pm0.3V, C_L=50pF, R_L=500\Omega$	1		5.2	
Propagation delay from input (PRE or CLR) to output(Q or Q)	$t_{PLH}/t_{PHL}$	$V_{CC}=1.8V\pm0.15V, C_L=30pF, R_L=1K\Omega$	1		6.9	ns
		$V_{CC}=2.5V\pm0.2V, C_L=30pF, R_L=500\Omega$	1		4.6	
		$V_{CC}=2.7V, C_L=50pF, R_L=500\Omega$	1		6.4	
		$V_{CC}=3.3V\pm0.3V, C_L=50pF, R_L=500\Omega$	1		5.4	

### ■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	$C_{PD}$	$V_{CC}=1.8V, f=10MHz$	24			pF
		$V_{CC}=2.5V, f=10MHz$	24			pF
		$V_{CC}=3.3V, f=10MHz$	26			pF

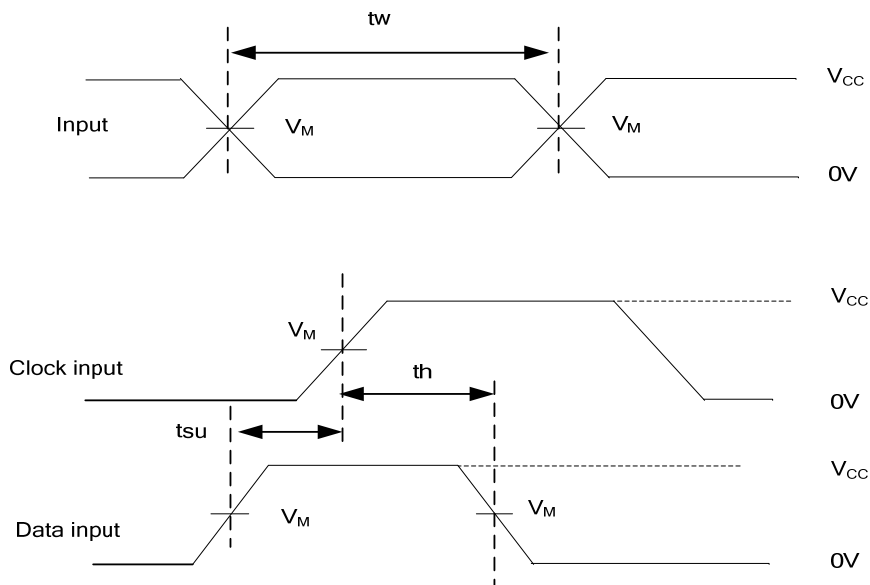
■ TEST CIRCUIT AND WAVEFORMS



Note:  $C_L$  includes probe and jig capacitance.

**Fig. 1** Load circuitry for switching times.

$V_{CC}$	Inputs		$V_M$	$C_L$	$R_L$
	$V_{IN}$	$t_R, t_F$			
$1.8V \pm 0.15V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	30pF	1K $\Omega$
$2.5V \pm 0.2V$	$V_{CC}$	$\leq 2ns$	$V_{CC}/2$	30pF	500 $\Omega$
2.7V	2.7V	$\leq 2.5ns$	1.5V	50pF	500 $\Omega$
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	$V_{CC}/2$	50pF	500 $\Omega$



**Fig. 2** Propagation delay from input to output and input voltage waveforms.

■ TEST CIRCUIT AND WAVEFORMS (Cont.)

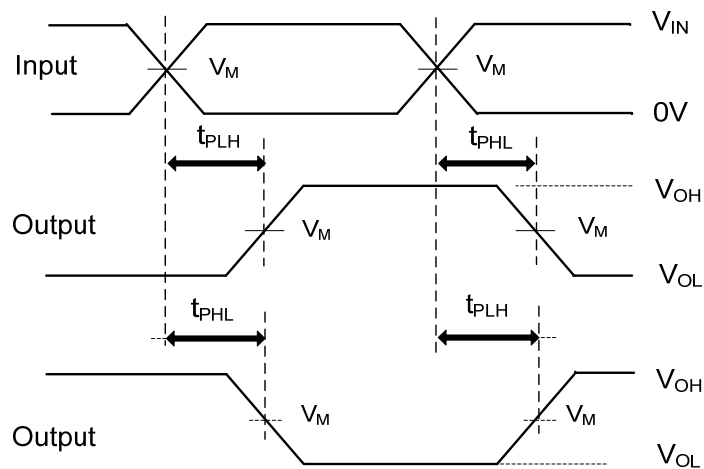


Fig. 3 PROPAGATION DELAY TIMES

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