

# $\mu$ A139/239/339 • $\mu$ A139A/239A/339A $\mu$ A2901 • $\mu$ A3302

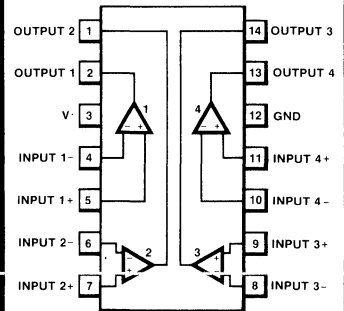
## LOW-POWER, LOW-OFFSET VOLTAGE QUAD COMPARATORS FAIRCHILD LINEAR INTEGRATED CIRCUITS

**GENERAL DESCRIPTION** — The  $\mu$ A139 series consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected PNP input stage allows the input common-mode voltage to include ground.

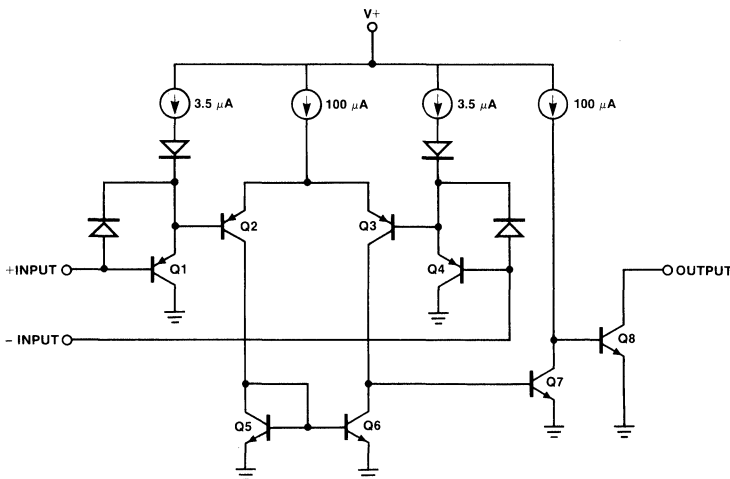
- SINGLE SUPPLY OPERATION — +2.0 V TO +36 V
- DUAL SUPPLY OPERATION —  $\pm 1.0$  V TO  $\pm 18$  V
- ALLOW COMPARISON OF VOLTAGES NEAR GROUND POTENTIAL
- LOW CURRENT DRAIN — 800  $\mu$ A TYP
- COMPATIBLE WITH ALL FORMS OF LOGIC
- LOW INPUT BIAS CURRENT — 25 nA TYP
- LOW INPUT OFFSET CURRENT —  $\pm 5$  nA TYP
- LOW OFFSET VOLTAGE —  $\pm 2$  mV

### CONNECTION DIAGRAM 14-PIN DIP

PACKAGE OUTLINES 6A 9A  
PACKAGE CODES D P



### SCHEMATIC DIAGRAM



### ORDER INFORMATION

TYPE	PART NO.
$\mu$ A139A	$\mu$ A139ADM
$\mu$ A139	$\mu$ A139DM
$\mu$ A239A	$\mu$ A239ADC
$\mu$ A239A	$\mu$ A239APC
$\mu$ A239	$\mu$ A239DC
$\mu$ A239	$\mu$ A239PC
$\mu$ A339A	$\mu$ A339ADC
$\mu$ A339A	$\mu$ A339APC
$\mu$ A339	$\mu$ A339DC
$\mu$ A339	$\mu$ A339PC
$\mu$ A2901	$\mu$ A2901DC
$\mu$ A2901	$\mu$ A2901PC
$\mu$ A3302	$\mu$ A3302DC
$\mu$ A3302	$\mu$ A3302PC

**ELECTRICAL CHARACTERISTICS** ( $V^+ = 5\text{ V}$ , Note 4)

CHARACTERISTICS	CONDITIONS	$\mu\text{A}139\text{A}$			$\mu\text{A}239\text{A}, \mu\text{A}339\text{A}$			$\mu\text{A}139$			$\mu\text{A}239, \mu\text{A}339$			$\mu\text{A}2901$			$\mu\text{A}3302$			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage	$T_A = 25^\circ\text{C}$ , (Note 9)		$\pm 1.0$	$\pm 2.0$		$\pm 1.0$	$\pm 2.0$		$\pm 2.0$	$\pm 5.0$		$\pm 2.0$	$\pm 5.0$		$\pm 2.0$	$\pm 7.0$		$\pm 3.0$	$\pm 20$	mV	
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = 25^\circ\text{C}$ , (Note 5)		25	100		25	250		25	100		25	250		25	250		25	500	nA	
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$ , $T_A = 25^\circ\text{C}$		$\pm 5.0$	$\pm 25$		$\pm 5.0$	$\pm 50$		$\pm 5.0$	$\pm 25$		$\pm 5.0$	$\pm 50$		$\pm 5.0$	$\pm 50$		$\pm 5.0$	$\pm 100$	nA	
Input Common-Mode Voltage Range	$T_A = 25^\circ\text{C}$ , (Note 6)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V	
Supply Current	$R_L = \infty$ on all Comparators, $T_A = 25^\circ\text{C}$ $R_L = \infty$ , $V^+ = 30\text{ V}$ , $T_A = 25^\circ\text{C}$		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	1.0 2.5		0.8	2.0	mA	
Voltage Gain	$R_L \geq 15\text{ k}\Omega$ , $V^+ = 15\text{ V}$ (To Support Large $V_O$ Swing), $T_A = 25^\circ\text{C}$	50	200		50	200		200			200		200		25	100		2	30	V/mV	
Large Signal Response Time	$V_{IN}$ = TTL Logic Swing, $V_{ref} = 1.4\text{ V}$ , $V_{RL} = 5.0\text{ V}$ , $R_L = 5.1\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$		300			300		300			300			300					300		ns
Response Time	$V_{RL} = 5.0\text{ V}$ , $R_L = 5.1\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$ , (Note 7)		1.3			1.3		1.3			1.3			1.3					1.3		$\mu\text{s}$
Output Sink Current	$V_{IN(-)} \geq 1.0\text{ V}$ , $V_{IN(+)} = 0$ , $V_O \leq 1.5\text{ V}$ , $T_A = 25^\circ\text{C}$	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16			2.0	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1.0\text{ V}$ , $V_{IN(+)} = 0$ , $I_{sink} \leq 4.0\text{ mA}$ , $T_A = 25^\circ\text{C}$		250	400		250	400		250	400		250	400			400		250	500		mV
Output Leakage Current	$V_{IN(+)} \geq 1.0\text{ V}$ , $V_{IN(-)} = 0$ , $V_O = 30\text{ V}$ , $T_A = 25^\circ\text{C}$			200		200		200			200			200					200		nA
Input Offset Voltage	(Note 9)			4.0		4.0		9.0			9.0		9.0	9.0	15				40		mV
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			$\pm 100$		$\pm 150$		$\pm 100$			$\pm 150$		50	200					300		nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300		400		300			400		200	500					1000		nA
Input Common-Mode Voltage Range		0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$		V
Saturation Voltage	$V_{IN(-)} \geq 1.0\text{ V}$ , $V_{IN(+)} = 0$ , $I_{sink} \leq 4\text{ mA}$			700		700		700			700		400	700					700		mV
Output Leakage Current	$V_{IN(+)} \geq 1.0\text{ V}$ , $V_{IN(-)} = 0$ , $V_O = 30\text{ V}$			1.0		1.0		1.0			1.0			1.0					1.0		$\mu\text{A}$
Differential Input Voltage	Keep all $V_{IN}$ 's $\geq 0\text{ V}$ (or $V^-$ , if used), (Note 8)			$V^+$		$V^+$		36			36	0		$V^+$					$V_{CC}$		V

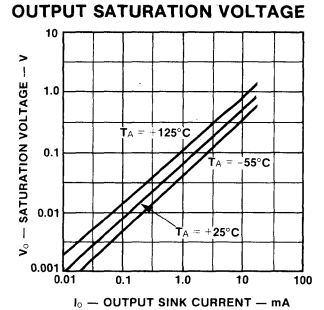
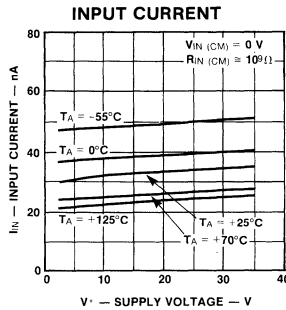
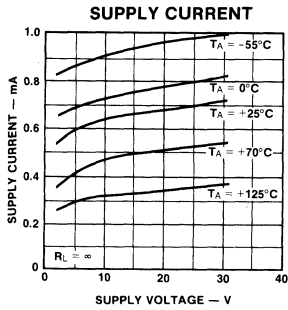
**ABSOLUTE MAXIMUM RATINGS**

	$\mu$ A139/ $\mu$ A239/ $\mu$ A339 $\mu$ A139A/ $\mu$ A239A/ $\mu$ A339A $\mu$ A2901	$\mu$ A3302
Supply Voltage, $V^+$	36 V or $\pm 18$ V	28 V or $\pm 14$ V
Differential Input Voltage	36 V	28 V
Input Voltage Range	-0.3 V to +36 V	-0.3 V to +28 V
Power Dissipation (Note 1)		
9A, 6A	1 W	1 W
Output Short-Circuit to Gnd, (Note 2)	Continuous	Continuous
Input Current ( $V_{IN} < -0.3$ V), (Note 3)	50 mA	50 mA
Operating Temperature Range		
$\mu$ A339, $\mu$ A339A	0° C to +70° C	
$\mu$ A239, $\mu$ A239A	-25° C to +85° C	
$\mu$ A139, $\mu$ A139A	-55° C to +125° C	
$\mu$ A2901, $\mu$ A3302	-40° C to +85° C	
Storage Temperature Range	-65° C to +150° C	-65° C to +150° C
Pin Temperature (Soldering, 10 s)	300° C	300° C

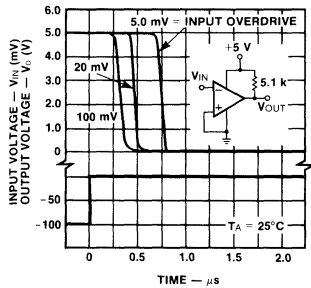
**NOTES:**

- For operating at high temperatures, the  $\mu$ A339/ $\mu$ A339A,  $\mu$ A2901  $\mu$ A3302 must be derated based on a 125° C maximum junction temperature and a thermal resistance of 125° C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The  $\mu$ A139 and  $\mu$ A139A must be derated based on a 150° C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ( $I_{PD} \leq 100$  mW), provided the output transistors are allowed to saturate.
- Short circuits from the output to  $V^+$  can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of  $V^+$ .
- This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the  $V^+$  voltage level or to ground for a large overdrive for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which negative, again returns to a value greater than -0.3 V.
- These specifications apply for  $V^+ = 5.0$  V and  $-55^\circ \text{C} \leq T_A \leq +125^\circ \text{C}$ , unless otherwise stated. With the  $\mu$ A239/ $\mu$ A239A, all temperature specifications are limited to  $-25^\circ \text{C} \leq T_A \leq +85^\circ \text{C}$ , the  $\mu$ A339/ $\mu$ A339A temperature specifications are limited to  $0^\circ \text{C} \leq T_A \leq +70^\circ \text{C}$ , and the  $\mu$ A2901,  $\mu$ A3302 temperature range is  $-40^\circ \text{C} \leq T_A \leq +85^\circ \text{C}$ .
- The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is  $V^+ - 1.5$  V, but either or both inputs can go to +30 V without damage.
- The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained; see typical performance characteristics section.
- Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V or 0.3 V below the magnitude of the negative power supply, if used.
- At output switch point,  $V_O \approx 1.4$  V,  $R_S = 0\Omega$  with  $V^+$  from 5 V; and over the full input common-mode range (0 V to  $V^+ - 1.5$  V).
- For input signals that exceed  $V_{CC}$ , only the overdriven comparator is affected. With a 5 V supply,  $V_{IN}$  should be limited to 25 V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

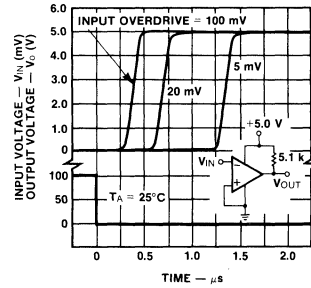
TYPICAL PERFORMANCE CHARACTERISTICS  
 $\mu$ A139/ $\mu$ A239/ $\mu$ A339,  $\mu$ A139A/ $\mu$ A239A/ $\mu$ A339A,  $\mu$ A3302



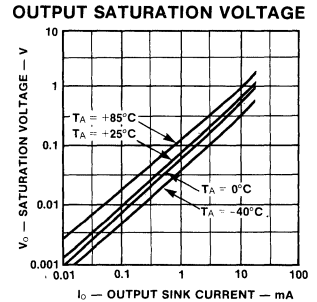
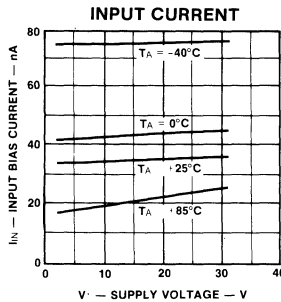
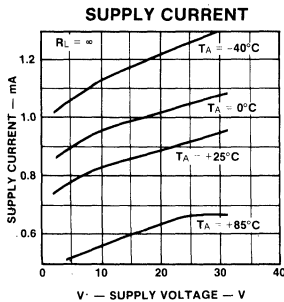
**RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION**



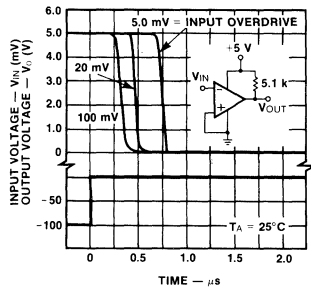
**RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION**



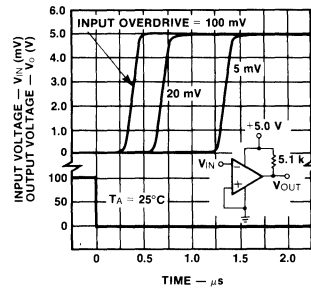
TYPICAL PERFORMANCE CHARACTERISTICS  $\mu$ A2901



**RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION**



**RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION**



**APPLICATION HINTS**

The  $\mu$ A139 series are high-gain, wide-bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to  $< 10\text{ k}\Omega$  reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

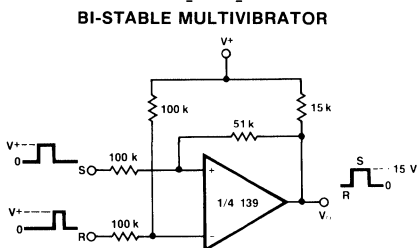
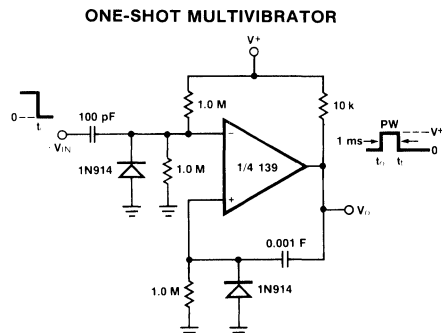
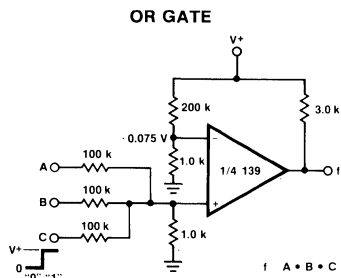
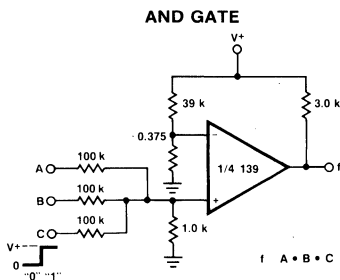
The bias network of the  $\mu$ A139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V to 30 V.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than  $V^+$  without damaging the device. Protection should be provided to prevent the input voltages from going negative more than  $-0.3\text{ V}$  (at  $25^\circ\text{C}$ ). An input clamp diode can be used as shown in the applications section.

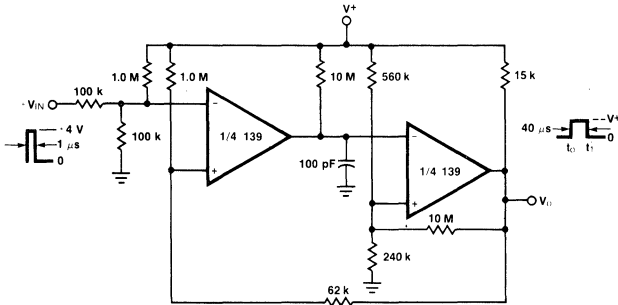
The output of the  $\mu$ A139 series is the uncommitted collector of a grounded-emitter npn output transistor. Many collectors can be tied together to provide an output ORing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the  $V^+$  terminal of the  $\mu$ A139 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of  $V^+$ ) and the  $\beta$  of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately  $60\ \Omega$  saturation resistance of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

**TYPICAL APPLICATIONS ( $V^+ = 15\text{ V}$ )**

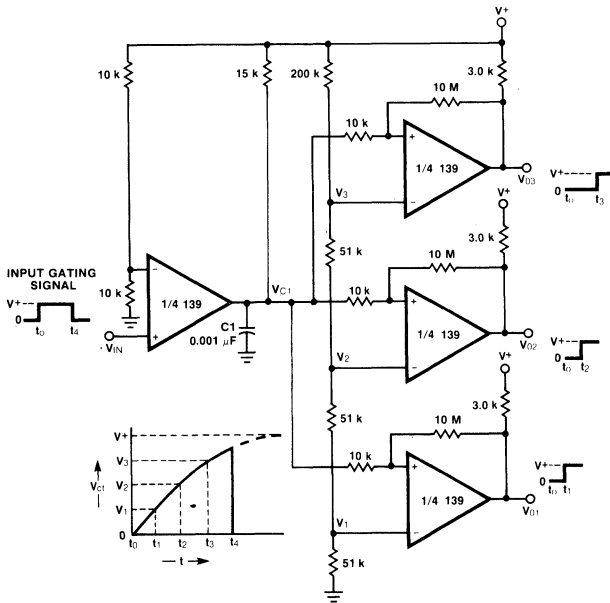


TYPICAL APPLICATIONS ( $V^+ = 15\text{ V}$ ) (Cont.)

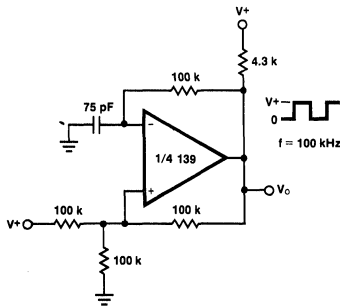
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT



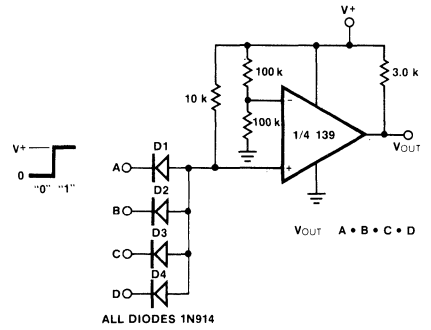
TIME DELAY GENERATOR



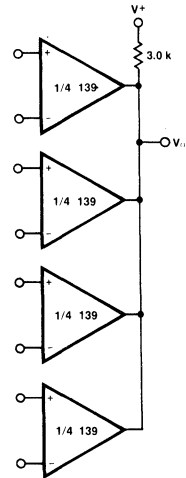
SQUAREWAVE OSCILLATOR



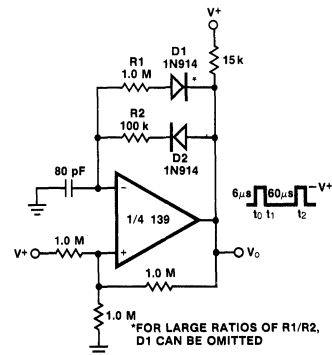
LARGE FAN-IN AND GATE



ORING THE OUTPUTS

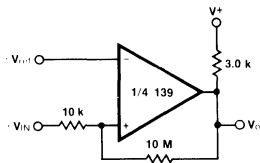


PULSE GENERATOR

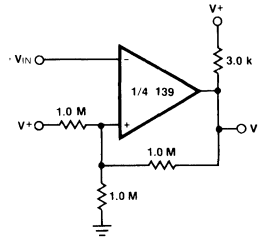


TYPICAL APPLICATIONS ( $V^+ = 15\text{ V}$ ) (Cont.)

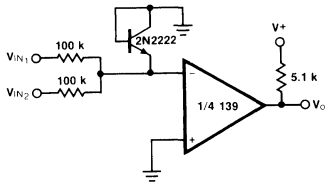
NON-INVERTING COMPARATOR WITH HYSTERESIS



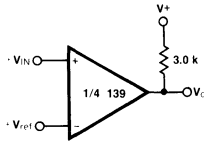
INVERTING COMPARATOR WITH HYSTERESIS



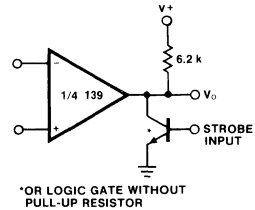
COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY



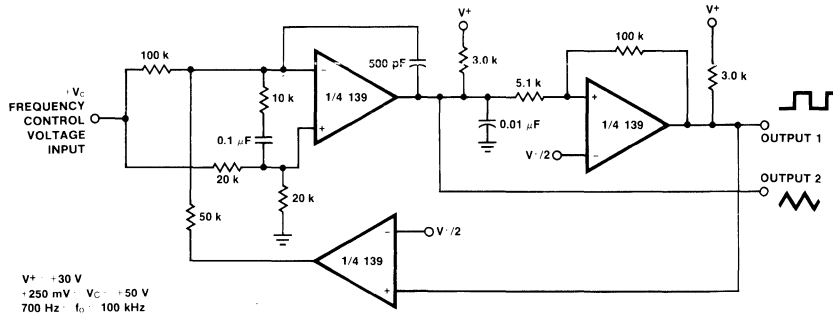
BASIC COMPARATOR



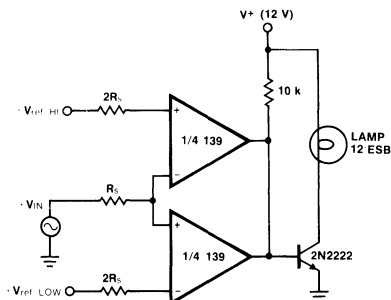
OUTPUT STROBING



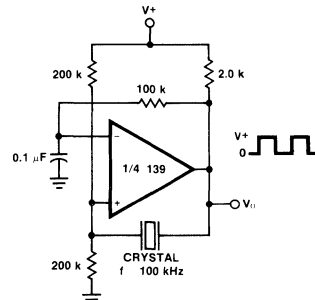
TWO-DECADE HIGH-FREQUENCY VCO



LIMIT COMPARATOR

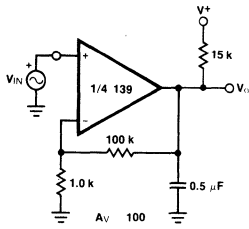


CRYSTAL CONTROLLED OSCILLATOR

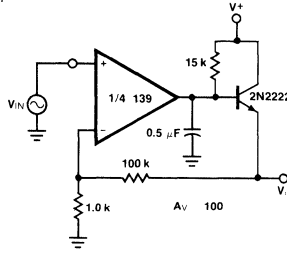


TYPICAL APPLICATIONS ( $V^+ = 15$  V) (Cont.)

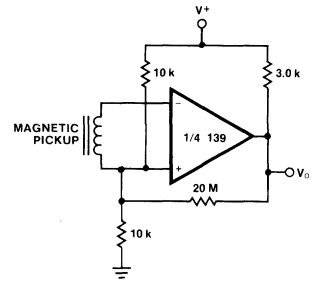
LOW FREQUENCY OP AMP



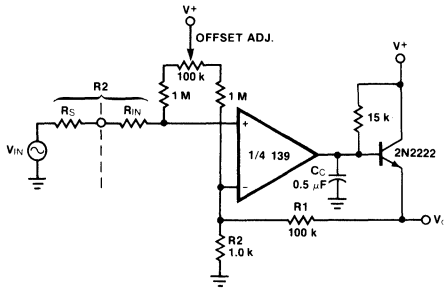
LOW FREQUENCY OP AMP  
( $V_O = 0$  V FOR  $V_{IN} = 0$  V)



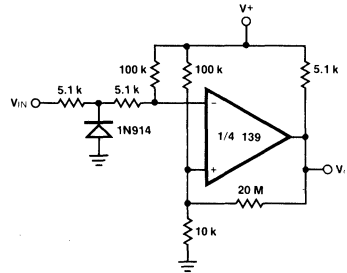
TRANSDUCER AMPLIFIER



LOW FREQUENCY OP AMP WITH OFFSET ADJUST

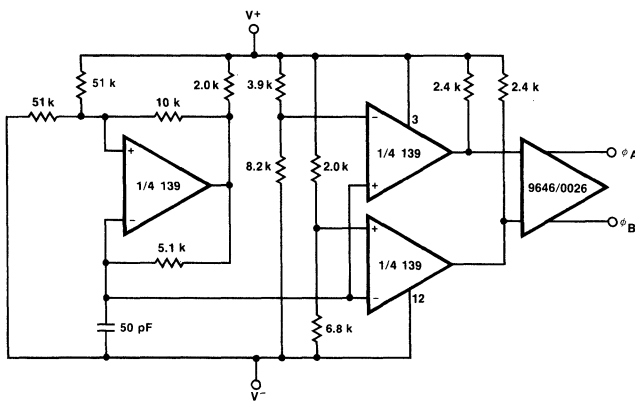


ZERO CROSSING DETECTOR (SINGLE POWER SUPPLY)

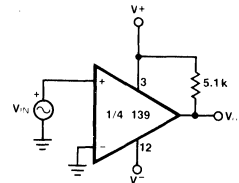


SPLIT-SUPPLY APPLICATIONS  $V^+ = +15$  V and  $V^- = -15$  V

MOS CLOCK DRIVER



ZERO CROSSING DETECTOR



COMPARATOR WITH A NEGATIVE REFERENCE

