μA3301 • μA3401

QUAD SINGLE-SUPPLY AMPLIFIERS

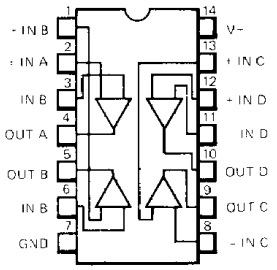
FAIRCHILD INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA3301/μA3401 are monolithic Quad Amplifiers consisting of four independent, dual input, internally compensated amplifiers. They are constructed using the Fairchild Planar* epitaxial process. They were designed specifically to operate from a single power supply voltage and to provide a large output voltage swing. The non-inverting input function is achieved by using a current mirror. Applications for the μA3301/μA3401 are ac amplifiers, FC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

- **SINGLE SUPPLY OPERATION – +4.0 Vdc to +28 Vdc**
- **INTERNALLY COMPENSATED**
- **WIDE UNITY GAIN BANDWIDTH – 5.0 MHz**
- **LOW INPUT BIAS CURRENT – 50 nA TYPICAL**
- **HIGH OPEN LOOP GAIN – 1000 V/V MINIMUM**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 9A
PACKAGE CODE P



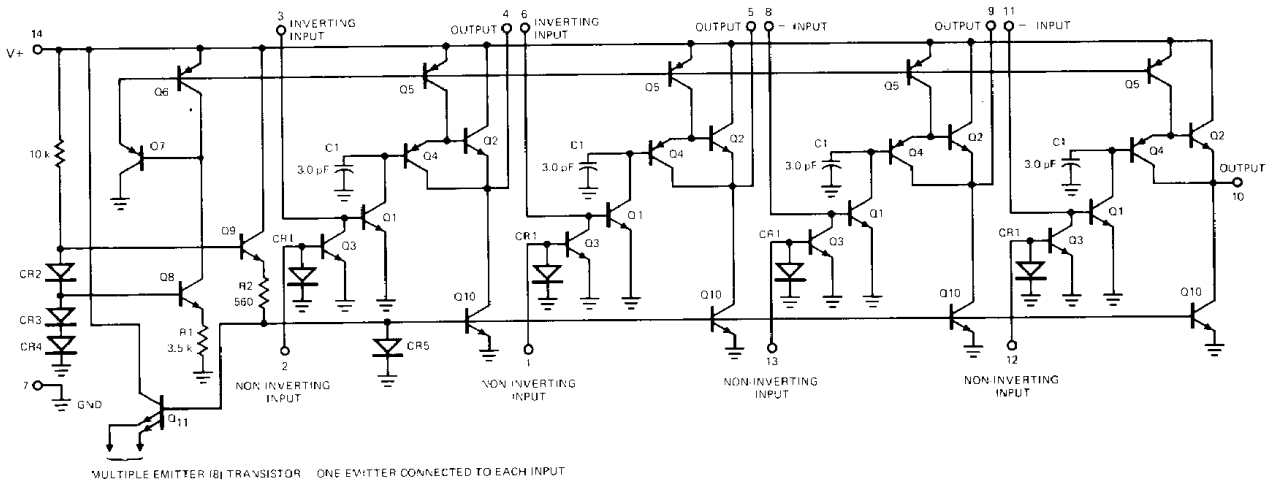
ORDER INFORMATION

TYPE	PART NO.
μA3301	μA3301PC
μA3401	μA3401PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA3301	+28 V
μA3401	+18 V
Non-Inverting Input Current	5.0 mA
Sink Current	50 mA
Source Current	50 mA
Internal Power Dissipation (Note 1)	670 mW
Operating Temperature Range	
μA3301	−40°C to +85°C
μA3401	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA3301

ELECTRICAL CHARACTERISTICS: V_S = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C, each amplifier, unless otherwise noted.

CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Open Loop Voltage Gain (Note 2)	Inverting Input	1000	2000		V/V
Input Bias Current (Note 3)	R_L = ∞, Inverting Input		50	300	nA
Input Resistance		0.1	1.0		MΩ
Current Mirror Gain (Note 4)	(I_{Mirror} = 200 μAdc)	0.80	0.98	1.16	A/A
Output Current					
Source	V_{OH} = 0.4 Vdc	3.0	10		mA
	V_{OH} = 9.0 Vdc		7.0		mA
Sink (Note 5)	V_{OL} = 0.4 Vdc	0.5	0.87		mA
Output Voltage (Note 6)					
HIGH		13.5	14.2		V
LOW			0.03	0.1	V
Slew Rate	C_L = 100 pF, R_L = 5.0 kΩ		0.6		V/μs
Unity Gain Bandwidth (Note 7)			5.0		MHz
Phase Margin (Note 7)			70		Degrees
Quiescent Power Supply Current (Note 8)					
Non-Inverting Inputs Open	Total for Four Amplifiers		6.9	10	mA
Non-Inverting Inputs Grounded	Total for Four Amplifiers		7.8	14	mA
Power Supply Rejection (Note 9)	(f = 100 Hz)		75		dB
Channel Separation	(f = 1.0 kHz)		85		dB
The following specifications apply for −40°C ≤ T_A ≤ +85°C.					
Open Loop Voltage Gain (R_L = 10 kΩ)	Inverting Input		1600		V/V
Input Bias Current	R_L = ∞			500	nA
Output Voltage (Note 10) Undistorted Output Swing		10	13.5		V_{pk-pk}

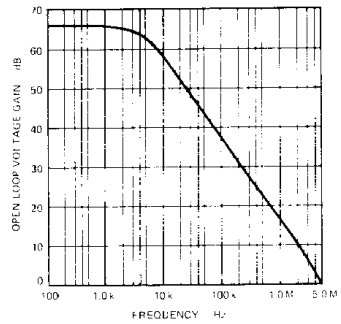
μA3401

ELECTRICAL CHARACTERISTICS: V_S = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C, each amplifier, unless otherwise noted.

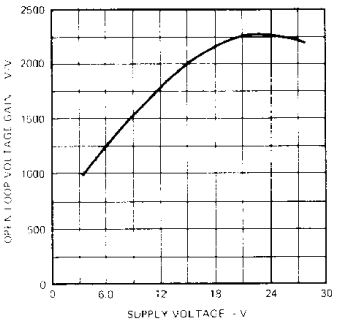
CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
Open Loop Voltage Gain (Note 2)	Inverting Input	1000	2000		V/V
Input Bias Current (Note 3)	R_L = ∞, Inverting Input		50	300	nA
Input Resistance		0.1	1.0		MΩ
Output Current					
Source		5.0	10		mA
Sink (Note 5)		0.5	1.0		mA
Output Voltage (Note 6)					
HIGH		13.5	14.2		V
LOW			0.03	0.1	V
Slew Rate	C_L = 100 pF, R_L = 5.0 kΩ		0.6		V/μs
Unity Gain Bandwidth (Note 7)			5.0		MHz
Phase Margin (Note 7)			70		Degrees
Quiescent Power Supply Current (Note 8)					
Non-Inverting Inputs Open	Total for Four Amplifiers		6.9	10	mA
Non-Inverting Inputs Grounded	Total for Four Amplifiers		7.8	14	mA
Power Supply Rejection (Note 9)	(f = 100 Hz)		75		dB
Channel Separation	(f = 1.0 kHz)		85		dB
The following specifications apply for 0°C ≤ T_A ≤ 70°C.					
Open Loop Voltage Gain (R_L = 10 kΩ)	Inverting Input	800			V/V
Input Bias Current	R_L = ∞			500	nA
Output Voltage (Note 10) Undistorted Output Swing		10	13.5		V_{pk-pk}

TYPICAL PERFORMANCE CURVES

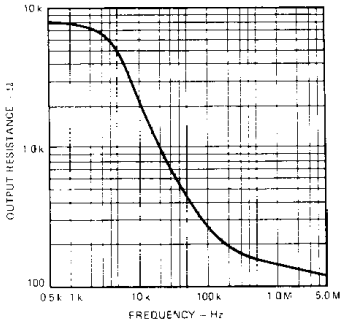
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



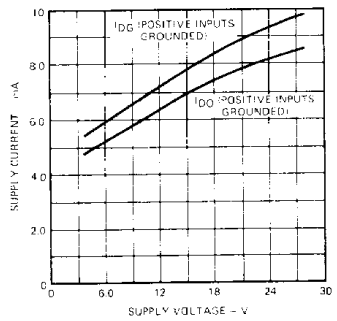
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



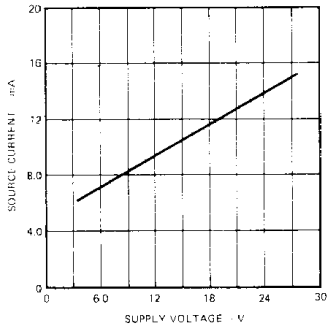
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



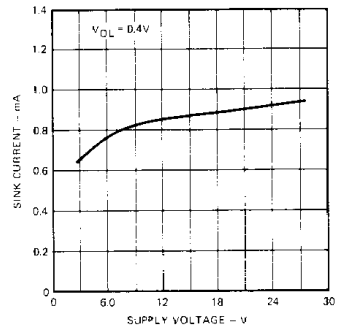
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



LINEAR SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



LINEAR SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



NOTES:

1. Rating applies to T_A up to 70°C. Above T_A = 70°C, derate linearly at 8.3 mW/°C.
2. Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
3. Input bias current can be defined only for the inverting input. The non-inverting input is not a true "differential input" — as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
4. Current mirror gain is defined as the current demanded at the inverting input divided by the current into the non-inverting input.
5. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
6. When used as a non-inverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
7. Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.
8. The quiescent current will increase approximately 0.3 mA for each non-inverting input which is grounded. Leaving the non-inverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
9. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.
10. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration as shown in the peak-to-peak output voltage test circuit.

TEST CIRCUITS

SMALL SIGNAL TRANSIENT RESPONSE

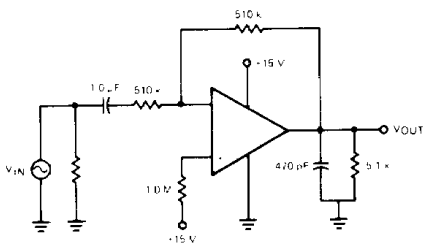
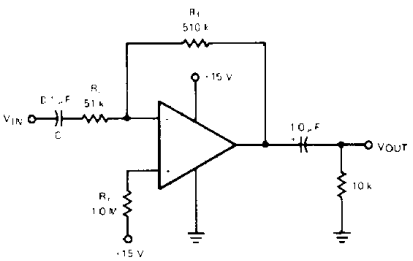


Fig. 1

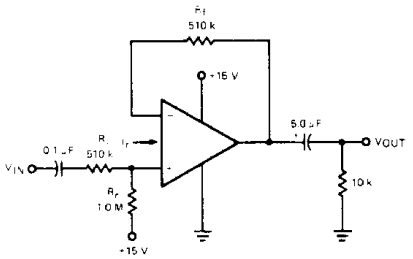
INVERTING AMPLIFIER



$$A_V = -\frac{R_f}{R_i} \text{ for } \frac{1}{\omega C} \ll R_i$$

Fig. 2

NON-INVERTING AMPLIFIER

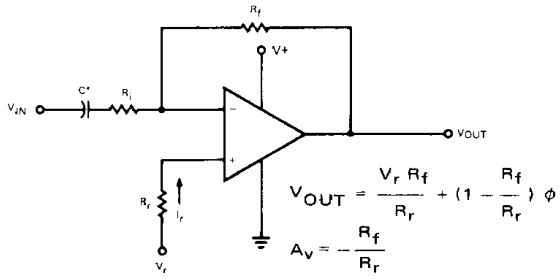


$$A_V = \frac{R_f}{R_i + \frac{26}{I_F \text{ (mA)}}} \simeq 1 \qquad \text{BW} = 250 \text{ kHz}$$

Fig. 3

TEST CIRCUITS (Cont'd)

INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



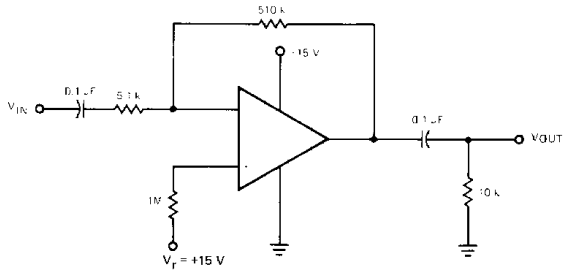
$$V_{OUT} = \frac{V_r R_f}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

$$A_v = -\frac{R_f}{R_r}$$

*Select for low frequency response.

Fig. 4

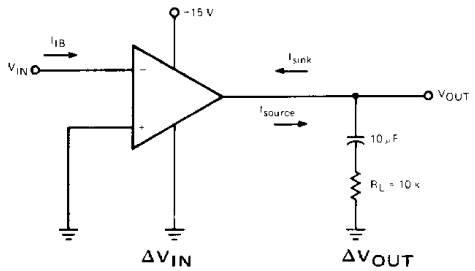
INVERTING AMPLIFIER WITH $A_v = 100$ AND $V_r = V+$



$A_v = 100$ $f_L = 300$ Hz, $f_H = 50$ kHz

Fig. 5

OPEN LOOP GAIN AND INPUT RESISTANCE (INPUT BIAS CURRENT, OUTPUT CURRENT)

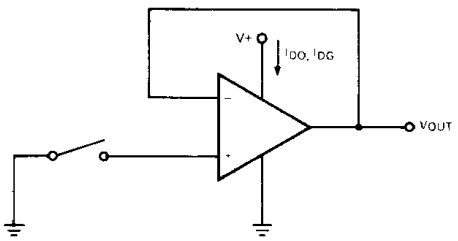


$$R_{in} = \frac{\Delta V_{IN}}{\Delta I_{IB}} \qquad A_{vol} = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

Amplifier must be biased by V_{IN} in the linear operating region

Fig. 6

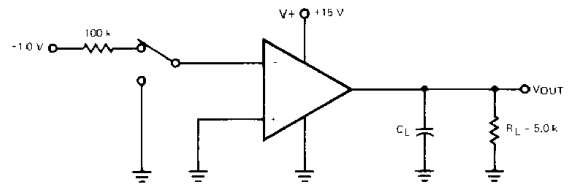
QUIESCENT POWER SUPPLY CURRENT



I_{DO} is total supply current with noninverting input open.
I_{DG} is total supply current with noninverting input grounded.

Fig. 7

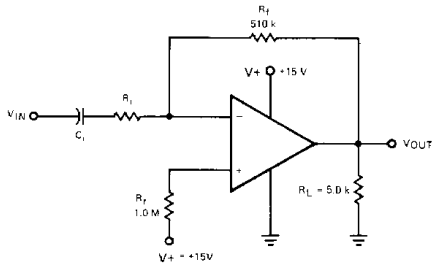
OUTPUT VOLTAGE SWING



V_{OL} measured with inverting input biased as shown.
V_{OH} measured with inverting input grounded.

Fig. 8

PEAK-TO-PEAK OUTPUT VOLTAGE



$$V_{OUT} \simeq V+ \frac{R_f}{R_r} \simeq \frac{V+}{2} \text{ for } R_r \simeq 2\,R_f$$

Fig. 9

NORMAL DESIGN PROCEDURE

Output Q-Point Biasing

A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the non-inverting input to effect the biasing as shown in Figures 2 and 3. The high impedance of the collector of the non-inverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the non-inverting input current be in the 5.0 μA to 100 μA range.

V+ Reference Voltage (Figures 2 and 3)

The non-inverting input is normally returned to the V+ voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 5.0 μA to 100 μA. Choosing the feedback resistor, R_f, to be equal to 1/2 R_r will now bias the amplifier output dc level to approximately:

$$\frac{V+}{2}$$

This allows for maximum dynamic range of the output voltage.

Reference Voltage Other Than V+ (Figure 4)

The biasing resistor R_r may be returned to a voltage (V_r) other than V+. By setting $R_f = R_r$, (still keeping I_r between 5.0 μA and 100 μA) the output dc level will be equal to V_r. Neglecting error terms, the expression for determining V_{Odc} is:

$$V_{OUT} = \frac{(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.7 V @ +25°C).

The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5.0 μA to 100 μA.

Gain Determination — Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_v = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 5.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

Non-Inverting Amplifier

Although recommended as an inverting amplifier, the 3301/3401 may be used in the non-inverting mode (Figure 3). The amplifier gain in this configuration is subject to the same error terms that affects the output Q point biasing so the gain may deviate as much as ±20 % from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately:

$$\frac{26}{I_r}\ \Omega,$$

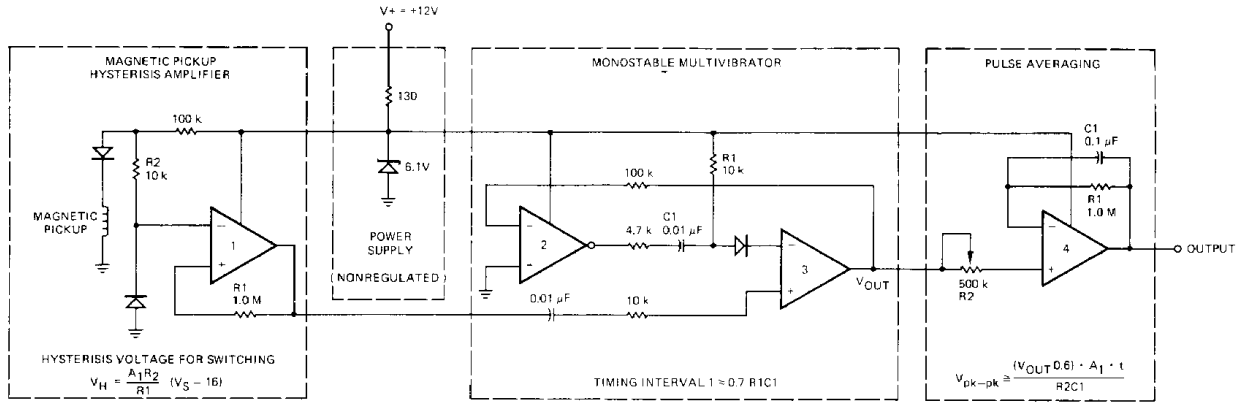
where I_r is input current in mA. The non-inverting gain expression is given by:

$$A_v = \frac{R_f}{R_i + \frac{26}{I_r\ (mA)}} \pm 20\%.$$

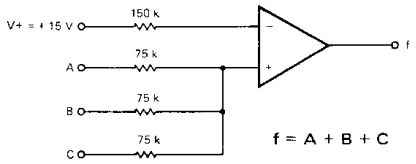
The bandwidth of the non-inverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for non-inverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

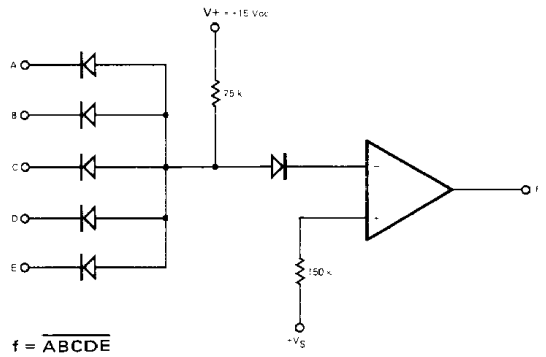
TACHOMETER CIRCUIT



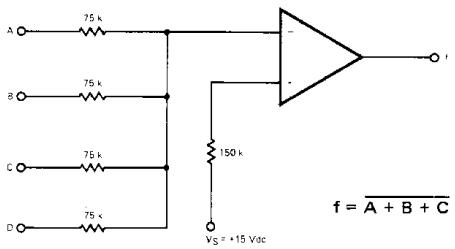
LOGIC OR GATE



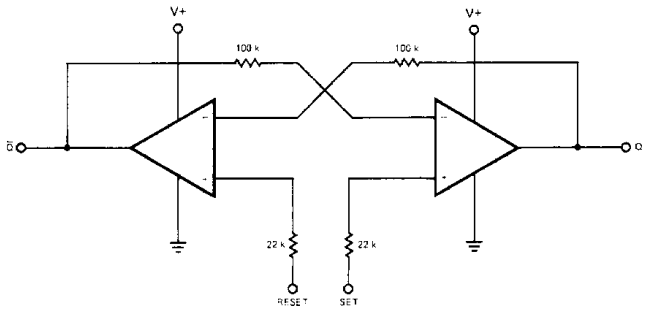
LOGIC NAND GATE (Large Fan In)



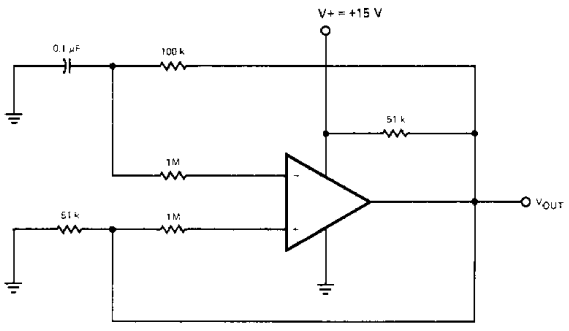
LOGIC NOR GATE



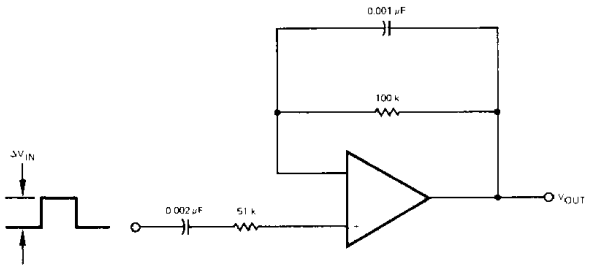
R-S FLIP-FLOP



STABLE MULTIVIBRATOR

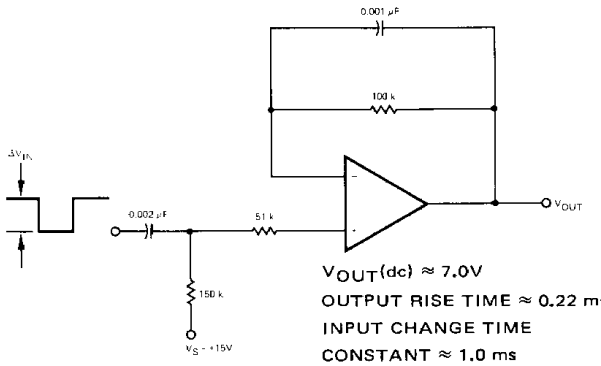


POSITIVE EDGE DIFFERENTIATOR



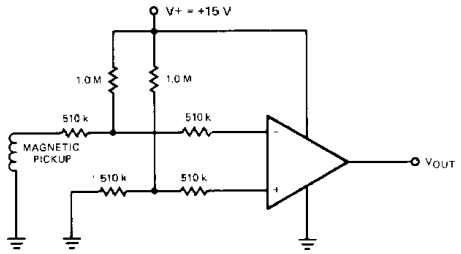
OUTPUT RISE TIME ≈ 0.22 ms
INPUT CHANGE TIME CONSTANT ≈ 1.0 ms

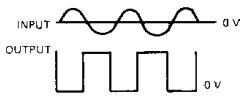
NEGATIVE EDGE DIFFERENTIATOR



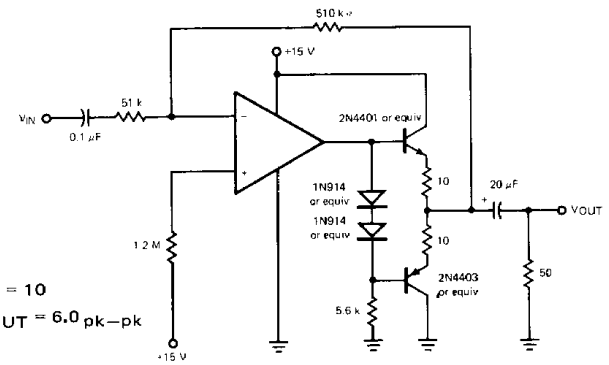
V_{OUT}(dc) ≈ 7.0V
OUTPUT RISE TIME ≈ 0.22 ms
INPUT CHANGE TIME CONSTANT ≈ 1.0 ms

ZERO CROSSING DETECTOR



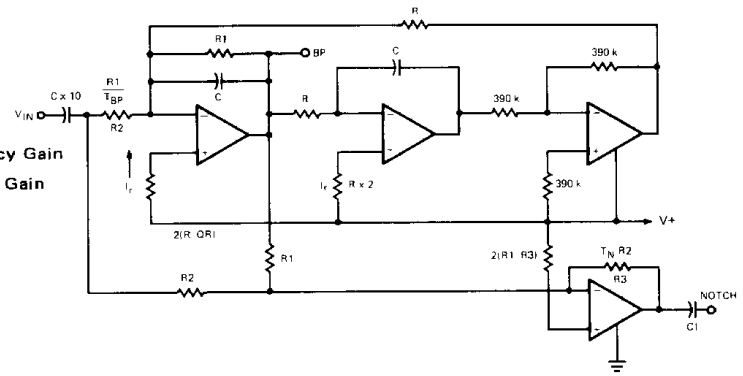


AMPLIFIER AND DRIVER FOR 50 Ω LINE



$A_V = 10$
$V_{OUT} = 6.0\ pk\text{–}pk$

BASIC BANDPASS AND NOTCH FILTER



T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain
$\omega 0 = \frac{1}{RC}$
$R1 = QR$
$R2 = \frac{R1}{T_{BP}}$
$R3 = T_N R2$