FAIRCHILD
A Schlumberger Company

μA9638
RS-422 Dual High Speed Differential Line Driver

Linear Division Interface Products

Description

The μA9638 is a Schottky, TTL compatible, dual differential line driver designed specifically to meet the EIA Standard RS-422 specifications. It is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down. The device features a short circuit protected active pull-up with low output impedance and is specified to drive 50 Ω transmission lines at high speed. The mini-DIP provides high package density.

- **Single 5.0 V Supply**
- **Schottky Technology**
- **TTL And CMOS Compatible Inputs**
- **Output Short Circuit Protection**
- **Input Clamp Diodes**
- **Complementary Outputs**
- **Minimum Output Skew (< 1.0 ns Typical)**
- **50 mA Output Drive Capability For 50 Ω Transmission Lines**
- **Meets EIA RS-422 Specifications**
- **Propagation Delay Of Less Than 10 ns**
- **"Glitchless" Differential Output**
- **Delay Time Stable With V_{CC} And Temperature Variations (< 2.0 ns Typical) (Figure 3)**
- **Extended Temperature Range**

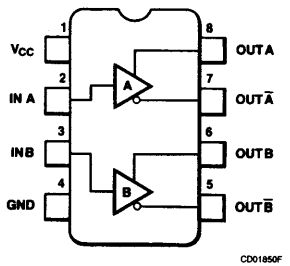
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	
Extended (μA9638M)	−55°C to +125°C
Commercial (μA9638C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO Package (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
V_{CC} Lead Potential to Ground	−5.0 V to +7.0 V
Input Voltage	−0.5 V to +7.0 V

Notes

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, 150°C for the Molded DIP and SO-8.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C; the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.

Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



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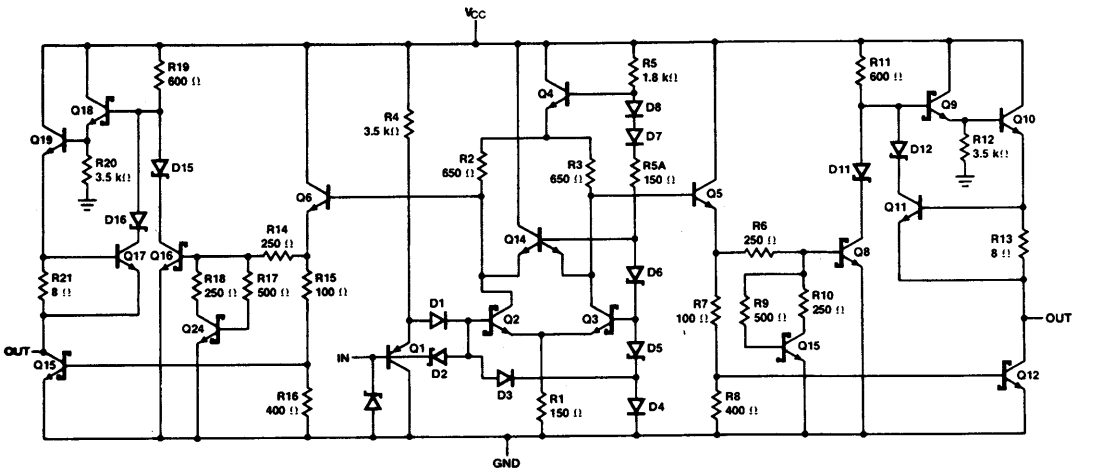
Order Information

Device Code	Package Code	Package Description
μA9638RM	6T	Ceramic DIP
μA9638RC	6T	Ceramic DIP
μA9638TC	9T	Molded DIP
μA9638SC	KC	Molded Surface Mount

Equivalent Circuit



↑ Input

Recommended Operating Conditions

Symbol	Characteristic	μA9638			μA9638C			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
I_{OH}	Output Current HIGH			−50			−50	mA
I_{OL}	Output Current LOW			50			50	mA
T_A	Operating Temperature	−55	25	125	0	25	70	°C

μA9638

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition[1]	Min	Typ[2]	Max	Unit
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW	Commercial			0.8	V
		Extended			0.5	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA		−1.0	−1.2	V
V_{OH}	Output Voltage HIGH	V_{CC} = Min, V_{IH} = $V_{IH\ Min}$, V_{IL} = $V_{IL\ Max}$, I_{OH} = −10 mA	2.5	3.5		V
		I_{OH} = −40 mA	2.0			
V_{OL}	Output Voltage LOW	V_{CC} = Min, V_{IH} = $V_{IH\ Min}$, V_{IL} = $V_{IL\ Max}$, I_{OL} = 40 mA			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, $V_{I\ Max}$ = 5.5 V			50	μA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_{IH} = 2.7 V			25	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_{IL} = 0.5 V			−200	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0 V	−50		−150	mA
V_T, $\overline{V}_T$	Terminated Output Voltage	See *Figure 1*	2.0			V
$V_T - \overline{V}_T$	Output Balance				0.4	V
V_{OS}, $\overline{V}_{OS}$	Output Offset Voltage				3.0	V
$V_{OS} - \overline{V}_{OS}$	Output Offset Balance				0.4	V
I_X	Output Leakage Current	T_A = 25°C, −0.25 V < V_X < 6.0 V			100	μA
I_{CC}	Supply Current (both drivers)	V_{CC} = 5.5 V, All Input at 0 V, No Load		45	65	mA

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ[2]	Max	Unit
t_{PHL}	Propagation Delay	C_L = 15 pF, R_L = 100 Ω, See *Figure 2*		10	20	ns
t_{PLH}				10	20	ns
t_f	Fall Time, 90% − 10%			10	20	ns
t_r	Rise Time, 10% − 90%			10	20	ns
$t_{PO} - t_{\overline{PO}}$	Skew Between Outputs A/$\overline{A}$ and B/$\overline{B}$			1.0		ns

Notes

1. Use minimum and maximum values specified in recommended operating conditions.
2. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.

DC Test Circuit

Figure 1 Terminated Output Voltage and Output Balance

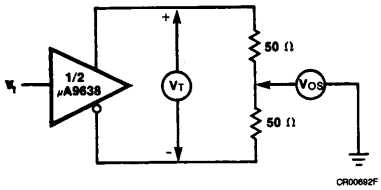
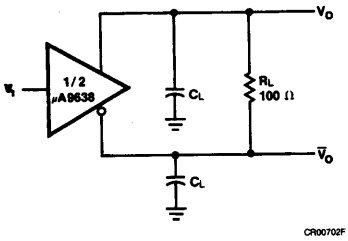
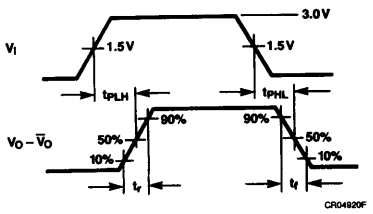


Figure 2 AC Test Circuit and Voltage Waveform





Notes
The pulse generator has the following characteristics:
PRR = 500 kHz t_W = 100 ns,
$t_r \leq 5.0$ ns, Z_O = 50 Ω.
C_L includes probe and jig capacitance

Figure 3 Typical Delay Characteristics