

HIGH-VOLTAGE ANALOG-SIGNAL IC

UC1676

4BPx80SEG Dot Matrix LCD Controller/Driver



MP Specifications
Datasheet Revision 1.1

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ULTRACHIP

The Coolest LCD Driver, Ever!!

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UC1676

4BPx80SEG Dot Matrix LCD Controller/Driver

INTRODUCTION

The UC1676 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four (4) backplanes and up to eighty (80) SEGs and can easily be cascaded for larger LCD applications. The UC1676 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-increment addressing, by hardware sub-addressing, and by display memory switching (static and duplex drive modes).

MAIN APPLICATIONS

- Battery operated hand held devices
- Portable Instruments

FEATURE HIGHLIGHTS

- Single-chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Selectable frame frequency: 64Hz, 82Hz, 110Hz, or 200Hz
400Hz is supported when using external Oscillator, (Max. 9.6KHz.)
- Internal LCD bias generation with voltage-follower buffers
- 80 SEG drives:

- Up to 40 7-SEG alphanumeric characters
- Up to 21 14-SEG alphanumeric characters
- Any graphics of up to 320 elements
- 80 x 4 bit RAM for display data storage
- Auto-incremental display data loading across device sub-address boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 2.5V to 5.5V
- Wide LCD supply range for low-threshold LCDs, guest-host LCDs, and high-threshold twisted nematic LCDs: from 2.5V to 11.0V
- Low power consumption
- 400 kHz I²C -bus interface
- Compatible with 4-bit, 8-bit, or 16-bit microprocessors or microcontrollers
- May be cascaded for large LCD applications (up to 5120 SEGs possible)
- No external components needed
- Compatible with Chip-On-Glass (COG) technology
- Manufactured using silicon gate CMOS process

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document.

ORDERING INFORMATION

Part Number	I ² C	Package	Description
UC1676cGAE	Yes	COG	Gold bumped die.

General Notes**APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I²C

The implementation of I²C is already included and tested in all silicon.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

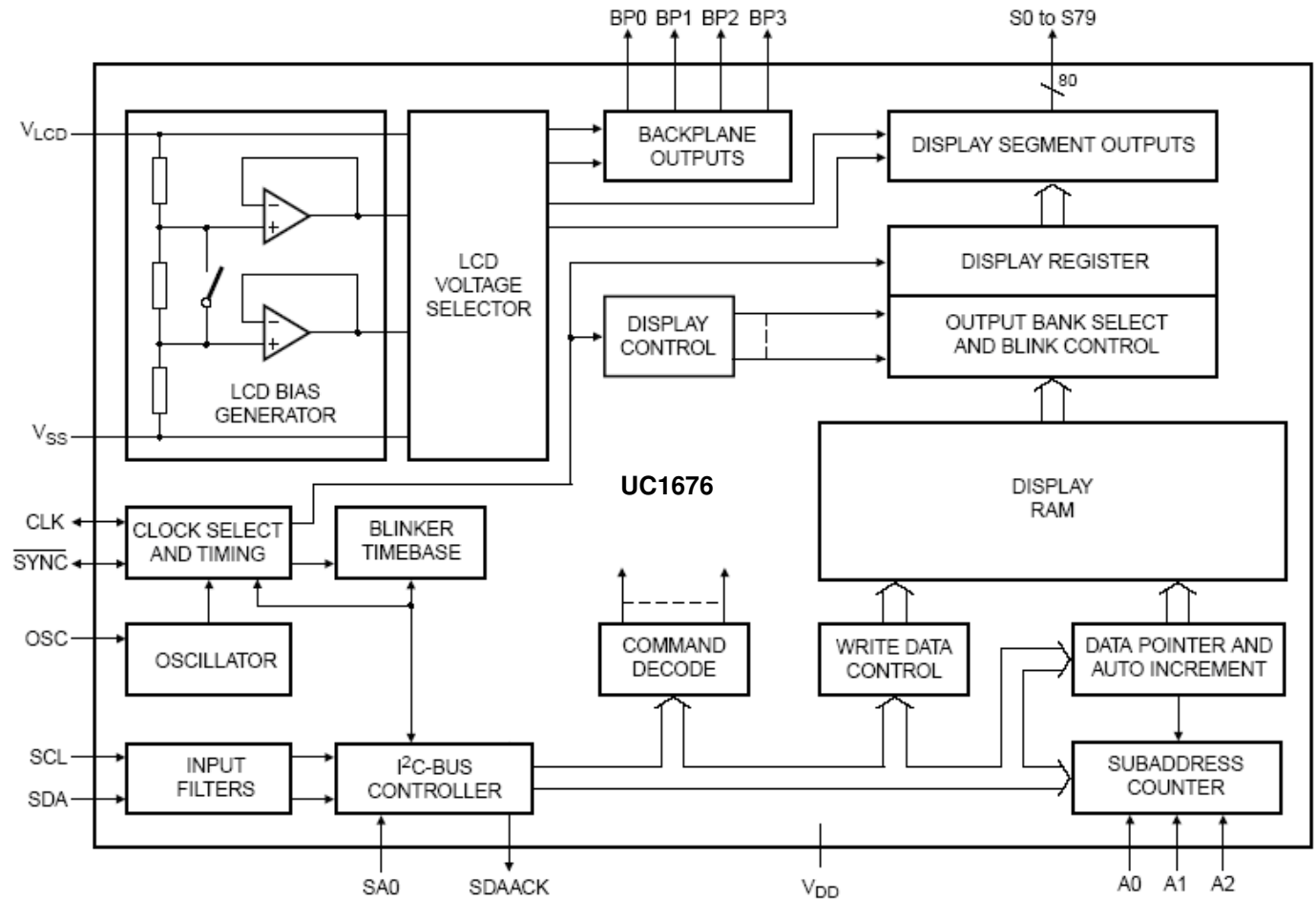
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BLOCK DIAGRAM



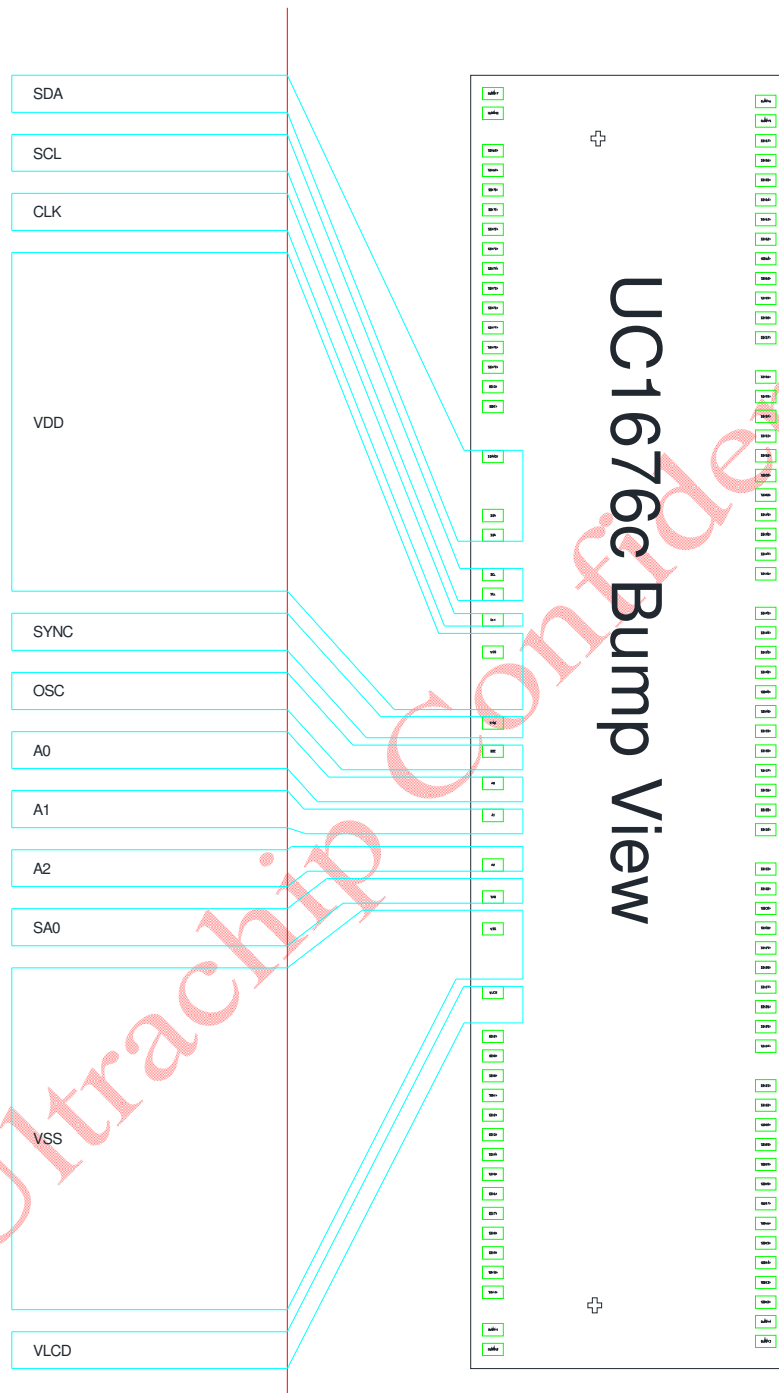
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PIN DESCRIPTION

Pin (Pad) Name	Pad No.	Type	Description
SDAACK	1	O	I ² C bus acknowledge output. Connect to SDA.
SDA	2~3	I	I ² C bus serial data input
SCL	4~5	I	I ² C bus serial clock input
CLK	6	I/O	Clock input and output When OSC pin is Low: Built-in oscillator is used, internal clock is output. Leave it open. When OSC pin is High: External clock is input.
V _{DD}	7	PWR	Supply voltage
$\overline{\text{SYNC}}$	8	I/O	Cascade synchronization input and output. Leave it open when cascade function is not used.
OSC	9	I	Oscillator select Low: Built-in oscillator is used. High: Built-in oscillator is stopped. External clock via the CLK pin is used.
A0, A1, A2	10~12	I	Hardware device address selection for cascading. Connect to V _{SS} for logic 0, V _{DD} for logic 1. Connect to V _{SS} when the cascade function is not used.
SA0	13	I	I ² C bus slave address selection Connect to V _{SS} for logic 0, V _{DD} for logic 1. When not used, connect to V _{SS} .
V _{SS}	14	PWR	Ground supply voltage
V _{LCD}	15	PWR	LCD supply voltage
BP2, BP0, BP3, BP1 (BO<2>, BO<0>, BO<3>, BO<1>)	16, 17, 98, 99	HV	LCD backplane output
S0~S79 (SO<0>~SO<79>)	18~97	HV	LCD SEG output
Dummy1~Dummy8	100~107	-	Dummy pins.

Note: The substrate (rear side of the die) is wired to V_{SS} but should not be electrically contracted.

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The operation condition, V_{DD}=2.5V (min.), should be satisfied under all operating conditions. UC1676c's peak current (I_{DD}) can be up to ~15mA during high speed data-write to UC1676c's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD} and V_{SS} ITO trances in COG modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop to below 2.5V and cause the IC to malfunction.

COMMAND TABLE

#	Command	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Mode-set	1	1	0	0	E	B	M1	M0	Set Display Mode	C0h
2	Load-data-pointer	0	DP6	DP5	DP4	DP3	DP2	DP1	DP0		00h
3	Frame-Rate-select	1	0	0	0	0	0	FR1	FR0	Select Frame Rate	80h
4	Device-select	1	1	1	0	0	A2	A1	A0	Select Device	E0h
5	Bank-select	1	1	1	1	1	0	I	O	Select Bank	F8h
6	Blink-select	1	1	1	1	0	A	BF1	BF0	Select Blink Mode	F0h

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COMMAND DESCRIPTION

(1) Mode-Set

Action	D7	D6	D5	D4	D3	D2	D1	D0
Set mode	1	1	0	0	E	B	M1	M0

E: Display status **0:** display disabled (blank) 1: display enabled

B: LCD bias configuration **0:** $\frac{1}{3}$ bias 1: $\frac{1}{2}$ bias

M[1:0]: LCD drive mode selection

00: 1:4 multiplex; 4 backplanes 01: static; 1 backplane
 10: 1:2 multiplex; 2 backplanes 11: 1:3 multiplex; 3 backplanes

To increase driving capabilities, refer to section "Backplane Outputs" on page 18 and its illustration on page 19.

(2) Load-Data-Pointer

Action	D7	D6	D5	D4	D3	D2	D1	D0
Load data pointer	0	DP6	DP5	DP4	DP3	DP2	DP1	DP0

P[6:0]: 7-bit binary value of 0 to 79, transferred to the data pointer to define one of 80 display RAM addresses. Value range: **0000000b~1001111b**, that is 0~79 in decimal.

(3) Frame-Rate-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select Frame Rate	1	0	0	0	0	0	FR1	FR0

FR[1:0]: **00b:** 64Hz 01b: 82Hz 10b: 110Hz 11b: 200Hz

(4) Device-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select Device	1	1	1	0	0	A2	A1	A0

A[2:0]: 3-bit binary value of 0 to 7 (default **000b**), transferred to the sub-address counter to define one of 8 hardware sub-addresses.

(5) Bank-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select RAM I/O	1	1	1	1	1	0	I	O

This command has no effect in 1:3 or 1:4 multiplex drive mode.

I: input bank selection, that is to select the storage of arriving display data

0: RAM bit 0 (RAM bits 0 and 1) 1: RAM bit 2 (RAM bits 2 and 3)

O: output bank selection, that is to select the retrieval of LCD display data

0: RAM bit 0 (RAM bits 0 and 1) 1: RAM bit 2 (RAM bits 2 and 3)

(6) Blink-Select

Action	D7	D6	D5	D4	D3	D2	D1	D0
Select blink	1	1	1	1	0	A	BF1	BF0

A: blink mode selection

0: normal blinking. Normal blinking can only be selected when multiplex drive mode=1:3 or 1:4.

1: blinking by alternating display RAM banks

BF[1:0]: blink frequency selection

00b: off 01b: blink mode 1 10b: blink mode 2 11b: blink mode 3

See the Blink Frequency table for detailed description about each blink mode.

BLOCK FUNCTION DESCRIPTION

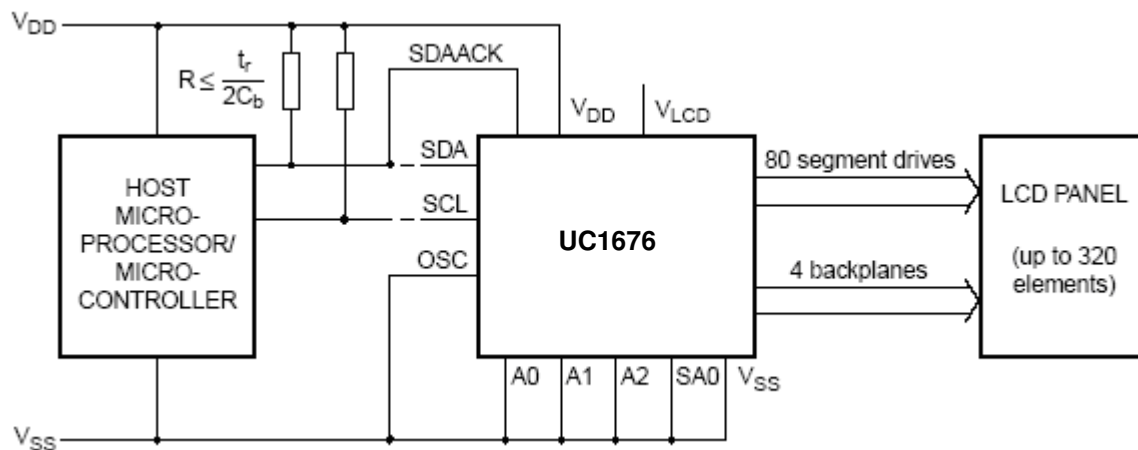
The UC1676 is a versatile peripheral device, designed to interface between any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 80 SEGs.

The display configurations possible with the UC1676 depend on the required number of active backplane outputs. A selection of display configurations is shown in table below:

Possible Display Configurations

# of Backplanes	# of Elements	7-SEG alphanumeric		14-SEG alphanumeric		Dot matrix
		Digits	Indicator Symbols	Characters	Indicator Symbols	
4	320	40	40	20	40	320 (4x80)
3	240	30	30	16	16	240 (3x80)
2	160	20	20	10	20	160 (2x80)
1	80	10	10	5	10	80 (1x80)

All of the display configurations can be implemented in a typical system as shown in following figure:



The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the UC1676.

The internal oscillator is selected by connecting pin OSC to V_{ss}. The only other connections required to complete the system are the power supplies (V_{DD}, V_{ss}, and V_{LCD}) and the LCD panel selected for the application.

LCD Bias Generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors between V_{LCD} and V_{ss}. The center resistor is bypassed by switch if the $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration is selected.

LCD Voltage Selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the Mode-Set command in the Command Description section. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of VLCD and the resulting discrimination ratios (D), are given in table below:

LCD Drive Mode	# of Backplanes	# of Levels	LCD Bias Configuration	$\frac{V_{OFF(RMS)}}{V_{LCD}}$	$\frac{V_{ON(RMS)}}{V_{LCD}}$	$D = \frac{V_{ON(RMS)}}{V_{OFF(RMS)}}$
static	1	2	static	0	1	∞
1:2 multiplex	2	3	1/2	0.354	0.791	2.236
1:2 multiplex	2	4	1/3	0.333	0.745	2.236
1:3 multiplex	3	4	1/3	0.333	0.638	1.915
1:4 multiplex	4	4	1/3	0.333	0.577	1.732

A practical value for VLCD is determined by equating VOFF(RMS) with a defined LCD threshold voltage (Vth), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is VLCD > 3Vth.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$,

where a = 1 for $\frac{1}{2}$ bias

a = 2 for $\frac{1}{3}$ bias

The RMS on-state voltage (VON(RMS)) for the LCD is calculated with Equation (1):

$$V_{ON(RMS)} = V_{LCD} \sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \dots\dots\dots (1)$$

where n = 1 for static mode
 n = 2 for 1:2 multiplex
 n = 3 for 1:3 multiplex
 n = 4 for 1:4 multiplex

The RMS off-state voltage (VOFF(RMS)) for the LCD is calculated with Equation (2):

$$V_{OFF(RMS)} = V_{LCD} \sqrt{\frac{a^2 - 2a + n}{n \times (1+a)^2}} \dots\dots\dots (2)$$

Discrimination is the ratio of VON(RMS) to VOFF(RMS) and is determined from Equation (3):

$$D = \frac{V_{on(rms)}}{V_{off(rms)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \dots\dots\dots (3)$$

where the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage VLCD, shown as follows:

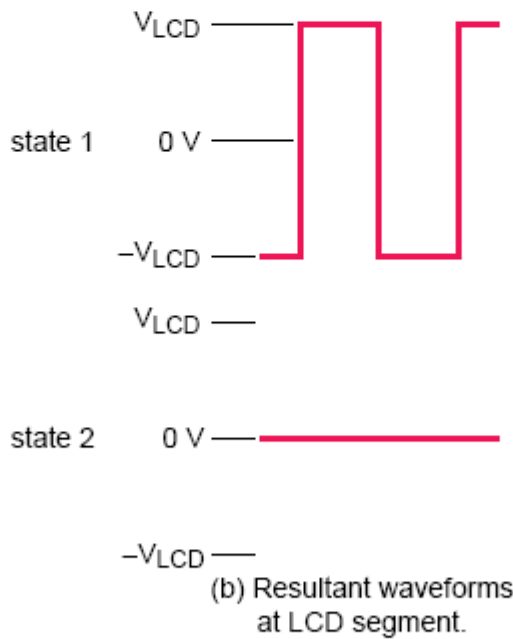
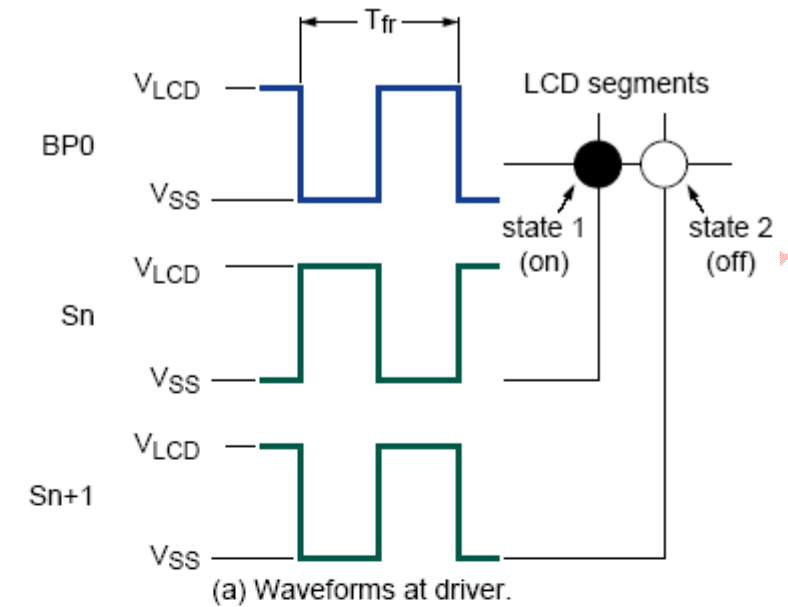
- 1:3 multiplex ($\frac{1}{2}$ bias):
 $V_{LCD} = \sqrt{6} \times V_{OFF(RMS)} = 2.449 V_{OFF(RMS)}$
- 1:4 multiplex ($\frac{1}{2}$ bias):
 $V_{LCD} = [\frac{4 \times \sqrt{3}}{3}] = 2.309 V_{OFF(RMS)}$

These compare with VLCD=3 VOFF(RMS) when $\frac{1}{3}$ bias is used.

It should be noted that VLCD is sometimes referred as the LCD operating voltage.

LCD Drive Mode Waveforms – Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and SEG drive waveforms for this mode are shown in the figure below:



$$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$$

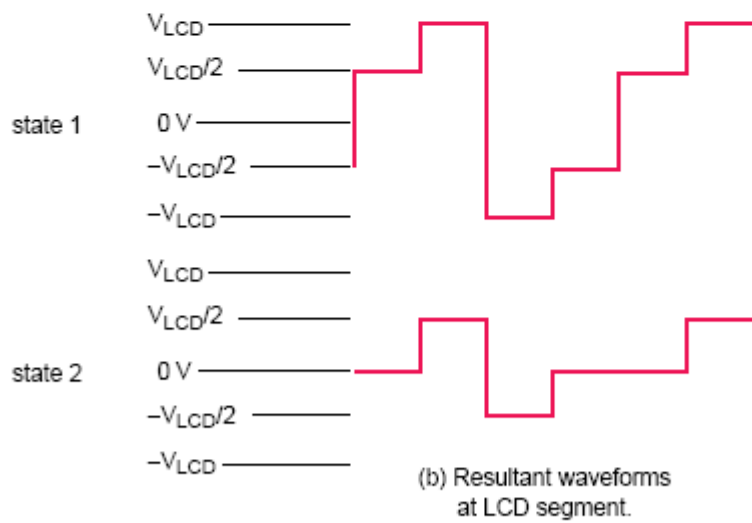
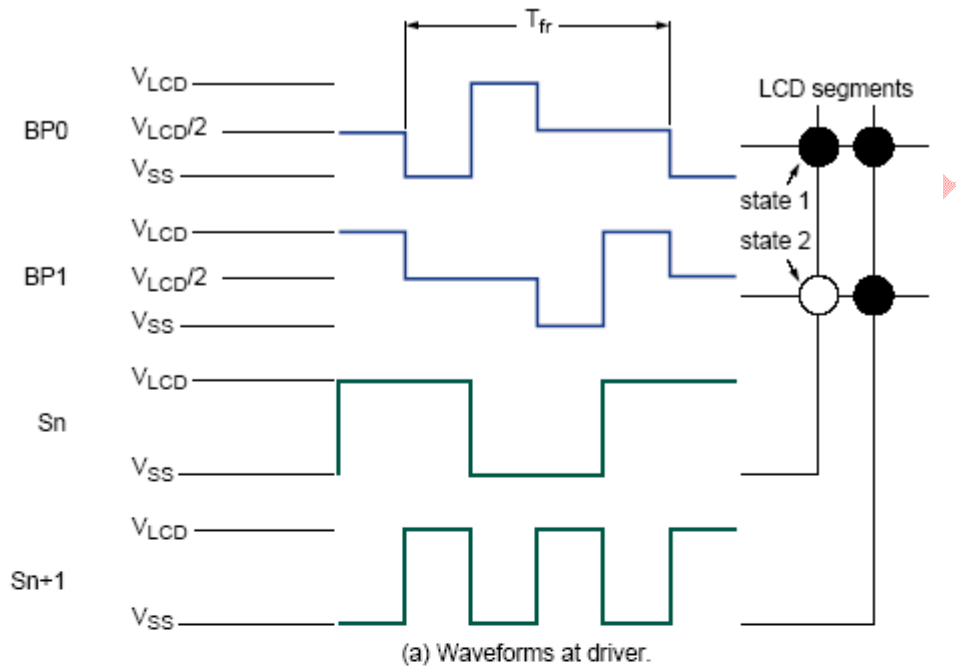
$$V_{on(RMS)} = V_{LCD}.$$

$$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t).$$

$$V_{off(RMS)} = 0 V.$$

LCD Drive Mode Waveforms – 1:2 Multiplex drive mode

When two (2) backplanes are provided in the LCD, the 1:2 multiplex mode applies. The UC1676 allows the use of $\frac{1}{2}$ bias or $\frac{1}{3}$ bias in this mode as shown in the following 2 figures.



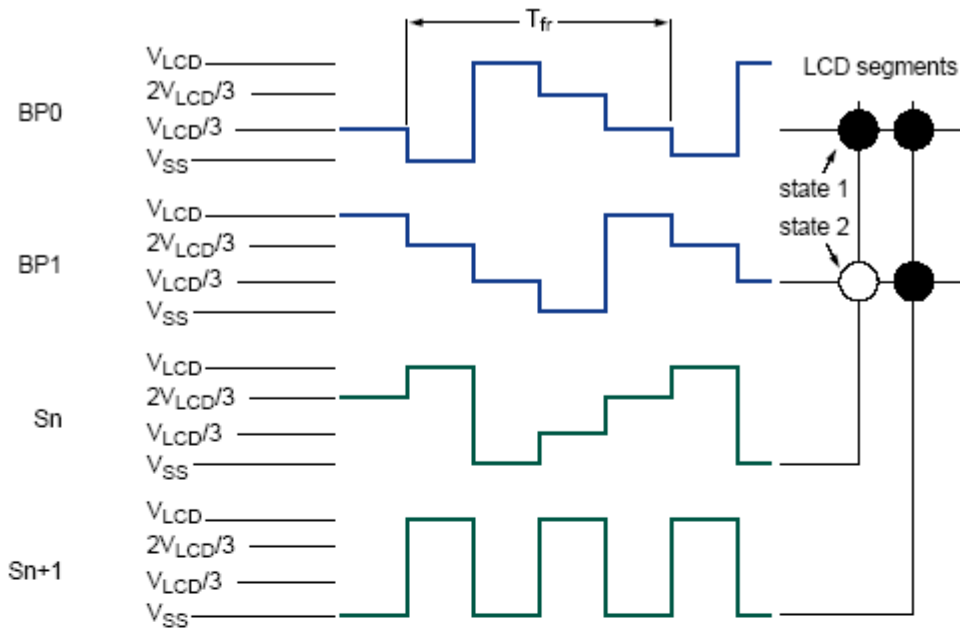
$$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$$

$$V_{on(RMS)} = 0.791V_{LCD}.$$

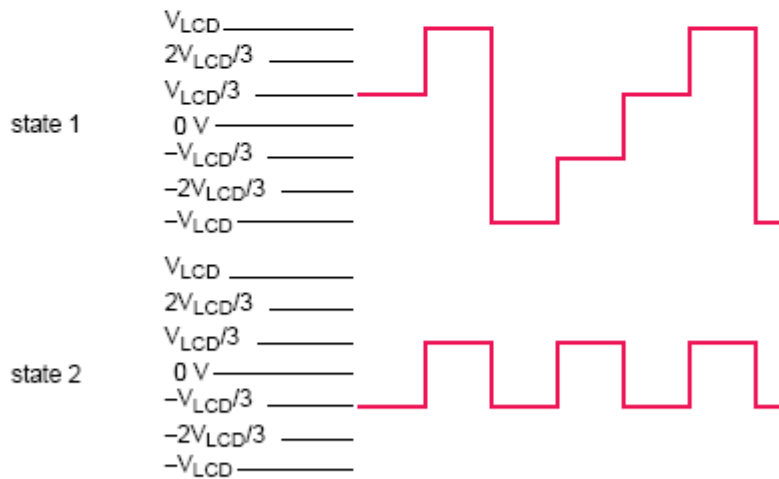
$$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t).$$

$$V_{off(RMS)} = 0.354V_{LCD}.$$

Waveforms for the 1:2 multiplex drive mode with $\frac{1}{2}$ bias



(a) Waveforms at driver.



(b) Resultant waveforms at LCD segment.

$$V_{\text{state1}}(t) = V_{S_n}(t) - V_{BP0}(t).$$

$$V_{\text{on(RMS)}} = 0.745V_{\text{LCD}}.$$

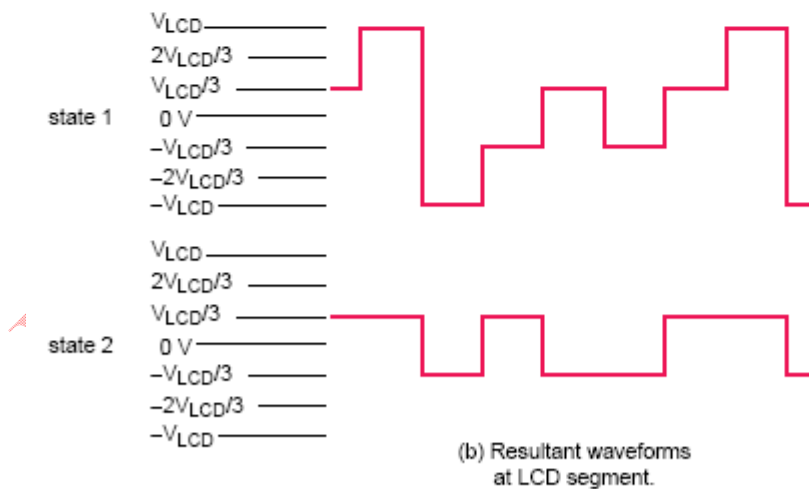
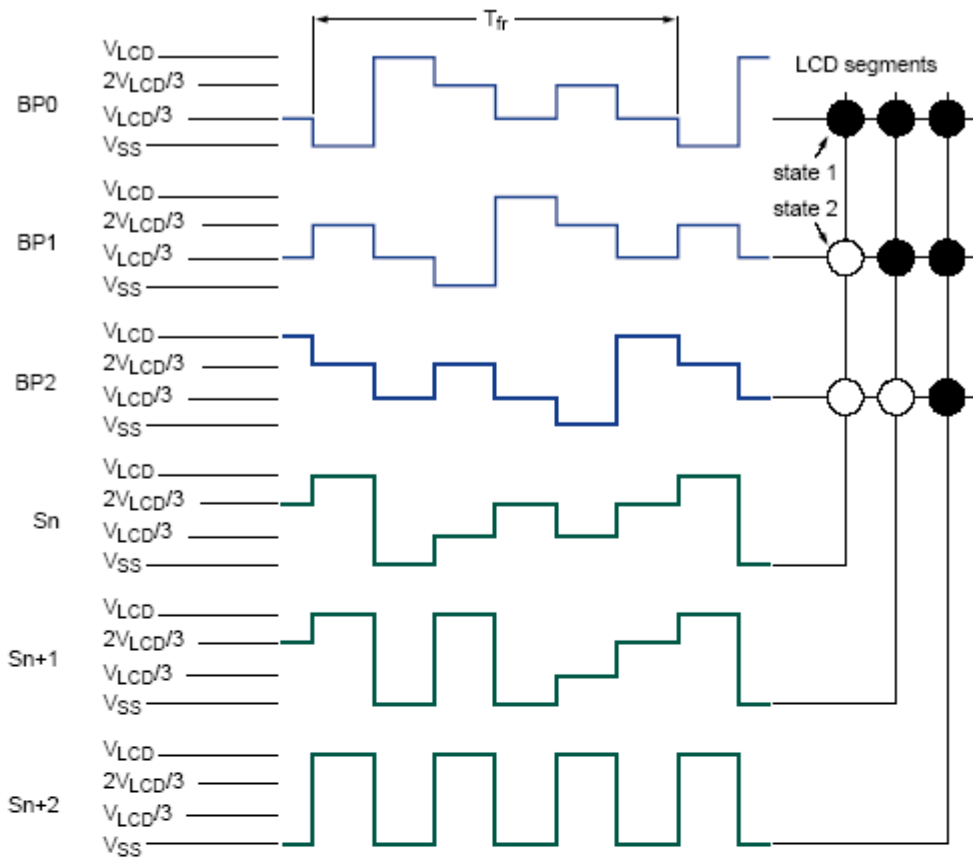
$$V_{\text{state2}}(t) = V_{S_n}(t) - V_{BP1}(t).$$

$$V_{\text{off(RMS)}} = 0.333V_{\text{LCD}}.$$

Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias

LCD Drive Mode Waveforms – 1:3 Multiplex drive mode

When three (3) backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in the figure below:



$$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$$

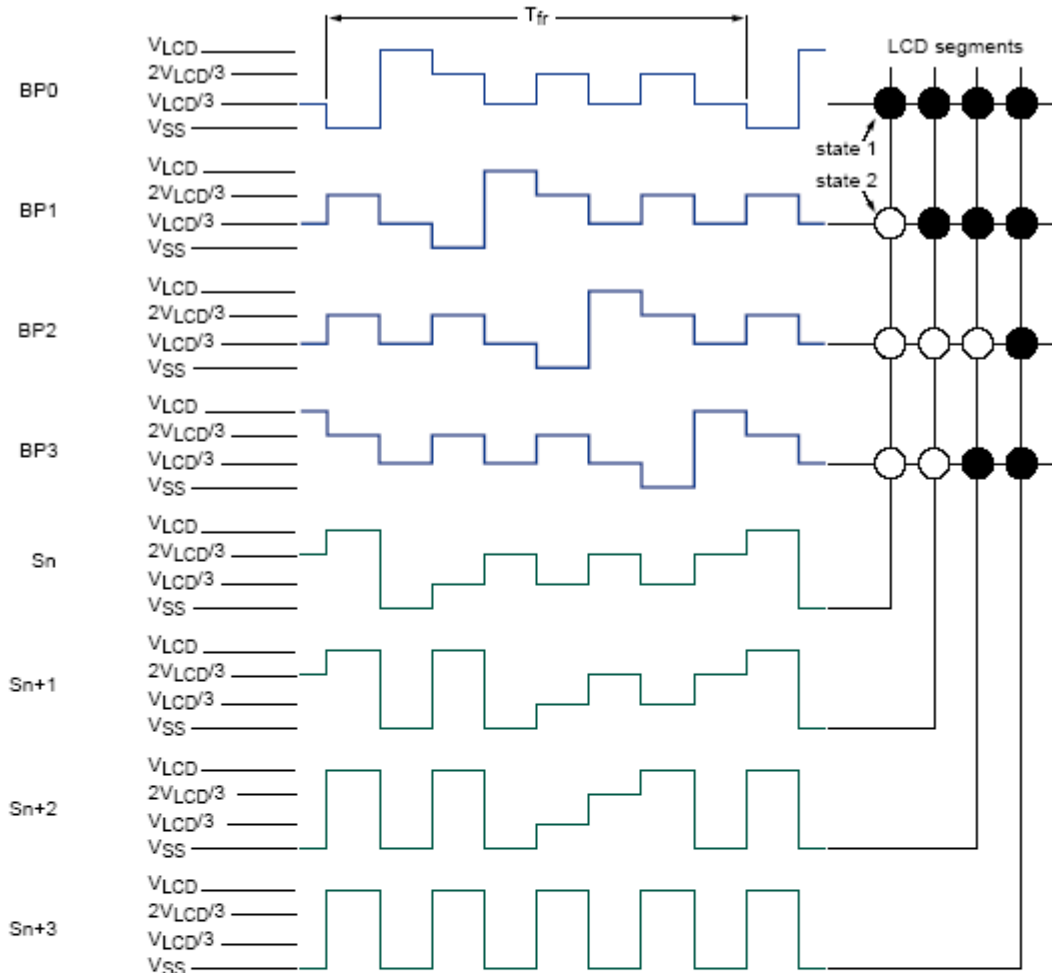
$$V_{on(RMS)} = 0.638V_{LCD}.$$

$$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t).$$

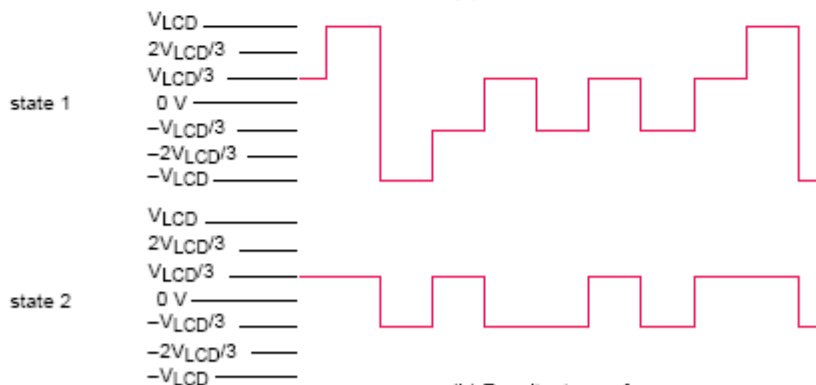
$$V_{off(RMS)} = 0.333V_{LCD}.$$

LCD Drive Mode Waveforms – 1:4 Multiplex drive mode

When four (4) backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in the figure below:



(a) Waveforms at driver.



(b) Resultant waveforms at LCD segment.

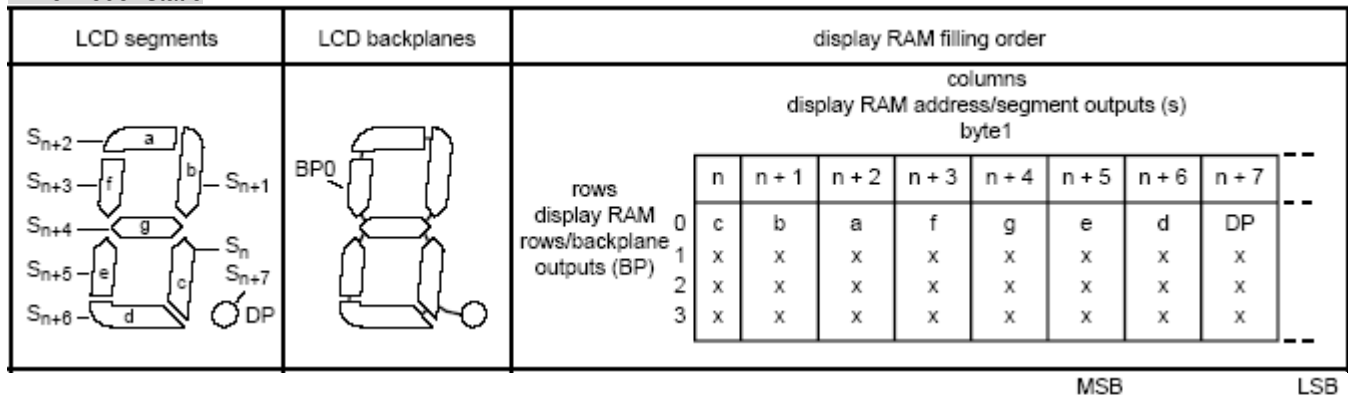
$$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$$

$$V_{on(RMS)} = 0.577V_{LCD}.$$

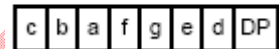
$$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t).$$

$$V_{off(RMS)} = 0.333V_{LCD}.$$

Drive Mode: Static

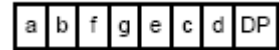
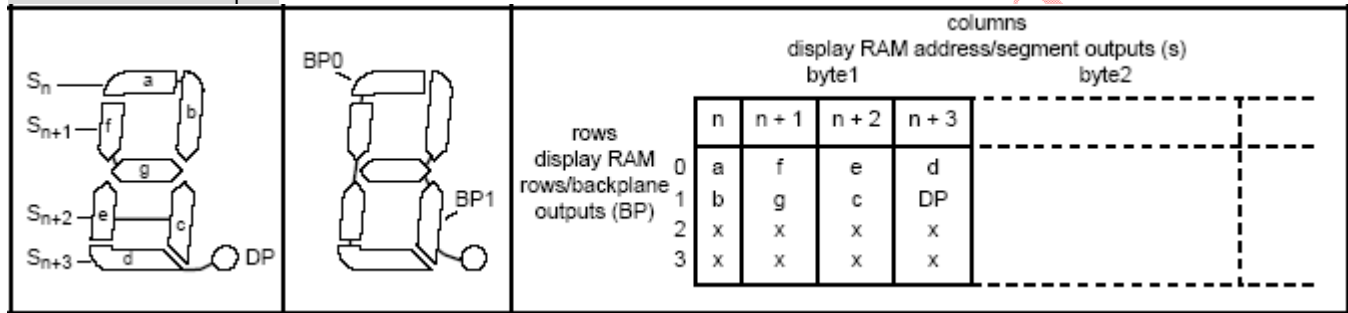


MSB LSB



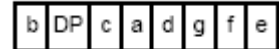
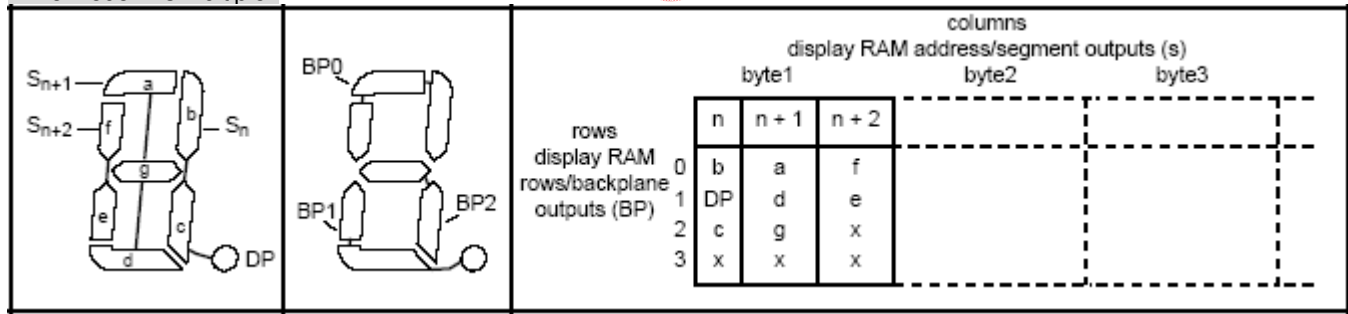
Transmitted Display Byte:

Drive Mode: 1:2 multiplex



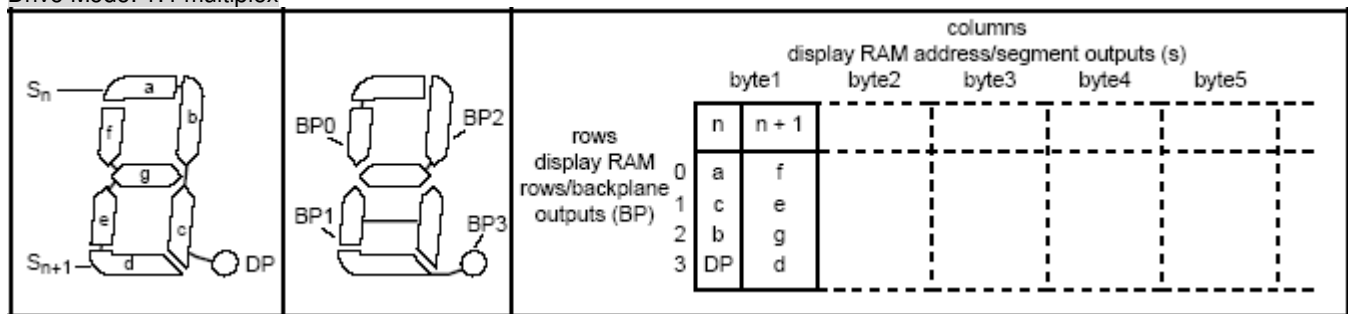
Transmitted Display Byte:

Drive Mode: 1:3 multiplex



Transmitted Display Byte:

Drive Mode: 1:4 multiplex



Transmitted Display Byte:

Remark: x = data bit unchanged

When display data is transmitted to the UC1676, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current

multiplex drive mode, data is stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-SEG display showing all drive modes is given in the Figure on the previous page; the RAM filling organization depicted applies equally to other LCD types.

The following applies to the figure on last page:

static	the 8 transmitted data bits are placed into row 0 of 8 successive 4-bit RAM words.
1:2 multiplex	the 8 transmitted data bits are placed in pairs into rows 0 and 1 of 4 successive 4-bit RAM words.
1:3 multiplex	the 8 bits are placed in triples into row 0, 1 and 2 of 3 successive 4-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
1:4 multiplex	the 8 transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 of 2 successive 4-bit RAM words.

Data Pointer

The addressing mechanism for the display RAM is realized using a data pointer.

This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command.

Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in the Figure on the previous page.

After each byte is stored, the content of the data pointer is automatically increased by a value dependent on the selected LCD drive mode:

Static	by eight (8)
1:2 multiplex	by four (4)
1:3 multiplex	by three (3)
1:4 multiplex	by two (2)

If an I²C-bus data access is terminated early then the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

Sub-address Counter

The storage of display data is conditioned by the content of the sub-address counter. Storage is allowed only when the content of the sub-address counter match with the hardware sub-address applied to A0, A1, and A2. The sub-address counter value is defined by the device-select command (see command (4) Device-select). If the content of the sub-address counter and the hardware sub-address do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The sub-address counter is also increased when the data pointer overflows. The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next UC1676 occurs when the last RAM address is exceeded. Sub-addressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (ex. during the 27th display data byte

transmitted in 1:3 mux mode).

The hardware sub-address must not be changed whilst the device is being accessed on the I²C -bus interface.

Output bank selector

The output bank selector selects one of the 4 rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

Static	Row 0 is selected
1:2 multiplex	Rows 0 and 1 are selected
1:3 multiplex	Rows 0, 1, and 2 are selected sequentially
1:4 multiplex	All RAM addresses of row 0 are selected, these are followed by the contents of row 1, row 2, and then row 3.

The UC1676 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command. The input bank selector functions independently to the output bank selector.

Blinking

The display blink capabilities of the UC1676 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see command (6) Blink-select). The blink frequencies are fractions of the clock frequency. The ratios between the clock and blink frequencies depend on the blink mode selected:

Blink mode	Operating mode ratio	Blink frequency			
		fclk=1.536kHz	fclk=1.97kHz	fclk=2.640kHz	fclk=4.800kHz
off	–	blinking off	blinking off	Blinking off	Blinking off
1	fclk / 768	2.0Hz	2.5Hz	3.5Hz	6.3Hz
2	fclk / 1536	1.0Hz	1.3Hz	1.7Hz	3.1Hz
3	fclk / 3072	0.5Hz	0.6Hz	0.9Hz	1.6Hz

An additional feature is for an arbitrary selection of LCD SEGs to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD SEGs can blink by selectively changing the display RAM data at fixed time intervals.

If the entire display can blink at a frequency other than the typical blink frequency. This can be effectively performed by setting the display enable bit E at the required rate using the Mode-set command in the Command Description section.

Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor

when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

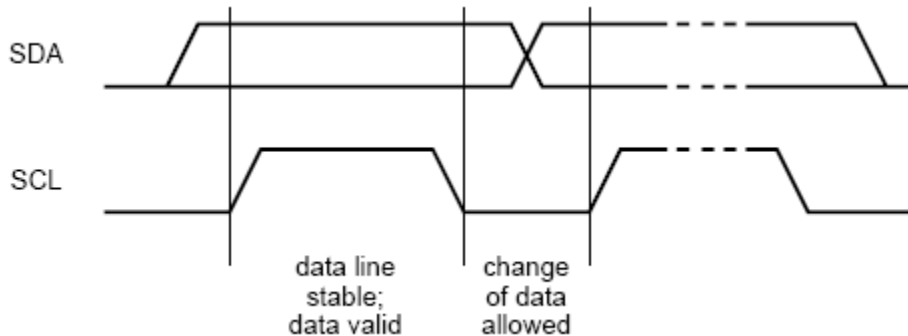
By connecting pin SDAACK to pin SDA on the UC1676, the SDA line becomes fully I²C-bus compatible. In COG applications where the track resistance from the SDAACK pin to the system SDA line can be significant, possibly a voltage divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. As a consequence it may be possible that the acknowledge generated by the UC1676 can't be interpreted as logic 0 by the master. In COG applications where the acknowledge cycle is required, it is therefore necessary to minimize the track resistance from the SDAACK pin to the system SDA line to guarantee a valid LOW level.

By separating the acknowledge output from the serial data line (having the SDAACK open circuit) design efforts to generate a valid acknowledge level can be avoided. However, in that case the I²C -bus master has to be set up in such a way that it ignores the acknowledge cycle.

The following definition assumes SDA and SDAACK are connected and refers to the pair as SDA.

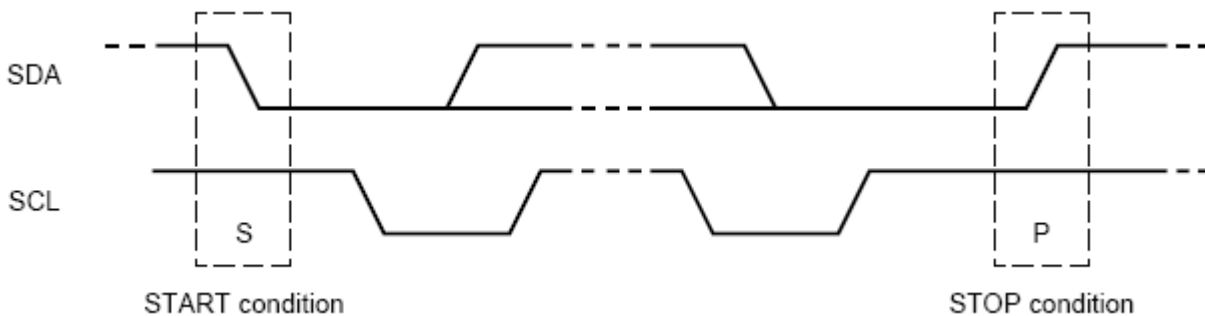
Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see the Bit Transfer Figure below).



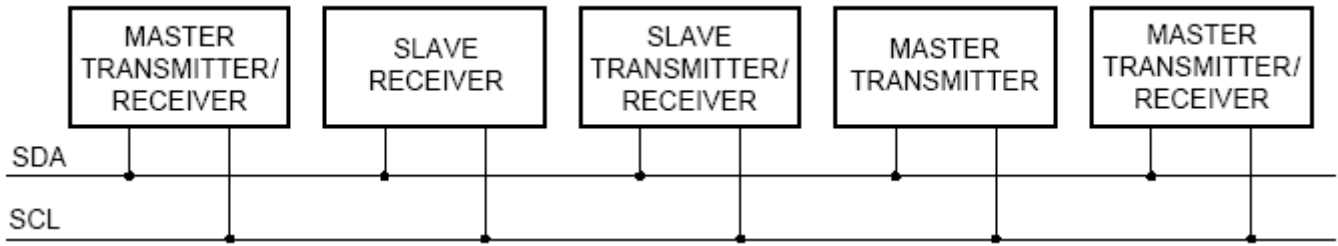
START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A High-to-Low change of the data line, while the clock is High, is defined as the START condition (S). A Low-to-High change of the data line, while the clock is High, is defined as the STOP condition (P). The START and STOP conditions are shown in the START/STOP Definition figure below:



System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in the figure below:

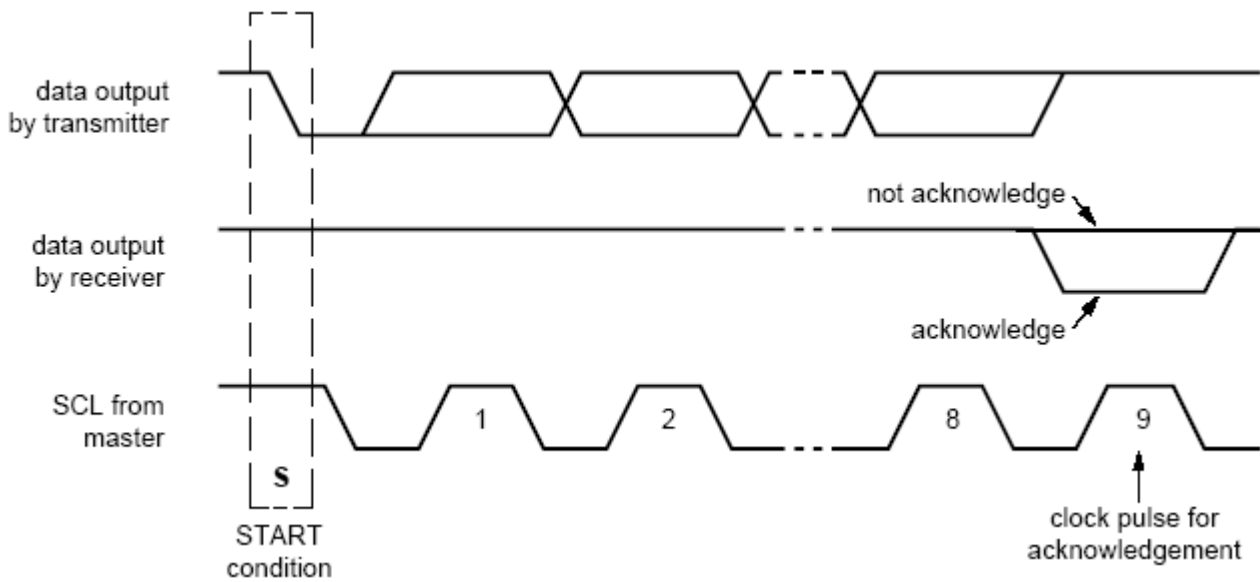


Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is shown in the figure below.



I²C-bus Controller

The UC1676 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the UC1676 are the acknowledge signals from the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data, and on the hardware sub-address.

In single device applications, the hardware sub-address inputs A0, A1, and A2 are normally tied to V_{ss} which defines the hardware sub-address 0. In multiple device applications

A0, A1, and A2 are tied to V_{ss} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware sub-address.

Input Filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

POWER MANAGEMENT

Power-Up Sequence

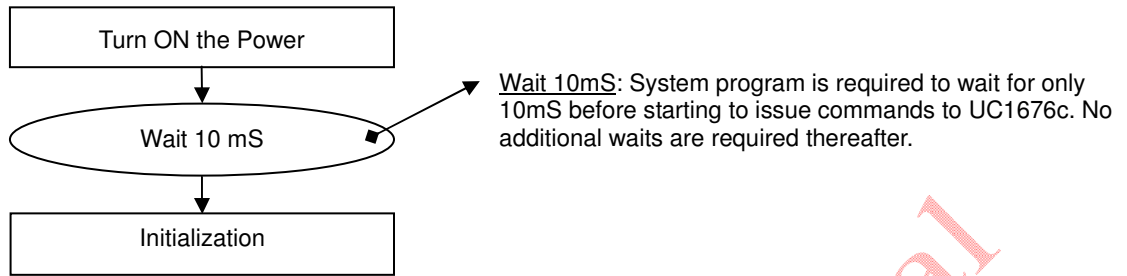


Figure 8: Reference Power-Up Sequence

There's no delay needed while turning ON V_{DD} :

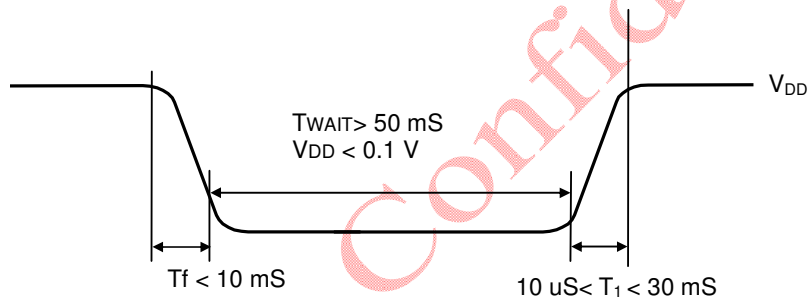


Figure 9: Power Off-On Sequence

Sample Power Management Command Sequences

The following tables are examples of command sequence for power-up and power-down operations. These are only to demonstrate some “*typical, generic*” scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

<u>Type</u>	<u>Required:</u>	These items are required
	<u>Customized:</u>	These items are not necessary if customer parameters are the same as default
	<u>Advanced:</u>	We recommend new users to skip these commands and use default values.
	<u>Optional:</u>	These commands depend on what users want to do.

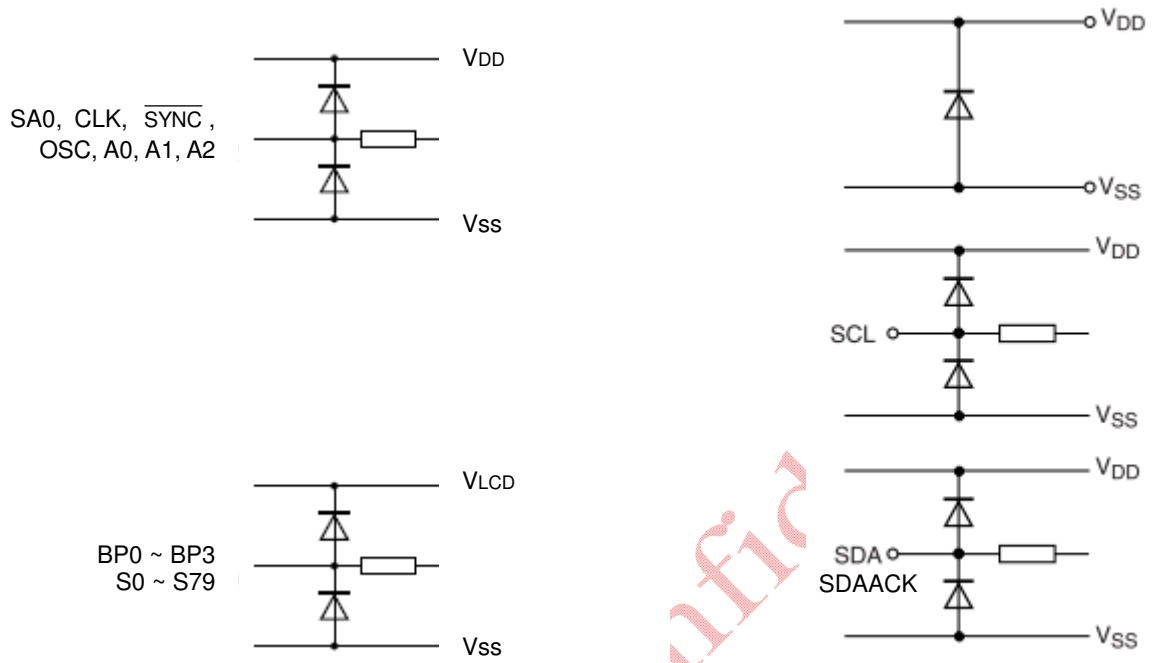
Power-Up

Type	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	Turn on V _{DD} and V _{LCD}	Wait until V _{DD} , V _{LCD} are stable
R	–	–	–	–	–	–	–	–	Wait 10mS	
R	1	0	0	0	0	0	0	0	Select Frame Rate	Default: 00b
R	1	1	1	0	0	0	0	0	Select Device	Default: 000b
R	1	1	1	1	1	0	0	0	Select Bank	Default: 00b
R	1	1	1	1	0	0	0	0	Select Blink Mode	Default: 000b
R	0	0	0	0	0	0	0	0	Set load data pointer	Default: 000 0000b
O	#	#	#	#	#	#	#	#	Write display RAM Bit Map	Set up display image
		
	#	#	#	#	#	#	#	#		
R	1	1	0	0	1	0	0	0	Set Display Mode	Set display enable

Power-Down

Type	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	C	1	0	0	0	0	0	0	Set Display Mode	Set display disable
R	–	–	–	–	–	–	–	–		V _{DD} and V _{LCD} OFF

INTERNAL CIRCUITRY



Ultrachip Confidential

ABSOLUTE MAXIMUM RATING

In accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{DD}	Supply voltage		-0.5	+6.5	V
V _{LCD}	LCD supply voltage		-0.5	+12.1	V
V _{i(n)}	Voltage on any input	V _{DD} related inputs	-0.5	+6.5	V
V _{o(n)}	Voltage on any output	V _{LCD} related outputs	-0.5	+12.1	V
I _i	Input current		-10	+10	mA
I _o	Output current		-10	+10	mA
I _{DD}	Supply current		-50	+50	mA
I _{SS}	Ground supply current		-50	+50	mA
I _{DD(LCD)}	LCD supply current		-50	+50	mA
P _{tot}	Total power dissipation		-	400	mW
P _{/out}	Power dissipation per output		-	100	mW
t _{STG}	Storage temperature		-55	+125	°C
t _{OPR}	Operation temperature		-40	+85	°C

Note: Static voltages across the liquid crystal display (LCD) can build up when the LCD supply voltage (V_{LCD}) is ON while the IC supply voltage (V_{DD}) is OFF, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

DC CHARACTERISTICS

V_{DD}=2.5V~5.5V, V_{SS}=0V, V_{LCD}=2.5V~11.0V, T_a=-40°C~+85°C, unless otherwise specified.

Symbol	Characteristics	Condition	Min.	Typical	Max.	Unit
Supply						
V _{DD}	Supply voltage		2.5	–	5.5	V
V _{LCD}	LCD supply voltage		2.5	–	11.0	V
I _{DD(LCD)}	LCD supply current	f _{CLK(EXT)} =1536Hz [1]		16	60	μA
I _{DD}	Supply current	f _{CLK(EXT)} =1536Hz [2]		2	20	μA
Logic						
V _I	Input voltage		V _{SS} -0.5	–	V _{DD} +0.5	V
V _{IH}	Input voltage – high	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0~A2, SA0	0.8 V _{DD}	–	V _{DD}	V
V _{IL}	Input voltage – low		V _{SS}	–	0.2 V _{DD}	V
V _{OH}	Output voltage – high		0.8 V _{DD}	–	–	V
V _{OL}	Output voltage – low		–	–	0.2 V _{DD}	V
I _{OH}	Output current – high	on pins CLK, V _{OH} =4.6V, V _{DD} =5V	+1	–	–	mA
I _{OL}	Output current – low	on pins CLK, $\overline{\text{SYNC}}$, V _{OL} =0.4V, V _{DD} =5V	–	–	–1	mA
I _L	Leakage current	on pins OSC, CLK, SCL, SDA, A0~A2, SA0, V _I =V _{DD} or V _{SS} .	–1	–	+1	μA
C _I	Input capacitance	[2]	–	–	7	pF
I ² C bus, input on pins SDA and SCL						
V _I	Input voltage		V _{SS} -0.5	–	5.5	V
V _{IH}	Input voltage – high		0.8 V _{DD}	–	5.5	V
V _{IL}	Input voltage – low		V _{SS}	–	0.2 V _{DD}	V
C _I	Input capacitance	[2]	–	–	7	pF
I _{OL(SDA)}	Output current – low	V _{OL} =0.4V, V _{DD} =5V, on pin SDA	+3	–	–	mA
LCD outputs						
ΔV _o	Output voltage variation	CBPL=35nF, on pin BPx	-100	–	+100	mV
		CSGM=5nF, on pin Sx	-100	–	+100	mV
R _o	Output resistance	V _{LCD} =5V, on pin BPx [3]	–	1.5	10	kΩ
		V _{LCD} =5V, on pin Sx [3]	–	6.0	13.5	kΩ

Note:

- [1] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
 [2] Not tested, design specification only.
 [3] Outputs measured individually and sequentially.

AC CHARACTERISTICS

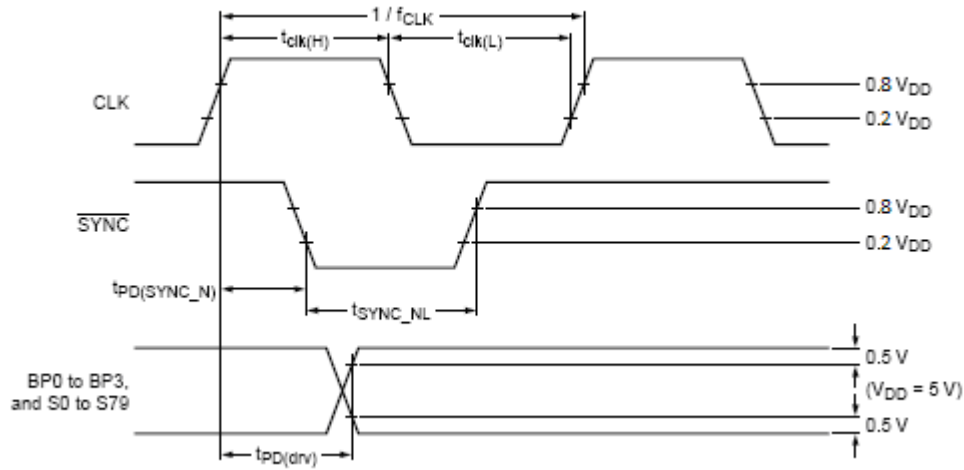


Figure: Driver Timing Waveform

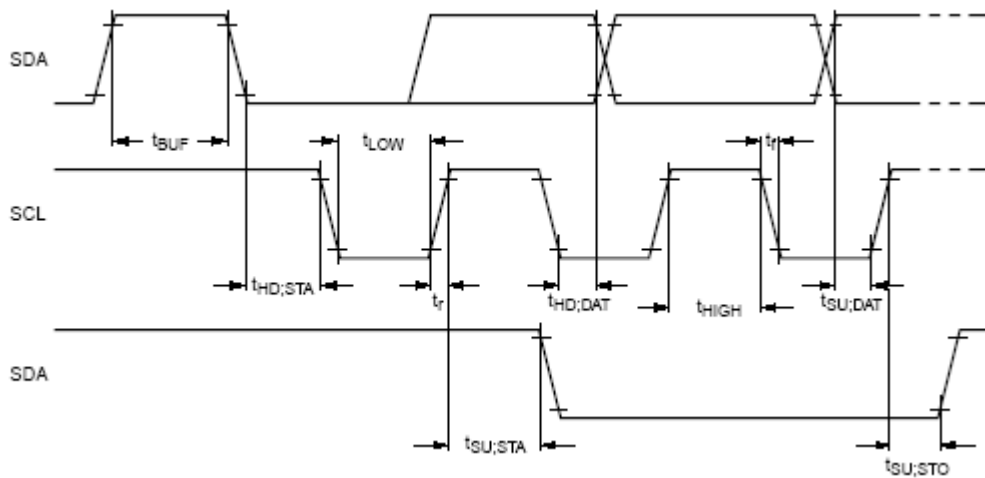


Figure: I²C Series Interface Characteristics

VDD=2.5V~5.5V, VSS=0V, VLCD=2.5V~11.0V, TAMB= -40°C~+85°C; unless otherwise specified.

Symbol	Signal	Description	Condition	Min.	Typ.	Max.	Unit
Internal: output pin CLK							
fCLK	CLK	Clock frequency	[1][2]	-25%	1536	+25%	Hz
					1970		
					2640		
					4800		
fFR	CLK	Frame frequency	[1][2]	-25%	64	+25%	Hz
					82		
					110		
					200		
External: input pin CLK							
fCLK(EXT)	CLK	External clock frequency	[2]	800	-	9600	Hz
fCLK(H)	CLK	High-level clock time		90	-	-	uS
fCLK(L)	CLK	Low-level clock time		90	-	-	uS
Synchronization: input pin $\overline{\text{SYNC}}$							
tPD(SYNC_N)	$\overline{\text{SYNC}}$	$\overline{\text{SYNC}}$ propagation delay		-	30	-	nS
tSYNC_NL	$\overline{\text{SYNC}}$	$\overline{\text{SYNC}}$ low time		[5]	-	-	uS
Outputs: pins BP0~BP3 and S0~S79							
tPD(DRV)	BP0~BP3, S0~S79	Driver propagation delay	VLCD=5V	-	-	30	uS
I ² C bus timing [3][4]							
fSCL	SCL	SCL clock frequency		-	-	400	kHz
tHIGH	SCL	HIGH period of the SCL clock		0.6	-	-	uS
tLOW	SCL	LOW period of the SCL clock		1.3	-	-	uS
SDA pin							
tSU/DAT	SDA	Data set-up time		100	-	-	nS
tHD;DAT	SDA	Data hold time		0	-	-	nS
SCL and SDA pins							
Tbuf	SCL, SDA	Bus free time between STOP & START		1.3	-	-	uS
Tsu;sto	SCL, SDA	Set-up time from STOP		0.6	-	-	uS
Thd;sta	SCL, SDA	Hold time (repeated) START		0.6	-	-	uS
Tsu;sta	SCL, SDA	Set-up time for a repeated START		0.6	-	-	uS
Tr	SCL, SDA	Rise time of both SDA and SCL signals		-	-	0.3	uS
Tf	SCL, SDA	Fall time of both SDA and SCL signals		-	-	0.3	uS
Cb	SCL, SDA	Capacitive load for each bus line		-	-	400	pF
Tw(spike)	SCL, SDA	Spike pulse width	On bus	-	-	50	nS

Note:

- [1] Typical output duty cycle of 50 %.
- [2] The corresponding frame frequency is $f_{fr} = \frac{f_{clk}}{24}$.
- [3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to VIL and VIH with an input voltage swing of VSS to VDD.
- [4] For I²C-bus timings see the I²C Figure on the previous page.
- [5] The value is half cycle time.

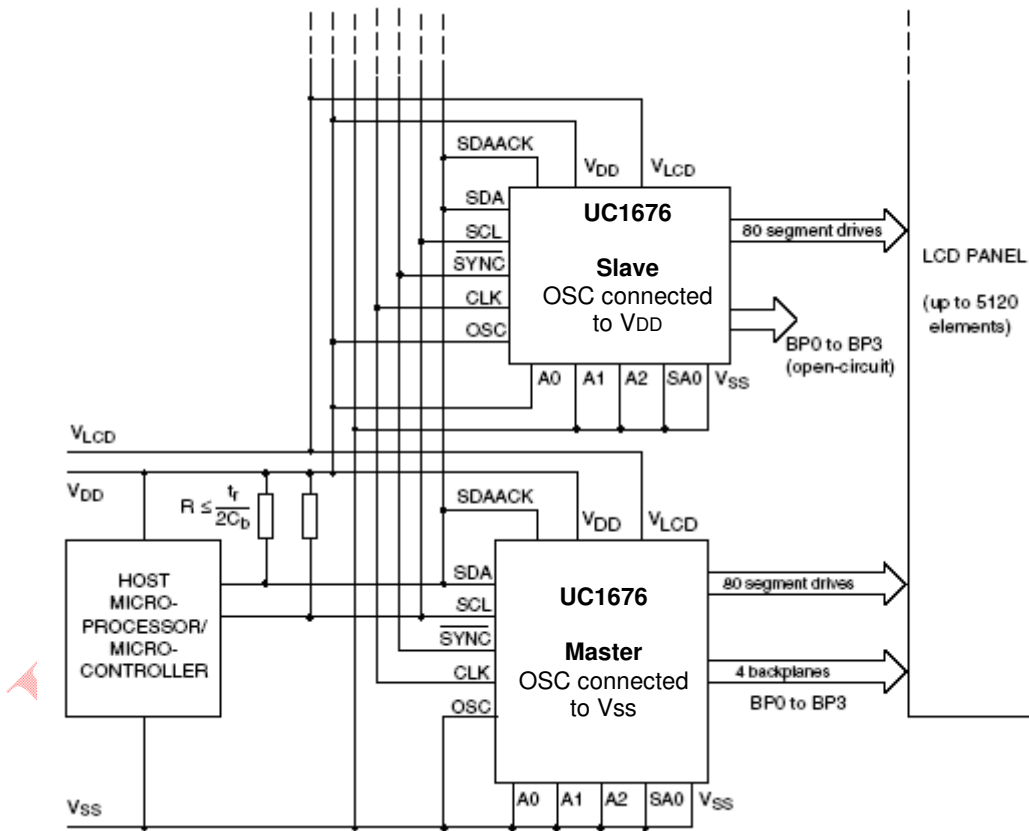
CASCADED OPERATION

In large display configurations, up to 16 UC1676 can be recognized on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, and A2) and the programmable I²C bus slave address (SA0).

Cluster	SA0	A[2:0]	Device
1	0	000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	7

Cluster	SA0	A[2:0]	Device
2	1	000	8
		001	9
		010	10
		011	11
		100	12
		101	13
		110	14
		111	15

When cascaded UC1676 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other UC1676 of the cascade contribute additional SEG outputs, but their backplane outputs are left open-circuit (See the following Figure).

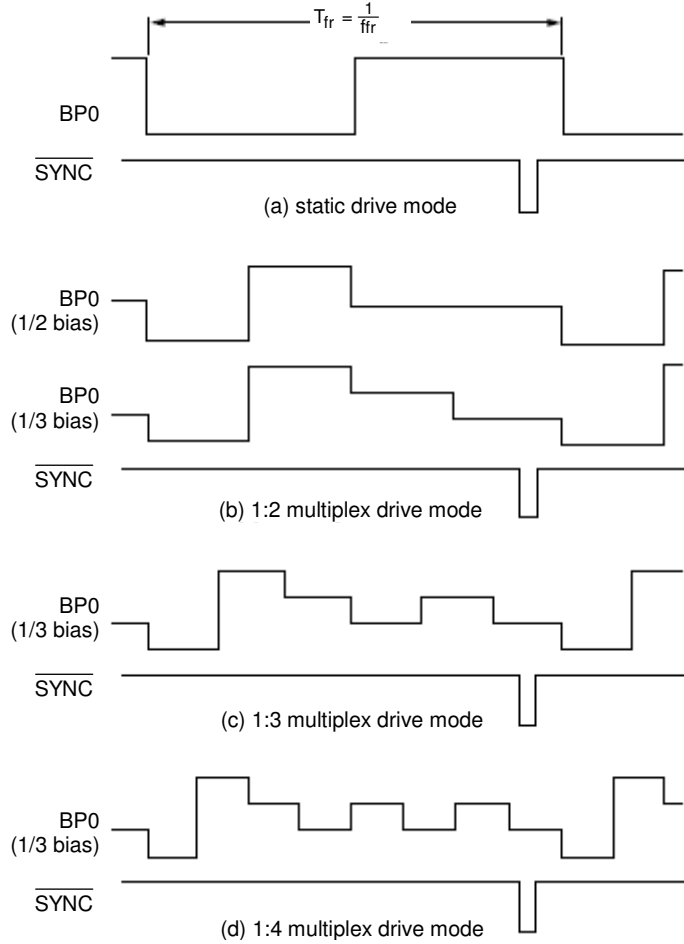


For display sizes that are not multiple of 320 elements, a mixed cascaded system can be considered containing only devices like UC1676. Depending on the application, one must take care of the software command and pin connection compatibility.

Only one master but multiple slaves are allowed in a cascade. No external clock should be used; the slaves get the clock from the master.

The SYNC line is provided to maintain the correct synchronization between all cascaded UC1676's. The only time that SYNC is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by the definition of a multiplex drive mode when UC1676 with different SA0 levels are cascaded).

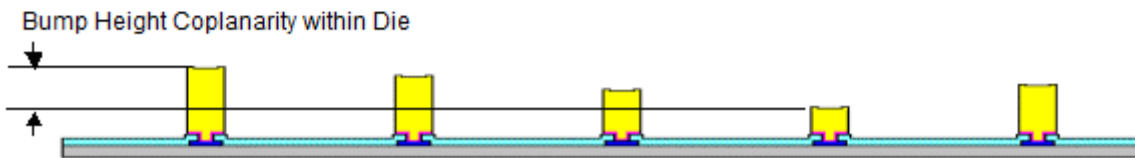
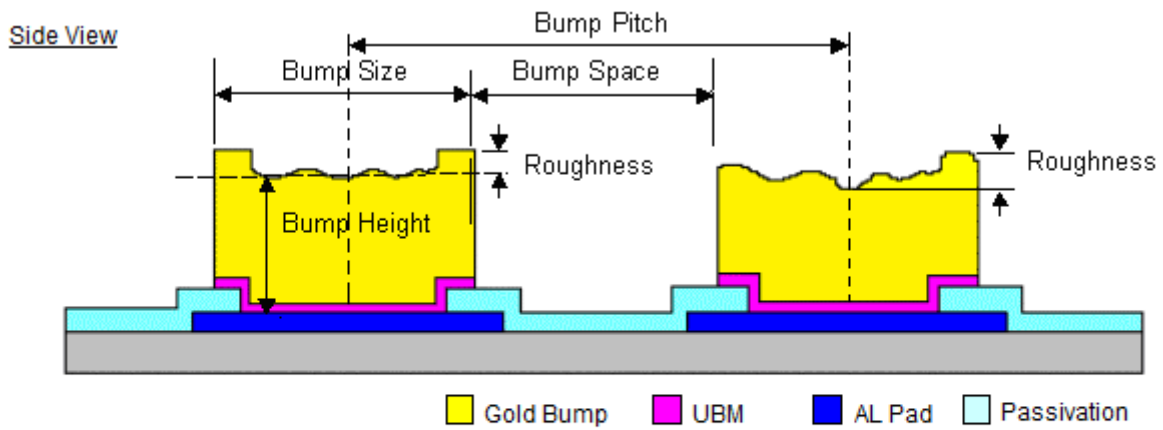
$\overline{\text{SYNC}}$ is organized as an input/output pin; The output selection is realized as an open-drain driver with an internal pull-up resistor. A UC1676 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first UC1676 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the UC1676 are shown in the Figure below.



The contact resistance between the $\overline{\text{SYNC}}$ pins of cascaded devices must be controlled. If the resistance is too high, then the device will not be able to synchronize properly. This is particularly applicable to COG applications. The table below shows the limited values for contact resistance.

Number of devices	Maximum contact resistance
2	6000 Ω
3~5	2200 Ω
6~10	1200 Ω
11~16	700 Ω

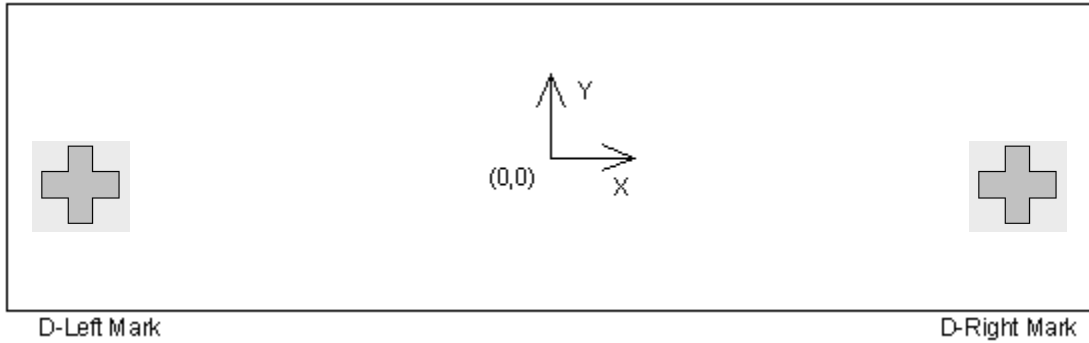
PHYSICAL DIMENSIONS



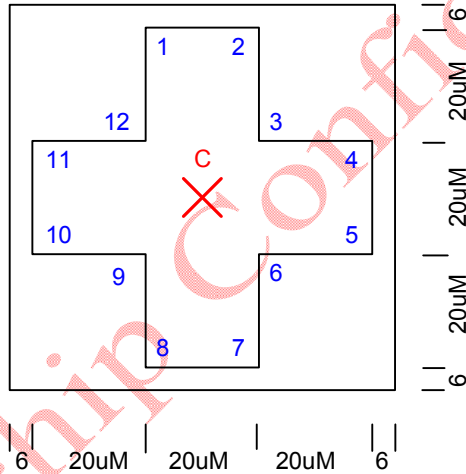
Die Size:	$(5256\mu\text{M} \pm 40\mu\text{M}) \times (1382\mu\text{M} \pm 40\mu\text{M})$
Die Thickness:	$300\mu\text{M} \pm 20\mu\text{M}$
Die TTV:	$(D_{\text{MAX}} - D_{\text{MIN}})$ within die $\leq 2\mu\text{M}$
Bump Height:	$15\mu\text{M} \pm 3\mu\text{M}$
	$(H_{\text{MAX}} - H_{\text{MIN}})$ within die $\leq 2\mu\text{M}$
Hardness:	$90\text{Hv} \pm 25\text{Hv}$
Bump Size:	$(50\mu\text{M} \pm 3\mu\text{M}) \times (90\mu\text{M} \pm 3\mu\text{M})$
Bump Area:	$4500\mu\text{M}^2$
Bump Pitch:	$80\mu\text{M}$
Bump Gap:	$30\mu\text{M} \pm 4\mu\text{M}$
Coordinate origin:	Chip center
Pad reference:	Pad center

ALIGNMENT MARK INFORMATION

ALIGNMENT MARK POSITION:



ALIGNMENT MARK SHAPES:



ALIGNMENT MARK COORDINATES:

Point	Left mark		Right mark	
	X	Y	X	Y
1	-2381	-107	2361	-121
2	-2361	-107	2381	-121
3	-2361	-127	2381	-141
4	-2341	-127	2401	-141
5	-2341	-147	2401	-161
6	-2361	-147	2381	-161
7	-2361	-167	2381	-181
8	-2381	-167	2361	-181
9	-2381	-147	2361	-161
10	-2401	-147	2341	-161
11	-2401	-127	2341	-141
12	-2381	-127	2361	-141
C	-2371	-137	2371	-151

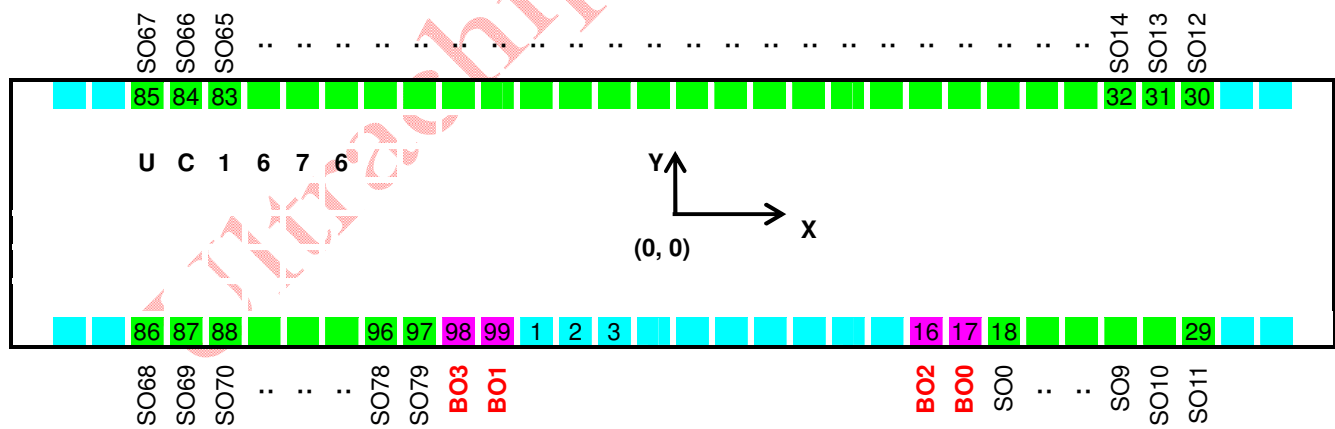
PAD COORDINATES

No	Name	X	Y	W	H
1	SDAACK	-1079.2	-594.4	50	90
2	SDA	-839.2	-594.4	50	90
3	SDA	-759.2	-594.4	50	90
4	SCL	-599.2	-594.4	50	90
5	SCL	-519.2	-594.4	50	90
6	CLK	-414.8	-594.4	50	90
7	VDD	-284.8	-594.4	50	90
8	SYNC	4.2	-594.4	50	90
9	OSC	119.2	-594.4	50	90
10	A0	249.2	-594.4	50	90
11	A1	379.2	-594.4	50	90
12	A2	581.2	-594.4	50	90
13	SA0	711.2	-594.4	50	90
14	VSS	841.2	-594.4	50	90
15	VLCD	1099.6	-594.4	50	90
16	BO<2>	1277.6	-594.4	50	90
17	BO<0>	1357.6	-594.4	50	90
18	SO<0>	1437.6	-594.4	50	90
19	SO<1>	1517.6	-594.4	50	90
20	SO<2>	1597.6	-594.4	50	90
21	SO<3>	1677.6	-594.4	50	90
22	SO<4>	1757.6	-594.4	50	90
23	SO<5>	1837.6	-594.4	50	90
24	SO<6>	1917.6	-594.4	50	90
25	SO<7>	1997.6	-594.4	50	90
26	SO<8>	2077.6	-594.4	50	90
27	SO<9>	2157.6	-594.4	50	90
28	SO<10>	2237.6	-594.4	50	90
29	SO<11>	2317.6	-594.4	50	90
30	SO<12>	2357.6	594.4	50	90
31	SO<13>	2277.6	594.4	50	90
32	SO<14>	2197.6	594.4	50	90
33	SO<15>	2117.6	594.4	50	90
34	SO<16>	2037.6	594.4	50	90
35	SO<17>	1957.6	594.4	50	90
36	SO<18>	1877.6	594.4	50	90

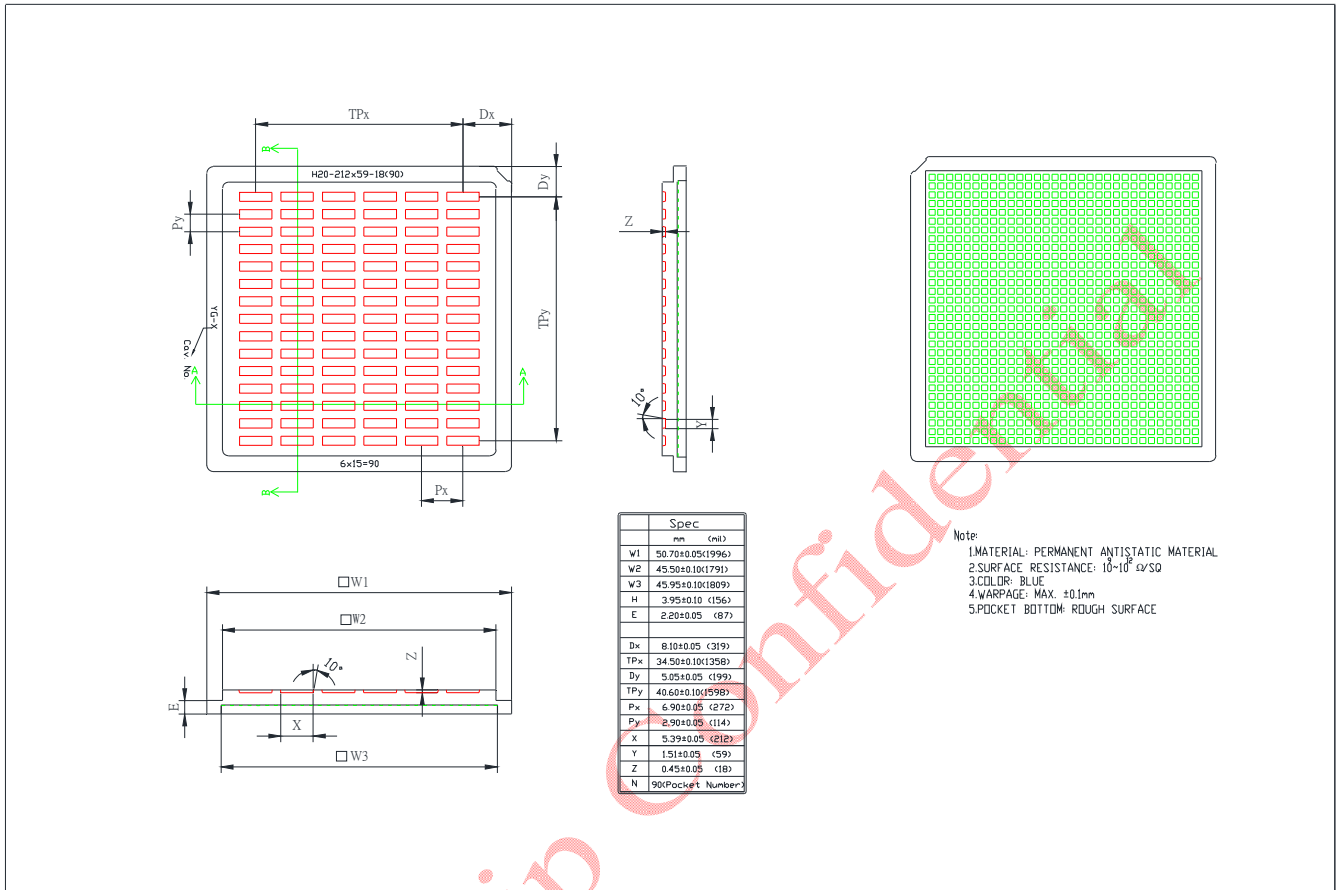
No	Name	X	Y	W	H
37	SO<19>	1797.6	594.4	50	90
38	SO<20>	1717.6	594.4	50	90
39	SO<21>	1637.6	594.4	50	90
40	SO<22>	1557.6	594.4	50	90
41	SO<23>	1477.6	594.4	50	90
42	SO<24>	1317.6	594.4	50	90
43	SO<25>	1237.6	594.4	50	90
44	SO<26>	1157.6	594.4	50	90
45	SO<27>	1077.6	594.4	50	90
46	SO<28>	997.6	594.4	50	90
47	SO<29>	917.6	594.4	50	90
48	SO<30>	837.6	594.4	50	90
49	SO<31>	757.6	594.4	50	90
50	SO<32>	677.6	594.4	50	90
51	SO<33>	597.6	594.4	50	90
52	SO<34>	437.6	594.4	50	90
53	SO<35>	357.6	594.4	50	90
54	SO<36>	277.6	594.4	50	90
55	SO<37>	197.6	594.4	50	90
56	SO<38>	117.6	594.4	50	90
57	SO<39>	37.6	594.4	50	90
58	SO<40>	-42.4	594.4	50	90
59	SO<41>	-122.4	594.4	50	90
60	SO<42>	-202.4	594.4	50	90
61	SO<43>	-282.4	594.4	50	90
62	SO<44>	-362.4	594.4	50	90
63	SO<45>	-442.4	594.4	50	90
64	SO<46>	-602.4	594.4	50	90
65	SO<47>	-682.4	594.4	50	90
66	SO<48>	-762.4	594.4	50	90
67	SO<49>	-842.4	594.4	50	90
68	SO<50>	-922.4	594.4	50	90
69	SO<51>	-1002.4	594.4	50	90
70	SO<52>	-1082.4	594.4	50	90
71	SO<53>	-1162.4	594.4	50	90
72	SO<54>	-1242.4	594.4	50	90

No	Name	X	Y	W	H
73	SO<55>	-1322.4	594.4	50	90
74	SO<56>	-1402.4	594.4	50	90
75	SO<57>	-1562.4	594.4	50	90
76	SO<58>	-1642.4	594.4	50	90
77	SO<59>	-1722.4	594.4	50	90
78	SO<60>	-1802.4	594.4	50	90
79	SO<61>	-1882.4	594.4	50	90
80	SO<62>	-1962.4	594.4	50	90
81	SO<63>	-2042.4	594.4	50	90
82	SO<64>	-2122.4	594.4	50	90
83	SO<65>	-2202.4	594.4	50	90
84	SO<66>	-2282.4	594.4	50	90
85	SO<67>	-2362.4	594.4	50	90
86	SO<68>	-2322.4	-594.4	50	90
87	SO<69>	-2242.4	-594.4	50	90
88	SO<70>	-2162.4	-594.4	50	90
89	SO<71>	-2082.4	-594.4	50	90
90	SO<72>	-2002.4	-594.4	50	90

No	Name	X	Y	W	H
91	SO<73>	-1922.4	-594.4	50	90
92	SO<74>	-1842.4	-594.4	50	90
93	SO<75>	-1762.4	-594.4	50	90
94	SO<76>	-1682.4	-594.4	50	90
95	SO<77>	-1602.4	-594.4	50	90
96	SO<78>	-1522.4	-594.4	50	90
97	SO<79>	-1442.4	-594.4	50	90
98	BO<3>	-1362.4	-594.4	50	90
99	BO<1>	-1282.4	-594.4	50	90
100	DUMMY1	2469.7	-594.4	50	90
101	DUMMY2	2549.7	-594.4	50	90
102	DUMMY3	2517.6	594.4	50	90
103	DUMMY4	2437.6	594.4	50	90
104	DUMMY5	-2442.3	594.4	50	90
105	DUMMY6	-2522.3	594.4	50	90
106	DUMMY7	-2554.4	-594.4	50	90
107	DUMMY8	-2474.4	-594.4	50	90



TRAY INFORMATION



REVISION HISTORY

Revision	Description	Date
0.6	First Release	Sep. 17, 2014
0.7	(1) DC Characteristics section, V _{IH} (Min.): 0.7V _{DD} → 0.8V _{DD} V _{IL} (Max.): 0.3V _{DD} → 0.2V _{DD}	Jan. 6, 2015
	(2) AC Characteristics section, SYNC low time: 1 → half cycle time	
0.8	(Same as Revision 0.7)	Mar. 20, 2015
1.0	(1) The description for command (1) is enriched.	Aug. 12, 2015
	(2) Operation Temperature (Min.): -30 → -40°C (Absolute Maximum Rating section, page 27)	
1.1	(1) The Power-ON Reset section is removed.	Dec. 15, 2017
	(2) The word "resetting" is removed from description in the Blinking section.	
	(3) "Power-ON Reset Voltage" item is removed from the DC Characteristics table.	
	(4) "Power-ON Reset" related description is removed from the Cascaded Operation section.	
	(5) The maximum limitation of falling/rising time, tf/tr, is removed.	