



## UC1842B/43B-D

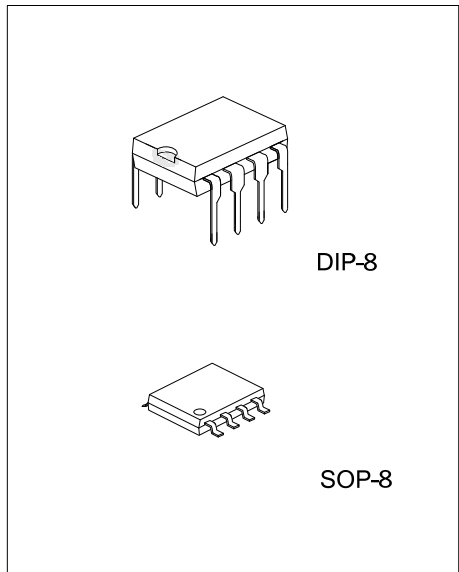
## LINEAR INTEGRATED CIRCUIT

### HIGH PERFORMANCE CURRENT MODE PWM CONTROLLERS

#### DESCRIPTION

The UTC **UC1842B-D/1843B-D** are high performance fixed frequency current mode controllers that specifically designed for Off-Line and DC to DC converter applications with minimal external parts count.

The differences between **UC1842B-D** and **UC1843B-D** are the under-voltage lockout thresholds. The **UC1842B-D** ideally suited to off-line applications with UVLO thresholds of 16V<sub>(ON)</sub> and 10V<sub>(OFF)</sub>, and **UC1843B-D** has UVLO thresholds of 8.4V<sub>(ON)</sub> and 7.6V<sub>(OFF)</sub> for lower voltage applications.



#### FEATURES

- \* Operation output switching frequency up to 500 kHz
- \* Automatic feed forward compensation
- \* Latching PWM for cycle-by-cycle current limiting
- \* High current totem pole output
- \* Internally trimmed reference with under voltage lockout
- \* UVLO with hysteresis
- \* Low startup and operating current

#### ORDERING INFORMATION

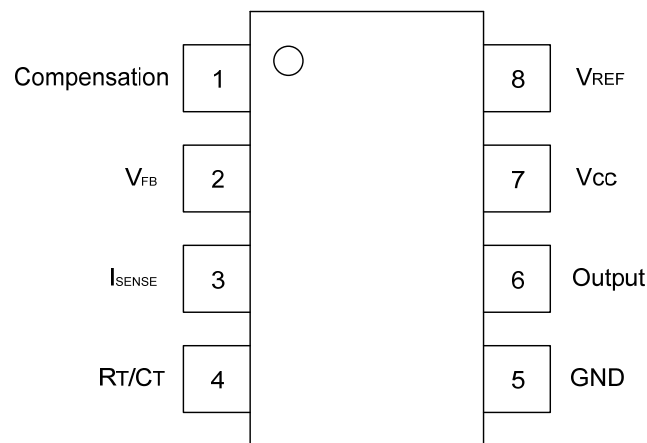
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC1842BL-D-D08-T	UC1842BG-D-D08-T	DIP-8	Tube
UC1842BL-D-S08-R	UC1842BG-D-S08-R	SOP-8	Tape Reel
UC1843BL-D-D08-T	UC1843BG-D-D08-T	DIP-8	Tube
UC1843BL-D-S08-R	UC1843BG-D-S08-R	SOP-8	Tape Reel

<p>UC1842BG-D-D08-T</p> <p>(1) Packing Type (2) Package Type (3) Version Code (4) Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) Version D (4) G: Halogen Free and Lead Free, L: Lead Free</p>
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## MARKING

PACKAGE	UC1842B-D	UC1843B-D
DIP-8		
SOP-8		

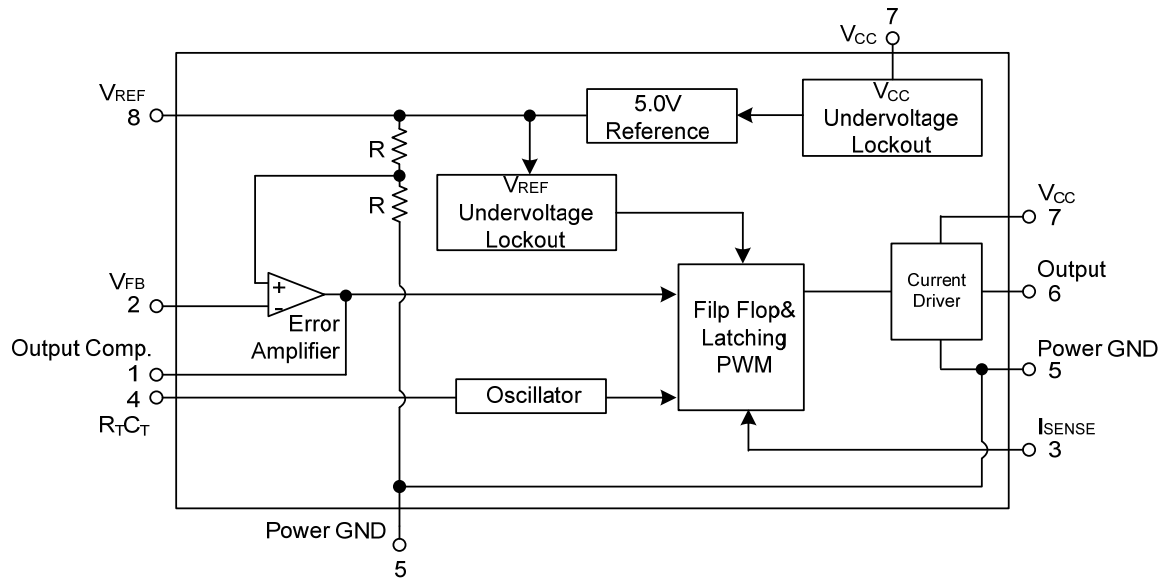
## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NO	PIN NAME	FUNCTION
1	Compensation	Error amplifier output, this pin is made available for loop compensation.
2	$V_{FB}$	Voltage Feedback, the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	$I_{SENSE}$	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	$R_T/C_T$	The Oscillator frequency and maximum output duty cycle are programmed by connecting resistor $R_T$ to $V_{REF}$ and capacitor $C_T$ to ground. Operation to 1 MHz is possible.
5	GND	Power ground
6	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin. The output switches at one-half the oscillator frequency.
7	$V_{CC}$	Positive supply
8	$V_{REF}$	Reference output, provides charging current for capacitor $C_T$ though resistor $R_T$ .

### ■ BLOCK DIAGRAM



### ■ ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT	
Current Sense and Voltage feedback Inputs	V <sub>IN</sub>	-0.3 ~ +5.5	V	
Supply Voltage (Low Impedance Source)	V <sub>CC</sub>	30	V	
Supply Voltage (I <sub>CC</sub> <30mA)	V <sub>CC</sub>	Self Limiting	V	
Error Amp Output Sink Current	I <sub>SINK</sub>	10	mA	
Output Current, Source or Sink (Note 2)	I <sub>OUT</sub>	1.0	A	
Output Energy (Capacitive Load per cycle)	W	5.0	μJ	
Power Dissipation	DIP-8	P <sub>D</sub>	1250	mW
	SOP-8		800	mW
Junction Temperature	T <sub>J</sub>	+150	°C	
Operation Temperature	T <sub>OPR</sub>	-40 ~ +125	°C	
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C	

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Maximum package power dissipation limits must be observed.

### ■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT	
Junction to Ambient	DIP-8	θ <sub>JA</sub>	100	°C/W
	SOP-8		156	°C/W

### ■ ELECTRICAL CHARACTERISTICS

(T<sub>A</sub>=25°C, V<sub>CC</sub>=15V, R<sub>T</sub>=10k, C<sub>T</sub>=3.3nF, -40°C ≤ T<sub>A</sub> ≤ +125°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REFERENCE SECTION</b>						
Reference Output Voltage	V <sub>REF</sub>	I <sub>OUT</sub> =1.0mA, T <sub>J</sub> =25°C	4.9	5.0	5.1	V
Line Regulation	ΔV <sub>OUT</sub>	V <sub>CC</sub> =12V ~ 25V		2.0	20	mV
Load Regulation	ΔV <sub>OUT</sub>	I <sub>OUT</sub> =1.0mA ~ 20mA		15	30	mV
Temperature Stability	t <sub>s</sub>			0.2		mV/°C
Total Output Variation over Line, Load, Temperature	V <sub>REF</sub>		4.82		5.18	V
Output Noise Voltage	e <sub>N</sub>	f=10Hz ~ 10kHz, T <sub>J</sub> =25°C		50		μV
Long Term Stability	S	T <sub>A</sub> =125°C for 1000 Hours		5		mV
Output Short Circuit Current	I <sub>SC</sub>		-50	-155	-280	mA
<b>OSCILLATOR SECTION</b>						
Oscillator Voltage Swing	V <sub>OSC</sub>			1.6		V
Discharge Current	I <sub>DSG</sub>	V <sub>OSC</sub> =2.0V, T <sub>J</sub> =25°C		10.8		mA
Frequency	f <sub>OSC</sub>	T <sub>J</sub> =25°C	47	52	57	kHz
		-40°C ≤ T <sub>A</sub> ≤ +125°C	46		60	
Frequency Change with Voltage	Δf <sub>OSC</sub> /ΔV	V <sub>CC</sub> =12V ~ 25V		0.2	1.0	%
Frequency Change with Temperature	Δf <sub>OSC</sub> /ΔT	-40°C ≤ T <sub>A</sub> ≤ +125°C		5.0		%
<b>ERROR AMPLIFIER SECTION</b>						
Voltage Feedback Input	V <sub>FB</sub>	V <sub>OUT</sub> =2.5V	2.42	2.50	2.58	V
Output Voltage Swing	High	V <sub>OH</sub>	R <sub>L</sub> =15k to ground, V <sub>FB</sub> =2.3V	5.0	6.2	V
	Low	V <sub>OL</sub>	R <sub>L</sub> =15k to V <sub>REF</sub> , V <sub>FB</sub> =2.7V		0.8	
Output Current	Sink	I <sub>SINK</sub>	V <sub>OUT</sub> =1.6V, V <sub>FB</sub> =2.7V	2.0	12	mA
	Source	I <sub>SOURCE</sub>	V <sub>OUT</sub> =5.0V, V <sub>FB</sub> =2.3V	-0.5	-1.0	
Input Bias Current	I <sub>I(BIAS)</sub>	V <sub>FB</sub> =2.7V		-0.1	-2.0	μA
Open Loop Voltage Gain	G <sub>VO</sub>	V <sub>OUT</sub> =2.0V ~ 4.0V	65	90		dB
Power Supply Rejection Ratio	PSRR	V <sub>CC</sub> =12V ~ 25V	60	70		dB
Unity Gain Bandwidth	GB <sub>W</sub>	T <sub>J</sub> =25°C	0.7	1.0		MHz

### ■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT SENSE SECTION</b>							
Current Sense Input Voltage Gain (Note 2, 3)		$G_V$		2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 2)		$V_{I(THR)}$		0.9	1.0	1.1	V
Input Bias Current		$I_{I(BIAS)}$			-2.0	-10	$\mu A$
Power Supply Rejection Ratio		PSRR	$V_{CC}=12V \sim 25V$ (Note 4)		70		dB
Propagation Delay		$t_{PLH(IN/OUT)}$			150	300	ns
<b>OUTPUT SECTION</b>							
Output Voltage	Low	$V_{OL}$	$I_{SINK}=20mA$		0.2	0.8	V
			$I_{SINK}=200mA$		1.6	2.2	V
	High	$V_{OH}$	$I_{SOURCE}=20mA$	11	13.5		V
			$I_{SOURCE}=200mA$	11	13.4		V
Output Voltage with $U_{VLO}$ Activated		$V_{OL(UVLO)}$	$V_{CC}=6.0V, I_{SINK}=1.0mA$		0.7	1.2	V
Output Voltage Rise Time		$t_R$	$C_L=1.0nF, T_J=25^\circ C$		50	150	ns
Output Voltage Fall Time		$t_F$	$C_L=1.0nF, T_J=25^\circ C$		50	150	ns
<b>UNDERVOLTAGE LOCKOUT SECTION</b>							
Startup Threshold	UC1842B-D	$V_{THR}$		14.5	16.0	17.5	V
	UC1843B-D			7.8	8.4	9.0	V
Minimum Operating Voltage After Turn-On	UC1842B-D	$V_{CC(MIN)}$		8.5	10.0	11.5	V
	UC1843B-D			7.0	7.6	8.2	V
<b>PWM SECTION</b>							
Duty Cycle	MAX	$DC_{MAX}$		95	97	100	%
	MIN	$DC_{MIN}$				0	%
<b>TOTAL DEVICE</b>							
Power Supply Zener Voltage		$V_Z$	$I_{CC}=25mA$	30	34		V
Power Supply Current (Note 4)	UC1842B-D	$I_{CC}$	Start Up		0.25	0.5	mA
	UC1843B-D				0.25	0.5	mA
	UC1842B-D		Operating		12	17	mA
	UC1843B-D				12	17	mA

Notes: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

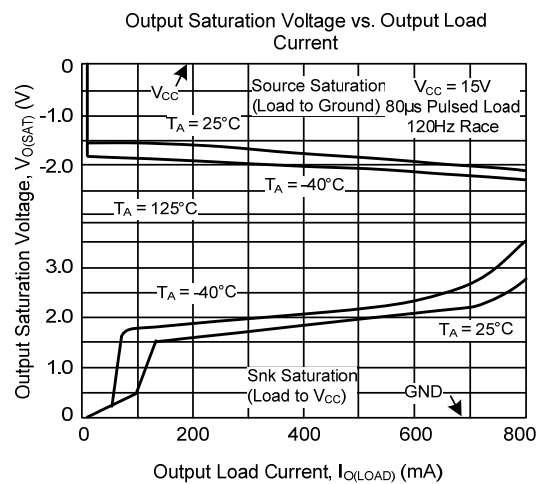
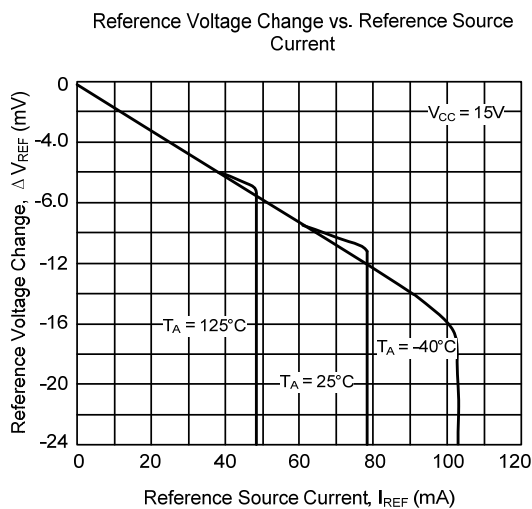
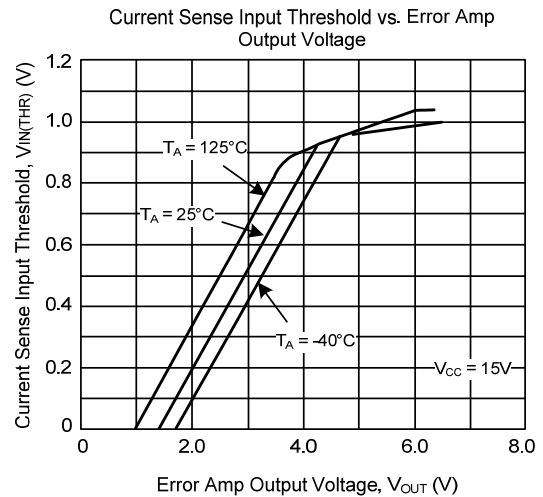
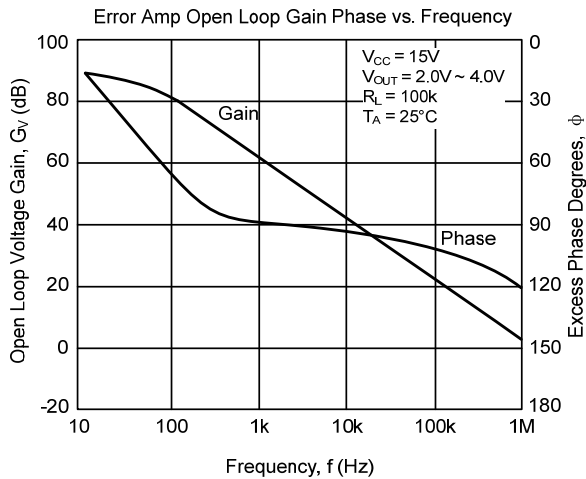
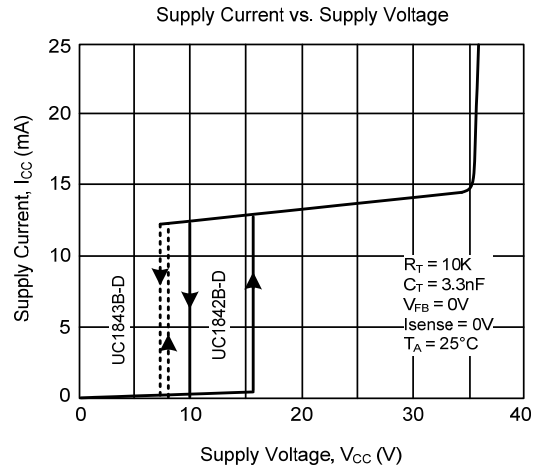
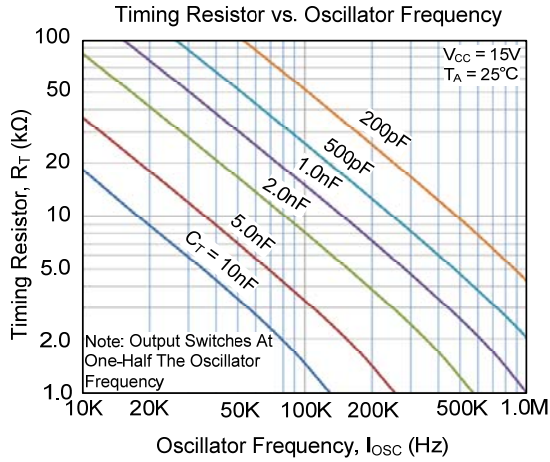
2. This parameter is measured at the latch trip point with  $V_{FB}=0V$ .

3. Comparator gain is defined as:  $\Delta V$  Output Compensation

$$A_V = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$$

4. Adjust  $V_{CC}$  above the startup threshold before setting to 15V.

## TYPICAL CHARACTERISTICS



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