UC1875-SP Rad-Tolerant Class-V, Phase Shift Resonant Controller

1 Features

- QML-V Qualified, SMD 5962-94555
- Rad-Tolerant: 50 kRad (Si) TID (1)
- Zero to 100% Duty Cycle Control
- Programmable Output Turn-On Delay
- Compatible with Voltage or Current Mode Topologies
- Practical Operation at Switching Frequencies to 1 MHz
- Four 2-A Totem Pole Outputs
- 10-MHz Error Amplifier
- Undervoltage Lockout (UVLO)
- Low Startup Current – 150 µA
- Outputs Active Low During UVLO
- Soft-Start Control
- Latched Overcurrent Comparator With Full Cycle Restart
- Trimmed Reference

2 Applications

Power FPGAs

(1) Radiation tolerance is a typical value based upon initial device qualification with a dose rate = 10 mrad/sec and applies to the 5962-9455502 devices. Radiation lot acceptance testing is available – contact factory for details.

3 Description

The UC1875-SP implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This circuit may be configured to provide control in either voltage or current mode operation, with a separate overcurrent shutdown for fast fault protection.

A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A-B, C-D).

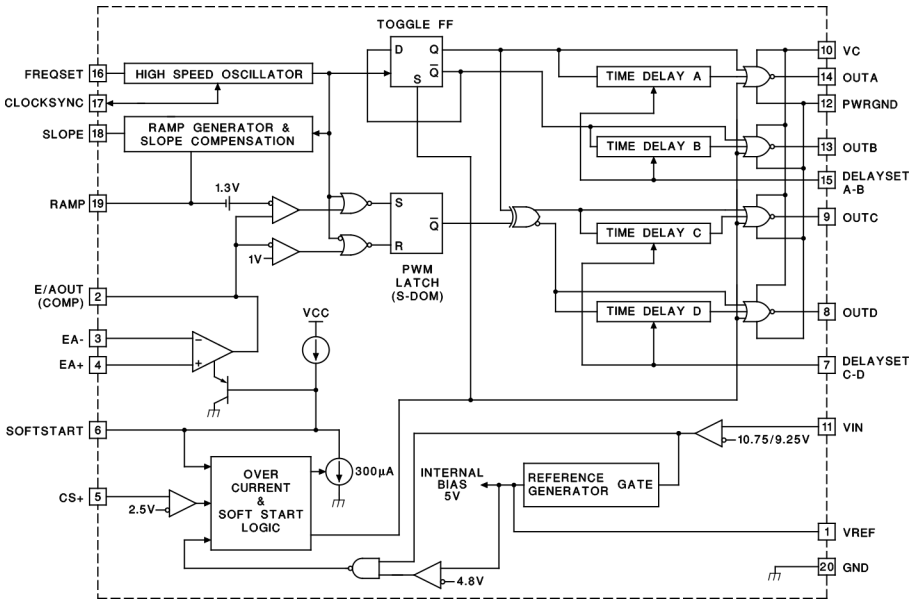
With the oscillator capable of operation at frequencies in excess of 2 MHz, overall switching frequencies to 1 MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UC1875-SP	LCCC (28)	11.43 mm × 11.43 mm
	CDIP (20)	24.20 mm × 6.92 mm
	CFP (24)	14.36 mm × 9.09 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2012) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Description (continued)

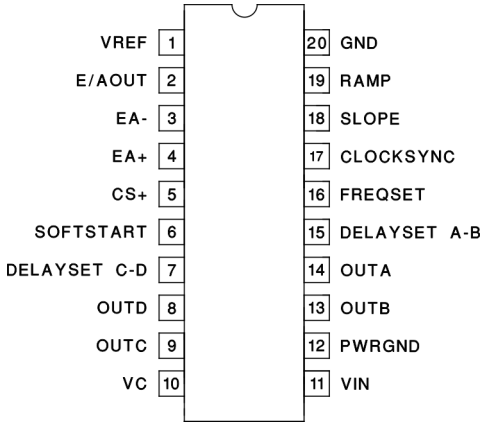
Protective features include an undervoltage lockout which maintains all outputs in an active-low state until the supply reaches a 10.75-V threshold. 1.5 hysteresis is built in for reliable, boot-strapped chip supply. Overcurrent protection is provided, and will latch the outputs in the OFF state within 70 ns of a fault. The current-fault circuitry implements full-cycle restart operation.

Additional features include an error amplifier with bandwidth in excess of 7 MHz, a 5-V reference, provisions for soft-starting, and flexible ramp generation and slope compensation circuitry.

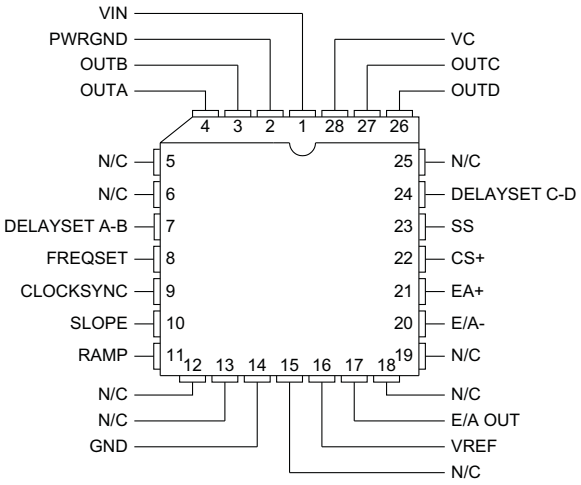
This device is available in hermetically sealed cerdip, surface mount, and ceramic leadless chip carrier packages for –55°C to 125°C operation.

6 Pin Configuration and Functions

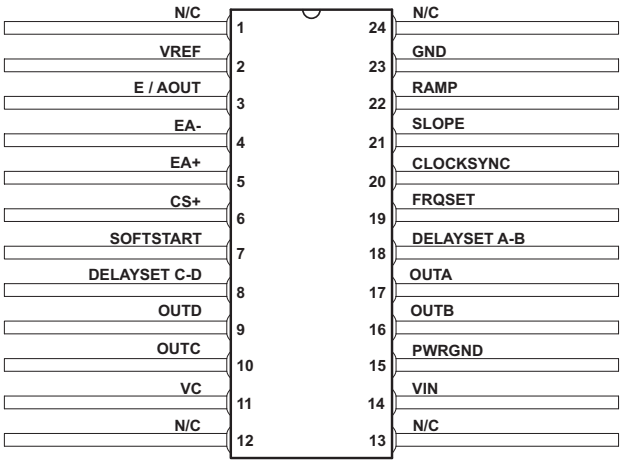
J Package
20-Pin CDIP
Top View



FK Package
28-Pin LCCC
Top View



W Package
24-Pin CFP
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	CDIP	LCCC	CFP		
CLOCK/ SYNC	17	9	20	I/O	Bi-directional clock and synchronization pin. Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point.
C/S+	5	22	6	I	The positive input to the current-fault comparator whose reference is set internally to fixed 2.5 V (separate from V_{REF}). When the voltage at this pin exceeds 2.5 V, the current-fault latch is set, the outputs are forced off and a SOFT START cycle is initiated. If a constant voltage above 2.5 V is applied to this pin the outputs are disabled from switching and held in a low state until the C/S (+) pin is brought below 2.5 V. The outputs may begin switching at 0 degrees phase shift before the SOFT START pin begins to rise, this condition will not prematurely deliver power to the load.
DELAY SET A/B	15	7	18	O	Output delay control. The users programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half bridges to accommodate differences in the resonant capacitor charging currents.
DELAY SET C/D	7	24	8	O	Output delay control. The users programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half bridges to accommodate differences in the resonant capacitor charging currents.
E/A+	4	21	5	I	This pin is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the E/A(-) pin.
E/A–	3	20	4	I	This pin is normally connected to the voltage divider resistors which sense the power supply output level.
E/A OUT (COMP)	2	17	3	O	Error amplifier output. This is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.
FREQ SET	16	8	19	O	Oscillator frequency set pin. A resistor and a capacitor from FREQ SET to GND will set oscillator frequency according to the following relationship: $f = 4/(R_{fSET} \times C_{RAMP})$.
GND	20	14	23	_	Signal ground. All voltages are measured with respect to ground (GND). The timing capacitor, on the FREQ SET pin, and bypass capacitor on the VREF pin, bypass capacitors on VIN and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.
N/C		5, 6, 12, 13, 15, 18, 19, 25	1, 12, 13, 24	_	No connection.
OUT A	14	4	17	O	The outputs are 2 A totem-pole drivers optimized for both MOSFET gates and level shifting transformers. The outputs operate as pair with a nominal 50% duty cycle. The A-B pair is intended to drive one half bridge in the external power stage and is synchronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.
OUT B	13	3	16	O	See OUT A description.
OUT C	9	27	10	O	See OUT A description.
OUT D	8	26	9	O	See OUT A description.
POWER GND	12	2	15	_	Power ground. VC should be bypassed with a ceramic capacitor from the VC pin to the section of the ground plane that is connected to PWR GND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a signal point to optimize noise rejection and minimize DC drops.

Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	CDIP	LCCC	CFP		
RAMP	19	11	22	I	Voltage ramp. This pin is the input to the pulse width modulator comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope: (dV/dT) = (sense voltage/R_{SLOPE} × C_{RAMP}).
SLOPE	18	10	21	I	Set ramp slope compensation. A resistor from this pin to V_{CC} will set the current used to generate the ramp. Connecting this resistor to the DC input line will provide voltage feed forward.
SOFT-START	6	23	7	O	SOFT START will remain at GND as long as VIN is below the UVLO threshold. SOFT START will be pulled up to about 4.8 V by an internal 9 μA current source when V_{IN} becomes valid (assuming a non-fault condition). In the event of a current-fault (C/S (+) voltage exceeding 2.5 V), SOFT START will be pulled to GND and then ramp to 4.8 V. If a fault occurs during the SOFT START cycle, the outputs will be immediately disabled and SOFT START must charge fully prior to resetting the fault latch. For paralleled controllers, the SOFT START pins may be paralleled to a single capacitor, but the change currents will be additive.
V_C	10	28	11	I	Output switch supply voltage. This pin supplies power to the drivers and their associated bias circuitry. Connect V_C to a stable source above 3 V for normal operation, above 12 V for best performance. This supply should be bypassed directly to the PWR GND pin with low ESR, low ESL capacitors.
V_{IN}	11	1	14	I	Primary chip supply voltage. This pin supplies power to the logic and analog circuitry on the integrated circuitry that is not directly associated with driving the output stages.
V_{REF}	1	16	2	I	This pin is an accurate 5 V voltage reference. This output is capable of delivering about 60 mA to peripheral circuitry and is internally short circuit current limited.

Table 1. Under Voltage Threshold (UVLO)

	UVLO TURN-ON	UVLO TURN-OFF	DELAY SET
UCC1875-SP	10.75V	9.25V	Yes

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage (VC, VIN)			20	V
Output current, source or sink	DC		0.5	A
	Pulse (0.5 μs)		3	A
Analog inputs	(Pins 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, 18, 19)	–0.3	5.3	V
Maximum junction temperature, J_{Tmax}			150	
Thermal Resistance, $R_{\theta JC(top)}$	J package		7	°C/W
	W package		5.4	
	FK package		5.6	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pin references are to 20-pin packages. All voltages are with respect to ground. Currents are positive into, negative out of the device terminals.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage Vin	10.75	12	18	V

7.4 Thermal Information

THERMAL METRIC (1)	UC1875-SP			UNIT
	J (CDIP)	FK (LCCC)	W (CFP)	
	20 PINS	28 PINS	24 PINS	
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	6.2	8.2	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

–55°C < T_A < 125°C. VC = VIN = 12 V, $R_{(FREQSET)}$ = 12 kΩ, $C_{(FREQSET)}$ = 330 pF, $R_{(SLOPE)}$ = 12 kΩ, $C_{(RAMP)}$ = 200 pF, $C_{(DELAYSET\ A-B)}$ = $C_{(DELAYSET\ C-D)}$ = 0.01 µF, $I_{(DELAYSET\ A-B)}$ = $I_{(DELAYSET\ C-D)}$ = –500 µA, T_A = T_J, unless otherwises stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT						
Start threshold				10.75	11.75	V
UVLO hysteresis			0.5	1.25	2	V
SUPPLY CURRENT						
I_{IN} Startup	VIN = 8 V, VC = 20 V, $R_{(SLOPE)}$ open, $I_{(DELAY)}$ = 0			150	600	µA
I_C Startup	VIN = 8 V, VC = 20 V, $R_{(SLOPE)}$ open, $I_{(DELAY)}$ = 0			10	100	µA
I_{IN}				30	44	mA
I_C				15	30	mA
VOLTAGE REFERENCE						
Output voltage	T_J = 25°C		4.92	5	5.08	V
Line regulation	11 V < VIN < 20 V			1	10	mV
Load regulation	I_{VREF} = –10 mA			5	20	mV
Total variation	Line, Load, Temperature		4.9		5.1	V
Noise Voltage	10 Hz to 10 kHz			50		µVrms
Long Term Stability	T_J = 125°C, 1000 hours			2.5		mV
Short circuit current	VREF = 0 V, T_J = 25°C			60		mA
ERROR AMPLIFIER						
Offset voltage				5	15	mV
Input bias current				0.6	3	µA
AVOL	1 V < $V_{(E/AOUT)}$ < 4 V		60	90		dB
CMMR	1.5 V < V_{CM} < 5.5 V		75	95		dB
PSRR	11 V < VIN < 20 V		85	100		dB
Output sink current	$V_{(E/AOUT)}$ = 1 V		1	2.5		mA
Output source current	$I_{(E/AOUT)}$ = 4 V			–1.3	–0.5	mA
Output voltage high	$I_{(E/AOUT)}$ = –0.5 mA		4	4.7	5	V
Output voltage low	$I_{(E/AOUT)}$ = 1 mA		0	0.5	1	V
Unity Gain BW	See (1)	01 device	5			MHz
		02 device	7			
Slew rate	See (1)		6	11		V/µs
PWM COMPARATOR						
RAMP offset voltage	T_J = 25°C (2)			1.3		V
Zero phase shift voltage	See (3)		0.55	0.9		V
PWM phase shift (4) (5)	$V_{(E/AOUT)}$ > (Ramp Peak + Ramp Offset)	01 device	98%	99.5%	102%	
		02 device	96%	100%	104%	
	$V_{(E/AOUT)}$ < Zero Phase Shift Voltage		0%	0.5%	2%	
Output skew (4) (5)	$V_{(E/AOUT)}$ > 1 V			5	±20	ns
Ramp to output delay (6) (1)				65	125	

(1) Not production tested.
(2) Ramp offset voltage has a temperature coefficient of about –4 mV/°C.
(3) The zero phase shift voltage has a temperature coefficient of about –2 mV/°C.
(4) Phase shift percentage (0% = 0 , 100% = 180) is defined as $\theta = \frac{200}{T}\phi\%$ where is the phase shift, and and T are defined in Figure 1. At 0% phase shift, is the output skew.
(5) Not production tested at –55·C.
(6) Ramp delay to output time is defined in Figure 1

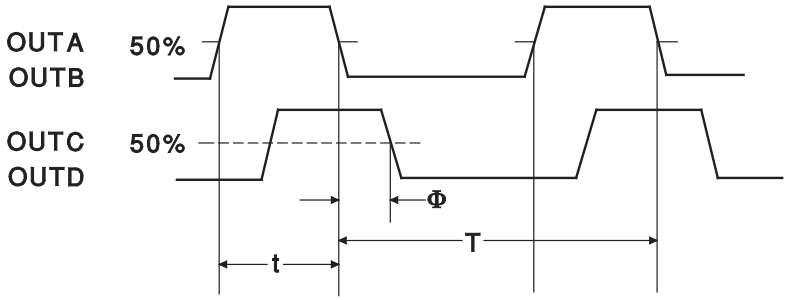
Electrical Characteristics (continued)

–55°C < T_A < 125°C. VC = VIN = 12 V, $R_{(FREQSET)}$ = 12 kΩ, $C_{(FREQSET)}$ = 330 pF, $R_{(SLOPE)}$ = 12 kΩ, $C_{(RAMP)}$ = 200 pF, $C_{(DELAYSET\ A\text{-}B)}$ = $C_{(DELAYSET\ C\text{-}D)}$ = 0.01 µF, $I_{(DELAYSET\ A\text{-}B)}$ = $I_{(DELAYSET\ C\text{-}D)}$ = –500 µA, T_A = T_J, unless otherwises stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OSCILLATOR						
Initial accuracy	T_A = 25°C	01 device	0.85	1	1.15	MHz
		02 device	0.85	1	1.19	
Voltage stability	11 V < VIN < 20 V			0.2%	2%	
Total variation	Line, Temperature		0.8		1.2	MHz
Sync pin threshold	T_J = 25°C			3.8		V
Clock out peak	T_J = 25°C			4.3		V
Clock out low	T_J = 25°C			3.3		V
Clock out pulse width	$R_{(CLOCKSYNC)}$ = 3.9 kΩ			30	100	ns
Maximum frequency (5)	$R_{(FREQUEST)}$ = 5 kΩ		2			MHz
RAMP GENERATOR/SLOPE COMPENSATION						
Ramp current, minimum	$I_{(SLOPE)}$ = 10 µA, $V_{(FREQSET)}$ = VREF			–11	–14	µA
Ramp current, maximum	$I_{(SLOPE)}$ = 1 mA, $V_{(FREQSET)}$ = VREF		–0.8	–0.95		mA
Ramp valley				0		V
Ramp peak - clamping level	$R_{(FREQSET)}$ = 100 kΩ		3.8	4.1	5	V
CURRENT LIMIT						
Input bias	V_{CS+} = 3 V			2	5	µA
Threshold voltage			2.4	2.5	2.6	V
Delay to output (1)				85	150	ns
SOFT START/RESET DELAY						
Charge current	$V_{(SOFTSTART)}$ = 0.5 V		–20	–9	–3	µA
Discharge current	$V_{(SOFTSTART)}$ = 1 V		120	230		µA
Restart threshold			4.3	4.7		V
Discharge level				300		mV
OUTPUT DRIVERS						
Output low level	I_{OUT} = 50 mA			0.2	0.4	V
Output high level	I_{OUT} = –50 mA			1.5	2.5	V
DELAY SET						
Delay set voltage	$I_{(DELAY)}$ = –500 µA		2.3	2.4	2.6	V
Delay time (1)	$I_{(DELAY)}$ = –250 µA (7)		150	250	600	ns

(7) Delay time can be programmed via resistors from the delay set pins to ground. Delay time = $\frac{62.5 \times 10^{-12}}{I_{(DELAY)}}$.

Where $I_{(DELAY)} = \frac{\text{Delay set voltage}}{R_{(DELAY)}}$. The Recommended range for $I_{(DELAY)}$ is 25 µA ≤ $I_{(DELAY)}$ ≤ 1 mA.



Duty Cycle = t/T, Period = T

T_{DHL} (A to C) = T_{DHL} (B to D) = Φ

Figure 1. Phase Shift, Output Skew and Delay Time Definitions

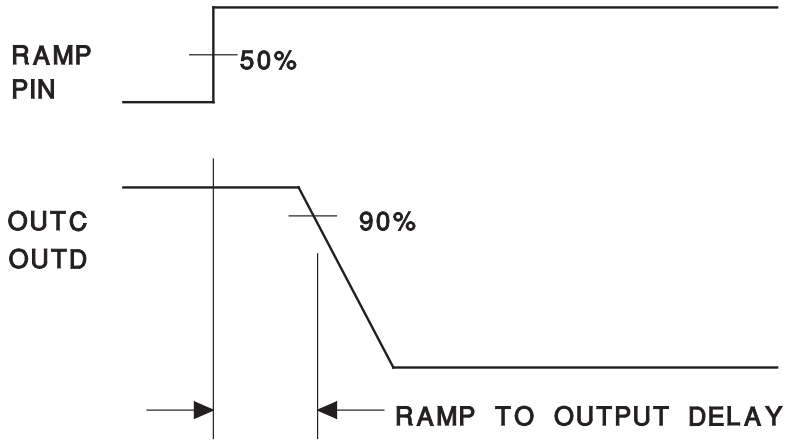


Figure 2. Ramp to Delay Output

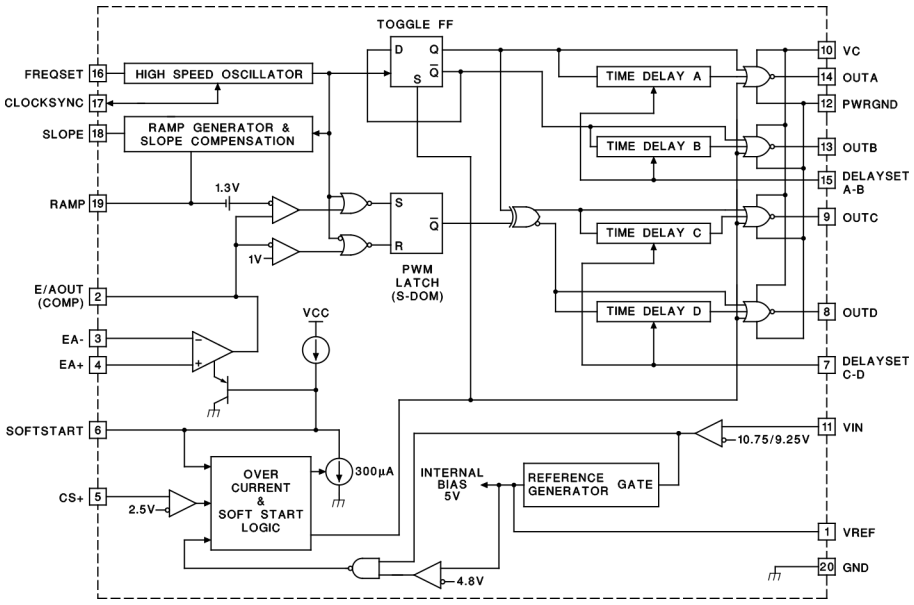
8 Detailed Description

8.1 Overview

Using the conventional full-bridge topology with phase-shifted control technique has already demonstrated its superiority in medium to high power, DC-to-DC power conversion. This control method provides well controlled dv/dt values and zero-voltage switching of all primary side semiconductors in the power stage over nearly all operating conditions. The major benefits offered by this approach are a simpler power stage than its hard switched counterpart, utilizing circuit parasitics instead of being penalized by them, improved efficiency and lower EMI level. These significant advantages are realized with a slightly more complex control algorithm.

The UC1875-SP implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This circuit may be configured to provide control in either voltage or current-mode operation, with a separate overcurrent shutdown for fast fault protection.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 CLKSYNC

(Bidirectional clock and synchronization pin): Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCKSYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

8.3.2 E/AOUT

(Error Amplifier Output): This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

Feature Description (continued)

8.3.3 CS+

(Current Sense): The non-inverting input to the current-fault comparator whose reference is set internally to a fixed 2.5 V (separate from VREF). When the voltage at this pin exceeds 2.5 V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5 V is applied to this pin the outputs are disabled from switching and held in a low state until the CS+ pin is brought below 2.5 V. The outputs may begin switching at 0 degrees phase shift before the SOFTSTART pin begins to rise -- this condition will not prematurely deliver power to the load.

8.3.4 FREQSET

(Oscillator Frequency Set pin): A resistor and a capacitor from FREQSET to GND will set the oscillator frequency.

8.3.5 DELSETA-B, DELSETC-D

(Output Delay Control): The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

8.3.6 EA–

(Error Amplifier Inverting Input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

8.3.7 EA+

(Error Amplifier Non-Inverting Input): This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the EA+ pin.

8.3.8 GND

(Signal Ground): All voltages are measured with respect to GND. The timing capacitor, on the FREQSET pin, any bypass capacitor on the VREF pin, bypass capacitors on VIN and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

8.3.9 OUTA – OUTD

(Outputs A-D): The outputs are 2 A totem-pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.

8.3.10 PWRGND

(Power Ground): VC should be bypassed with a ceramic capacitor from the VC pin to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

8.3.11 RAMP

(Voltage Ramp): This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{\text{Sense Voltage}}{R_{(SLOPE)} \times C_{(RAMP)}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation.

Feature Description (continued)

Because of the 1.3 V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of $R_{(SLOPE)}$ and $C_{(RAMP)}$.

8.3.12 SLOPE

(Set Ramp Slope/Slope Compensation): A resistor from this pin to VCC will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

8.3.13 SOFTSTART

(soft start): SOFTSTART will remain at GND as long as VIN is below the UVLO threshold. SOFTSTART will be pulled up to about 4.8 V by an internal 9 µA current source when VIN becomes valid (assuming a non-fault condition). In the event of a current-fault (CS+ voltage exceeding 2.5 V), SOFTSTART will be pulled to GND and them ramp to 4.8 V. If a fault occurs during the SOFTSTART cycle, the outputs will be immediately disabled and SOFTSTART must charge fully prior to resetting the fault latch.

For paralleled controllers, the SOFTSTART pins may be paralled to a single capacitor, but the charge currents will be additive.

8.3.14 VC

(Output Switch Supply Voltage): This pin supplies power to the output drivers and their associated bias circuitry. Connect VC to a stable source above 3 V for normal operation, above 12 V for best performance. This supply should be bypassed directly to the PWRGND pin with low ESR, low ESL capacitors

8.3.15 VIN

(Primary Chip Supply Voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12 V for normal operation. To ensure proper chip functionality, these devices will be inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

8.3.16 VREF

This pin is an accurate 5 V voltage reference. This output is capable of delivering about 60 mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled while VIN is low enough to force the chip into UVLO. The circuit is also in UVLO until VREF reaches approximately 4.75 V. For best results bypass VREF with a 0.1 µF, low ESR, low ESL, capacitor to the GND pin.

NOTE

When VIN exceeds the UVLO threshold the supply current (I_{IN}) will jump from about 100 µA to a current in excess of 20 µA. If the UC1875-SP is not connected to a well bypassed supply, it may immediately enter UVLO again.

8.4 Device Functional Modes

The UC1875-SP, with its 2-A peak current capability, is prepared for direct drive of the gates or gate-drive transformers of the most commonly used power switches. The UC1875-SP can be configured as a voltage-mode or current-mode controller.

The diagonal bridge switches are driven together in a conventional full-bridge converter, which alternately places the transformer primary across the input supply, V_{IN}, for some period of time, t_ON as shown in Figure 14. Power is only transferred to the output section during the ON times of the switches, which corresponds to a specific duty cycle when operated at a fixed frequency. Additionally, the complete range of required duty cycles is unique to the application, and can be estimated from the power supply input and output voltage specifications.

Rather than driving both of the diagonal full bridge switches together, a deliberate delay can be introduced between their turn-on commands with the phase-shifted approach. This delay is adjusted by the voltage loop of the control circuitry, and essentially results as a phase shift between the two drive signals. The effective duty cycle is controlled by varying the phase shift between the switch drive commands as shown in Figure 12.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Undervoltage Lockout Section

When power is applied to the circuit and VIN is below the upper UVLO threshold, I_{IN} will be below 600 µA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low. When VIN exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shut-down mode until the output of the reference, VREF, exceeds 4.75 V.

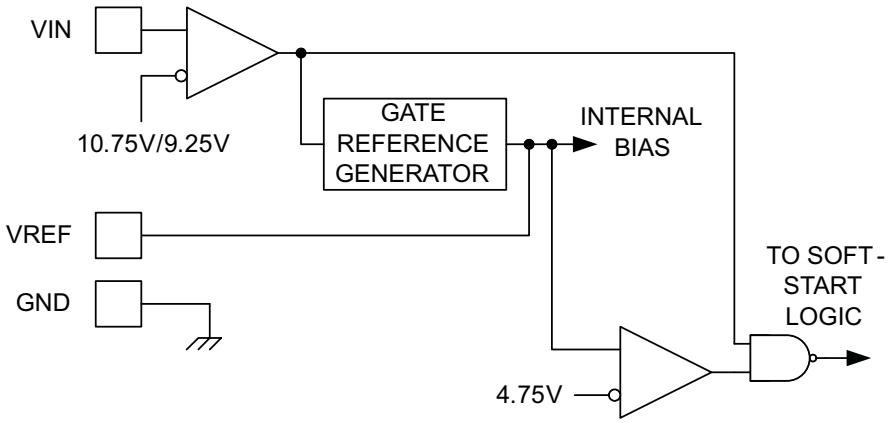


Figure 3. Undervoltage Circuit

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQSET pin.

Application Information (continued)

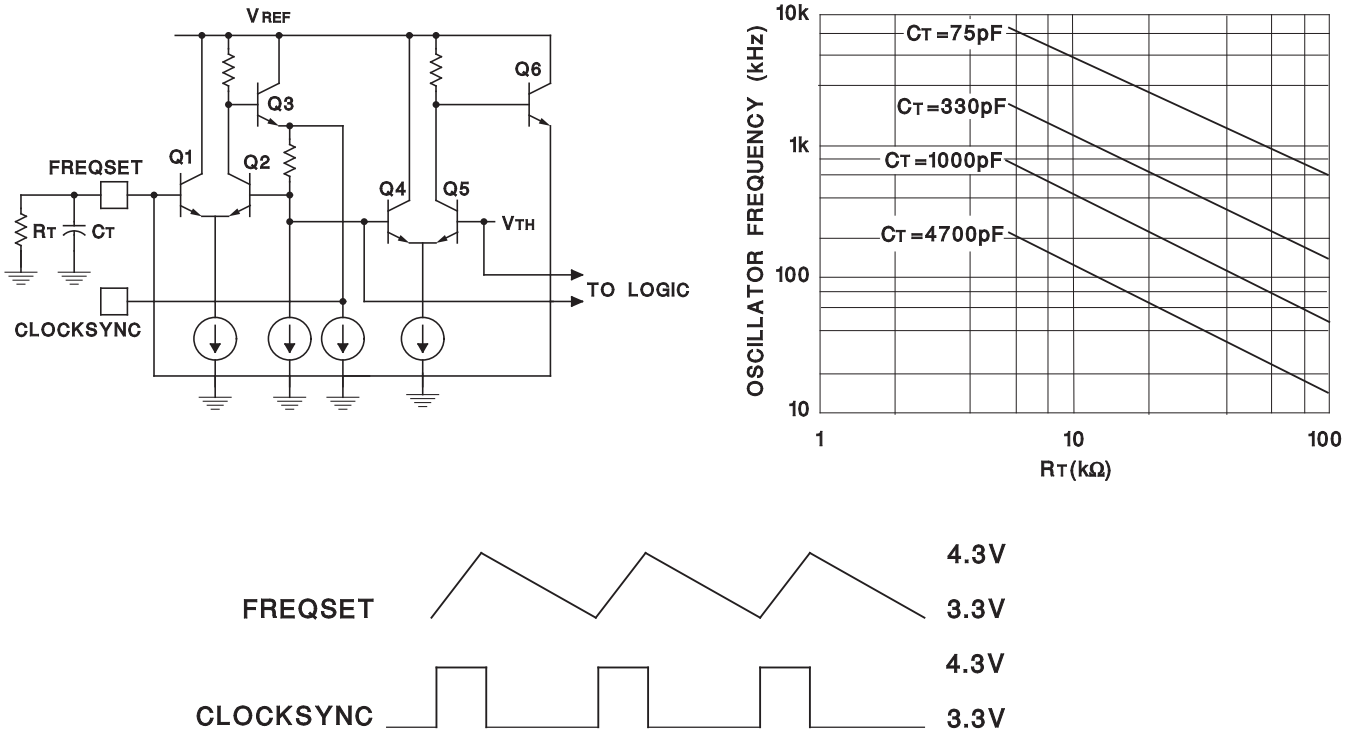


Figure 4. Simplified Oscillator Schematic

9.1.2 Synchronizing the Oscillator

The CLOCKSYNC pin of the oscillator may be used to synchronize multiple UC1875-SP device by connecting the CLOCKSYNC of each UC1875-SP to the others:

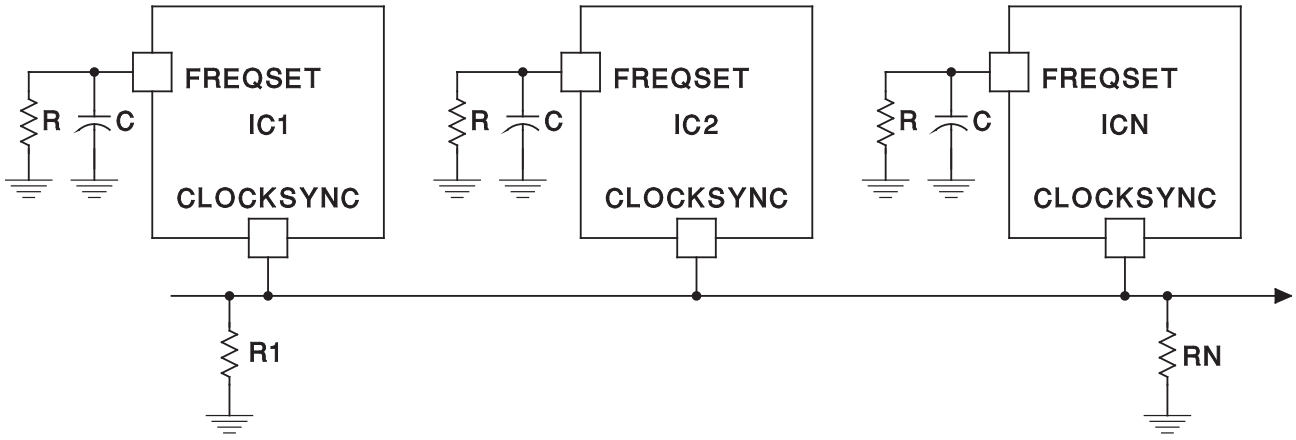


Figure 5. Synchronizing Multiple UC1875-SP

ALL ICs will sync to the chip with the fastest local oscillator.

R1 and RN may be needed to keep sync pulse narrow due to capacitance on line.

R1 and RN may also be needed to properly terminate $R_{(SYNC)}$ line.

Application Information (continued)

9.1.3 Syncing to External TTL/CMOS

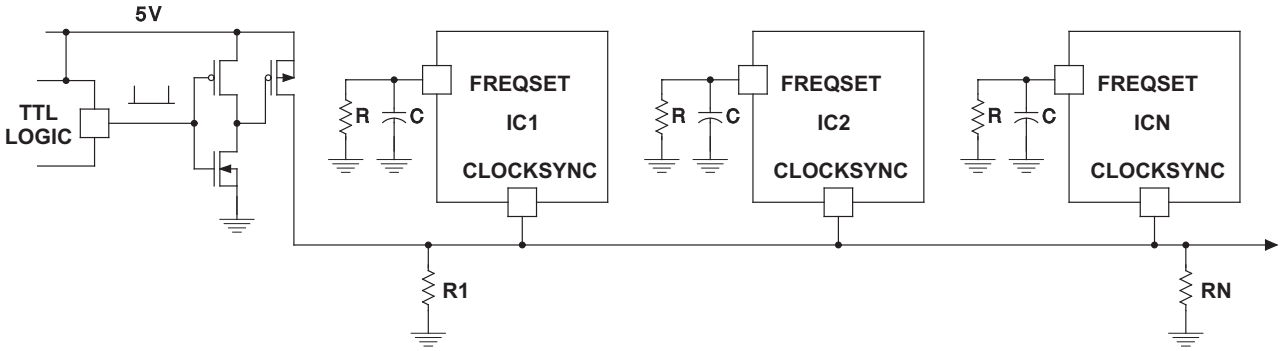


Figure 6. Synchronizing UC1875-SP

ICs will sync to the fastest chip or TTL clock if it is higher frequency.

R1 and RN may be needed to keep sync pulse narrow due to capacitance on line.

R1 and RN may also be needed to properly terminate $R_{(SYNC)}$ line.

Although the UC1875-SP has a local oscillator frequency, the device will synchronize to the fastest oscillator driving the CLOCKSYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.

Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in Figure 6.

Capacitive loading on the CLOCKSYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCKSYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R1, RN.

Application Information (continued)

9.1.4 Delay Blocks and Output Stages

In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.

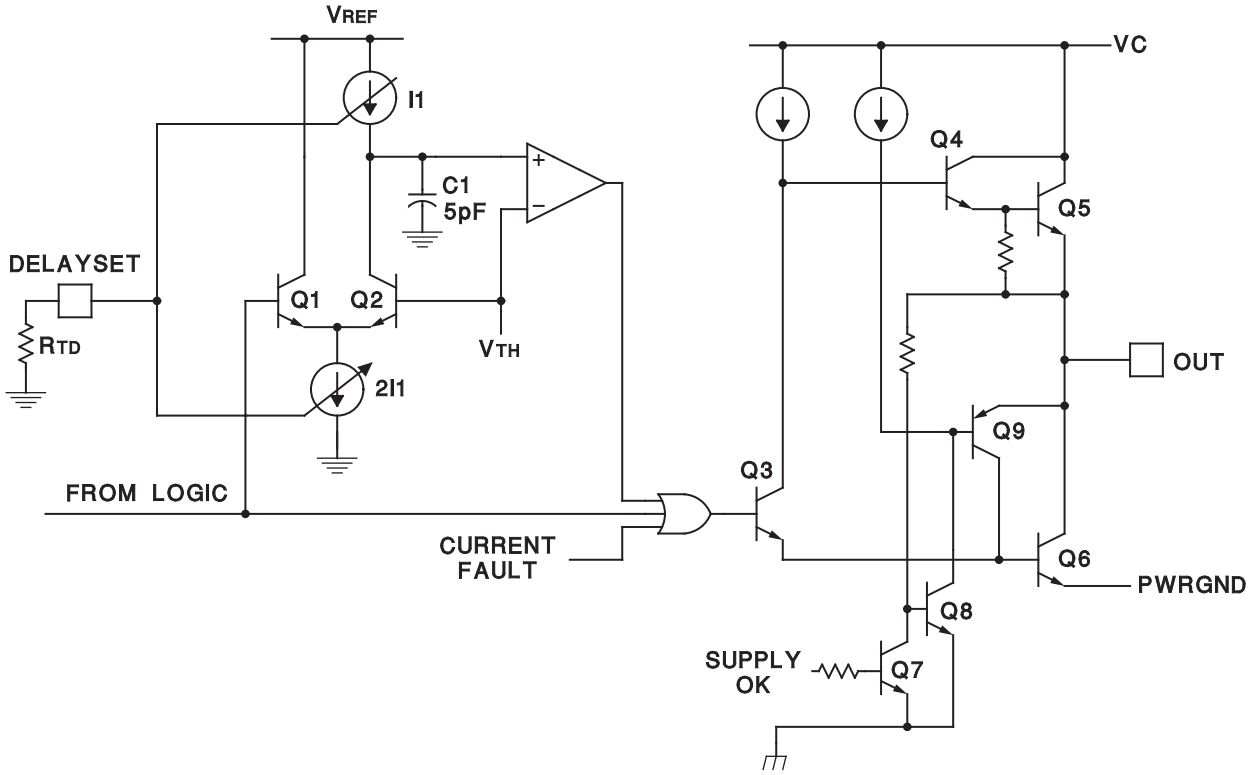


Figure 7. UC1875-SP Output Stage

The delay providing the dead-time is accomplished with C1 which must discharge to V_{TH} before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, R_{TD}. The voltage on the Delay Set pins is internally regulated to 2.5 V and the range of dead time control is from 50 to 200 nanoseconds.

NOTE

There is no way to disable the delay circuitry, and the delay time must be programmed.

Application Information (continued)

9.1.5 Output Switch Orientation

The four outputs of the UC1875-SP interfaces to the full bridge converter switches as shown in Figure 8

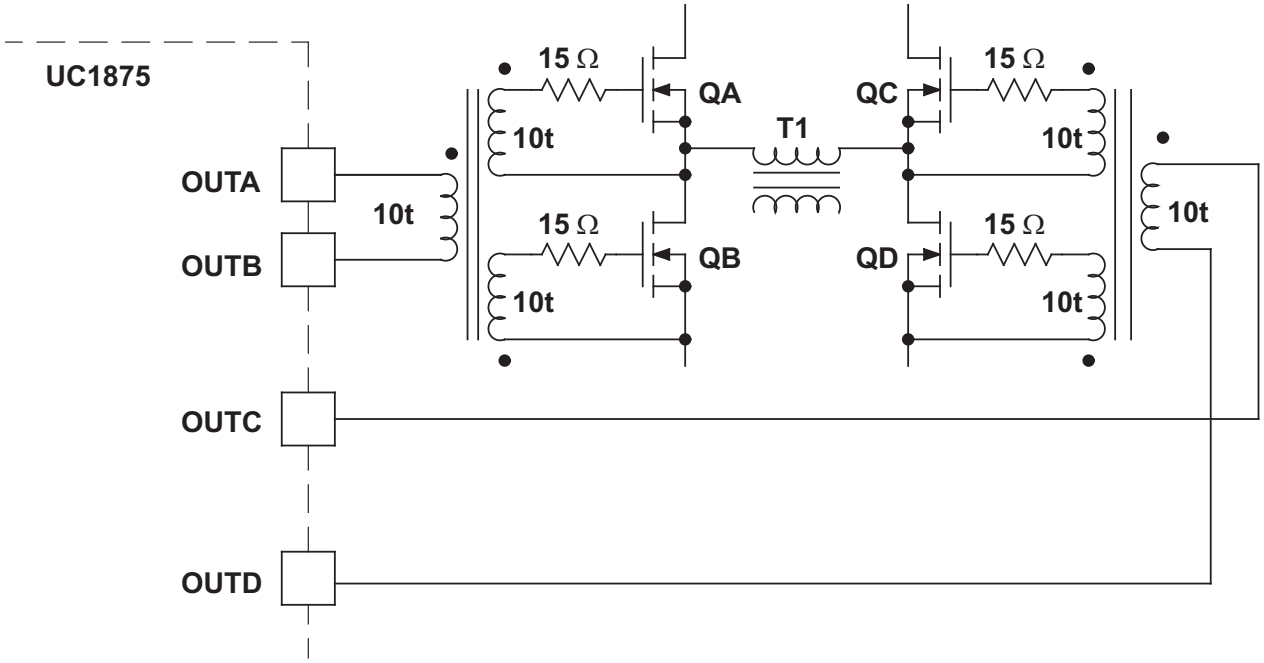


Figure 8. 3 Winding Bifilar, AWG 30 Kynar Insulation

9.1.6 Fault/Soft Start

The fault control circuitry provides two forms of power shutdown:

- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFTSTART pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT-START capacitor.

The fault logic insures that a continuous fault will institute a low frequency “hiccup” retry cycle by forcing the SOFT-START capacitor to charge through its full cycle between each restart attempt.

Application Information (continued)

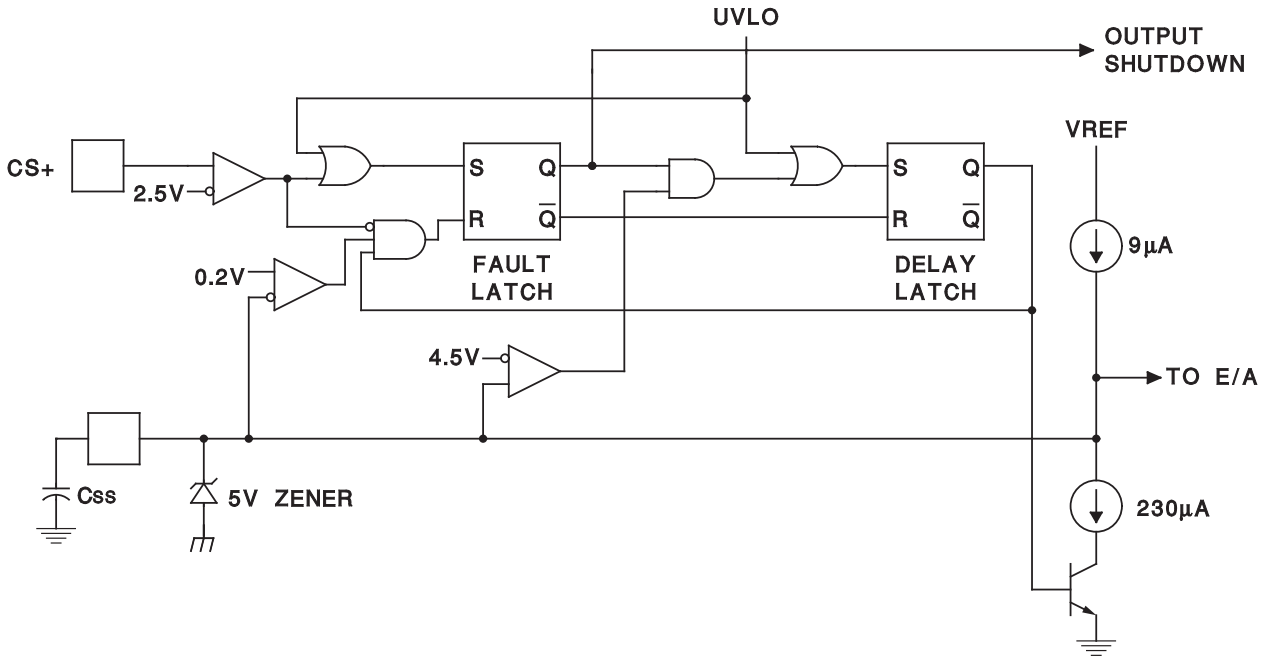


Figure 9. Fault and Restart

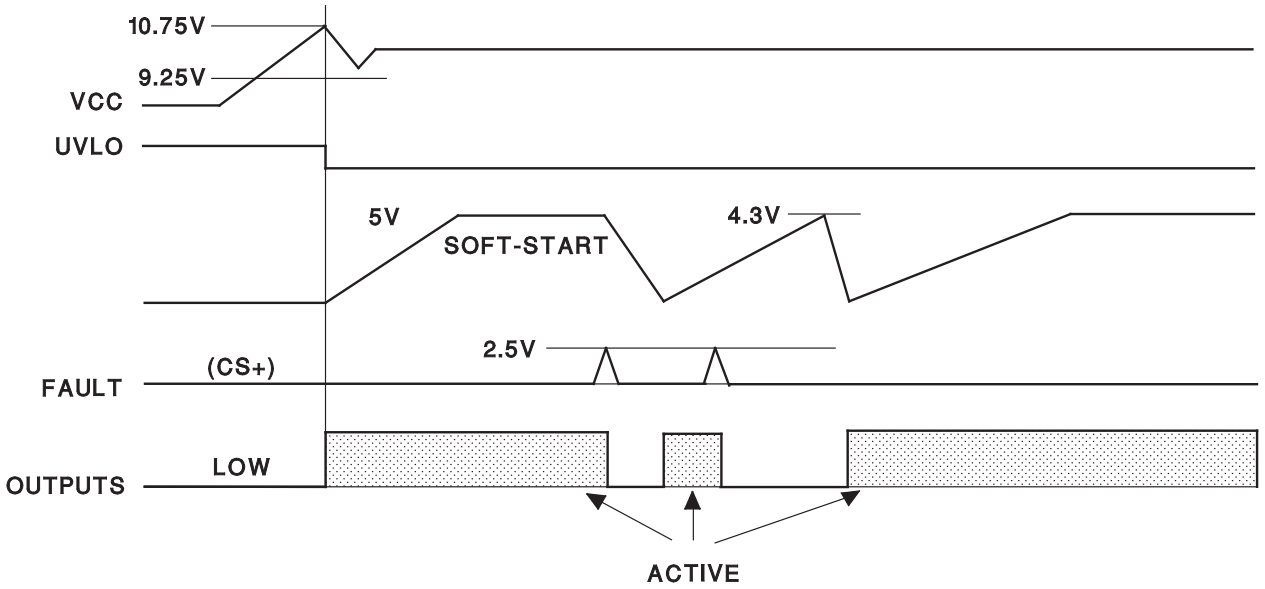


Figure 10. Fault Restart Waveform

Application Information (continued)

9.1.7 Slope/Ramp Pins

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

Figure 11 shows a voltage-mode configuration. With $R_{(SLOPE)}$ tied to a stable voltage source, the waveform on $C_{(RAMP)}$ will be a constant-slope ramp, providing conventional voltage-mode control. If $R_{(SLOPE)}$ is connected to the power supply input voltage, a variable-slope ramp will provide voltage feedforward.

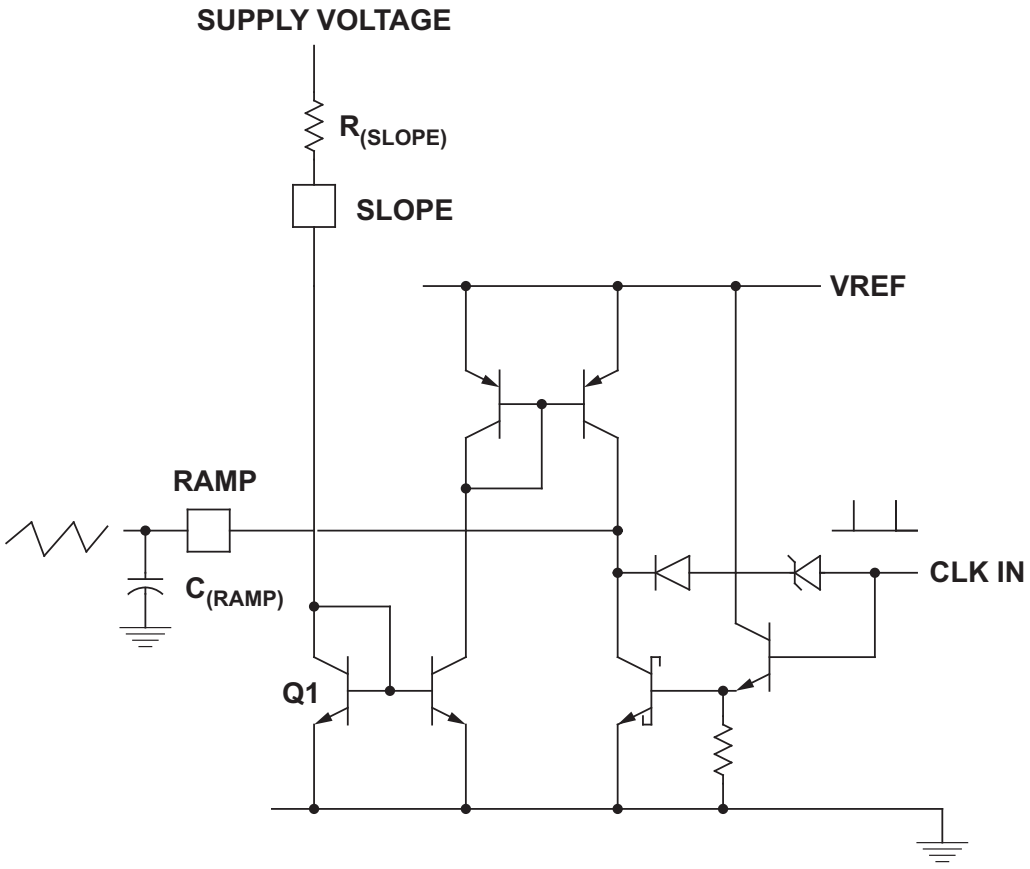


Figure 11. Voltage Mode Operation

1. Simple voltage mode operation achieved by placing $R_{(SLOPE)}$ between VIN and SLOPE
2. Voltage Feedforward achieved by placing $R_{(SLOPE)}$ between supply voltage and SLOPE pin of UC1875-SP.

RAMP:

$$\frac{dV}{dT} = \frac{V_{Rslope}}{R_{SLOPE} \times C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator.

9.2 Typical Application

A typical application for the phase-shifted bridge is to convert high-input voltage to low-output voltage while also providing system isolation.

Using this phase-shifted technique, two of the switches in series with the transformer can be ON, yet the applied voltage to the transformer is zero. These are not diagonal switches of the full-bridge converter, but either the two upper or two lower switches. In this mode, the transformer primary is essentially short circuited and clamped to the respective input rail. Primary current is maintained at its previous state because there is no voltage available for reset to take place. This deadband fills the void between the resonant transitions and power-transfer portion of the conversion cycle. Switches can be held in this state for a certain period of time which corresponds to the required off time for that particular switching cycle.

When the correct one of these switches is later turned off, the primary current flows into the switch output capacitance (Coss) causing the switch drain voltage to resonate to the opposite input rail. This aligns the opposite switch of the particular bridge leg with zero voltage across it, enabling zero-voltage switching when it is turned ON.

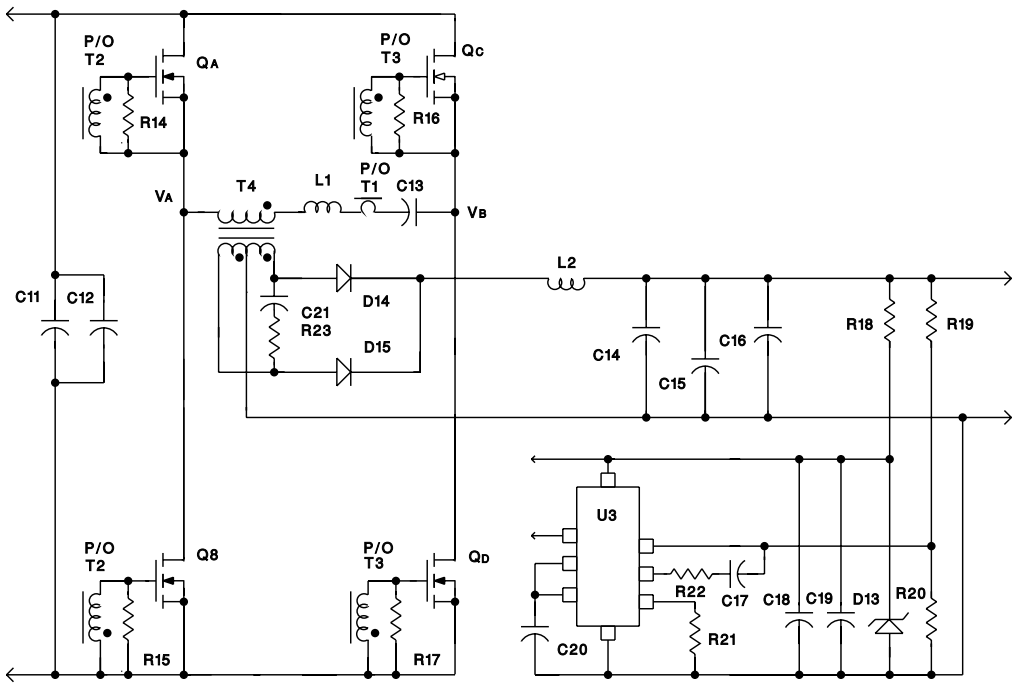


Figure 12. Phase-Shifted PWM Converter Control and Output Circuit Schematic

Typical Application (continued)

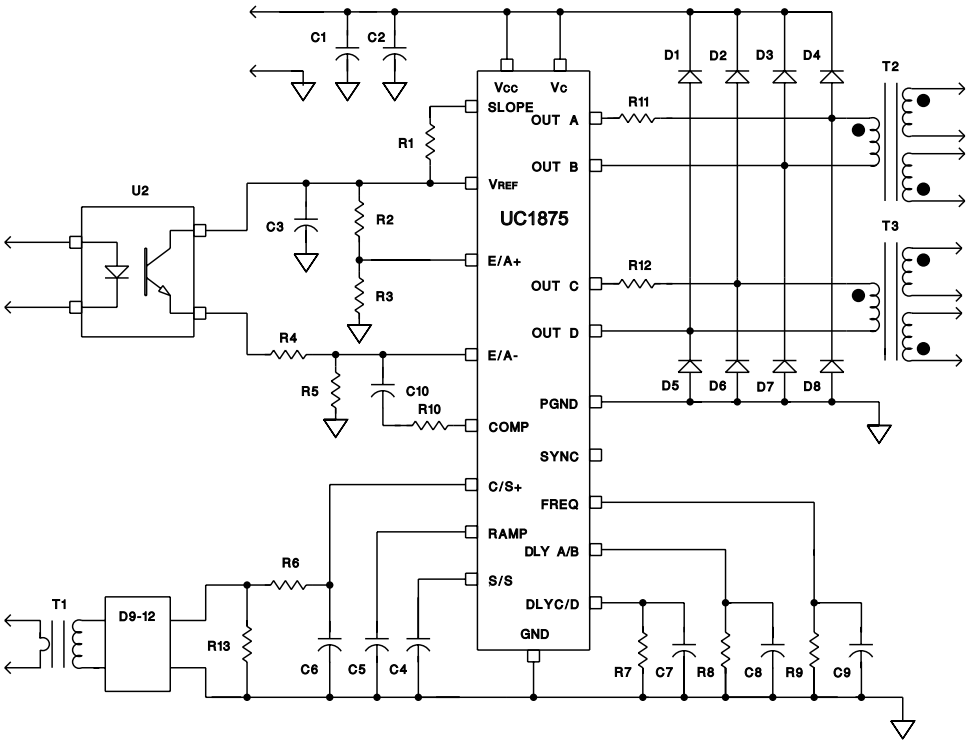


Figure 13. Phase Shifted PWM Converter Control and Drive Circuit Schematic

9.2.1 Design Requirements

Table 2 lists the requirements for this application. Further requirements can be found in *Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller* (SLUA107).

Table 2. Design Parameters

PARAMETER	VALUE
Vin	48 V
Vout	5 V at 40 A

9.2.2 Detailed Design Procedure

9.2.2.1 Phase-Shifted Fundamentals

Switches within the phase-shifted full bridge converter will be utilized differently than those of its non-resonant counterpart. Instrumental to this technique is the use of the parasitic elements of the MOSFET switch's construction. The internal body diode and output capacitance (Coss) of each device (in conjunction with the primary current) become the principal components used to accomplish and commutate the resonant transitions.

9.2.2.2 Circuit Schematic and Description

A more detailed operation of the phase-shifted converter operation follows a description of the circuit elements. The circuit schematic of this technique is shown in Figure 14, including voltage and current designations.

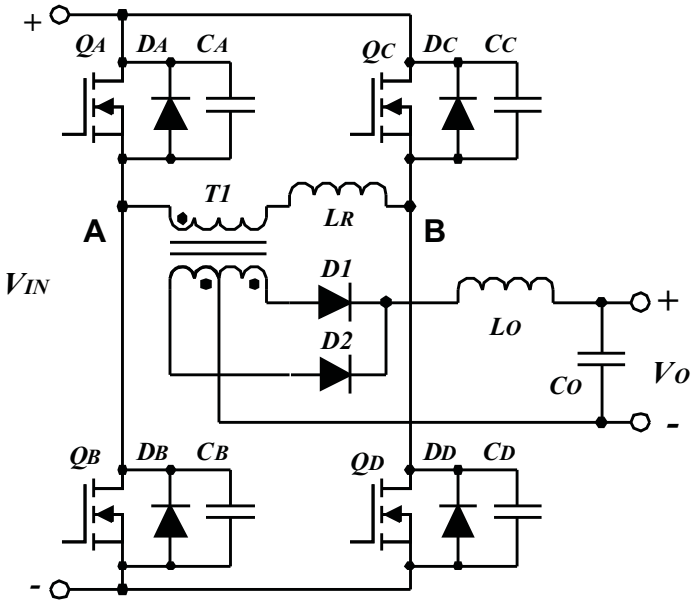


Figure 14. Phase-Shifted PWM Switch Orientation

The basic circuit is comprised of four switches labeled QA through QD and is divided up into two “legs”, the right and left hand legs. Each switch is shown shunted by its body diode (DA through DD) and parasitic output capacitance, (CA through CD). These have been identified separately to clarify the exact elements and current paths during the conversion interval.

A detailed model of the transformer primary section is presented which separately indicates the leakage and magnetizing inductances and currents of the primary. The reflected secondary contributors to primary current are also shown for completeness, and divided into two components. The DC primary current (IP) is the secondary DC output current divided by the transformer turns ratio (N). The secondary AC current should also be accounted for by multiplying the output inductance by the turns ratio squared (N2), or dividing the secondary AC ripple current ISEC(ac) by the turns ratio (N) as shown in Figure 15.

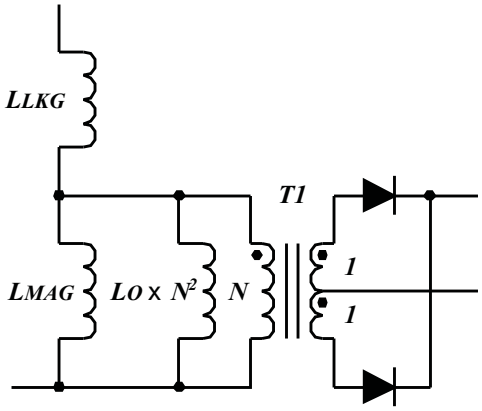


Figure 15. Primary Magnetic Components

9.2.2.3 Initial Conditions (Time: t = t(0))

The description of the Phase Shifted operation will begin with the conclusion of one power transfer cycle. This occurs when the transformer had been delivering power to the load and two of diagonal switches of the converter were conducting. The initial current flowing in the primary can be designated as IP(t(0)).

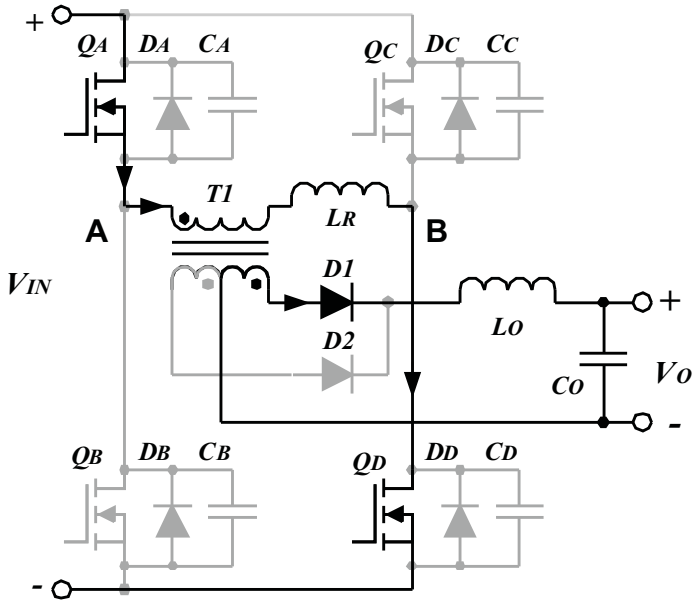


Figure 16. Initial Conditions

9.2.2.4 Right Leg Resonant Transition Interval (Time: t(0) < t < t(1))

The primary current flowing at time t(0) is equal to IP(t(0)) and was being conducted through the diagonal set of transistors QA in the upper left hand corner of the bridge and transistor QD in the lower right. Instantly, at time t(0) switch QD is turned off by the control circuitry which begins the resonant transition of the right hand leg of the converter.

The primary current flowing is maintained nearly constant at IP(t(0)) by the resonant inductance of the primary circuit, often referred to as the transformers leakage inductance. Since an external series inductance can be added to alter the effective leakage inductance value, this presentation will refer to the lumped sum of these inductors as the resonant inductance, LR. In a practical application it may be difficult to accurately control the transformers leakage inductance within an acceptable ZVS range, necessitating an external “shim” inductor to control the accuracy. It’s also possible that the transformer leakage inductance can be too low to provide the desired transition times for the application so an external inductor can be introduced to modify the resonant inductance.

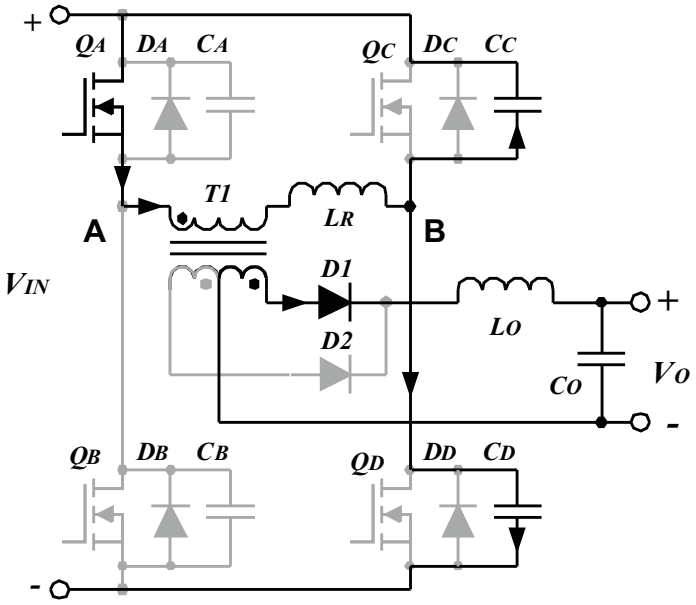


Figure 17. Right Leg Transition

With switch QD turned off, the primary current continues to flow using the switch output capacitance, CD to provide the path. This charges the switch capacitance of QD from essentially zero volts to the upper voltage rail, Vin+. Simultaneously, the transformer capacitance (Cxfmr) and the output capacitance of switch QC is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions switch QC with no drain to source voltage prior to turn-on and facilitates lossless, zero voltage switching.

The primary current causing this right leg transition can be approximated by the full load primary current of IP(t(0)). The small change due to the barely resonant circuit contribution is assumed to be negligible in comparison to the magnitude of the full load current.

During this right leg transition the voltage across the transformers primary has decreased from VIN to zero. At some point in the transition the primary voltage drops below the reflected secondary voltage, VO x N. When this occurs the primary is no longer supplying full power to the secondary and the output inductor voltage changes polarity. Simultaneously, energy stored in the output choke begins supplementing the decaying primary power until the primary contribution finally reaches zero.

Once the right leg transition has been completed there is no voltage across the transformer primary. Likewise, there is no voltage across the transformers secondary winding and no power transferred, assuming ideal conditions. Note that the resonant transition not only defines the rate of change in primary and secondary voltages dV/dt, but also the rate of change in current in the output filter network, dI/dt.

9.2.2.5 Clamped Freewheeling Interval (Time: t(1) < t < t(2))

Once the right leg transition is complete the primary current free wheels through transistor QA and the body diode of switch QC. The current would remain constant until the next transition occurs assuming that the components were ideal. Switch QC can be turned on at this time which shunts the body diode with the FET Rds(on) switch impedance thus lowering conduction losses. Although current is flowing opposite to the normal convention (source to drain) the channel of QC will conduct and divide the current between the switch and body diode.

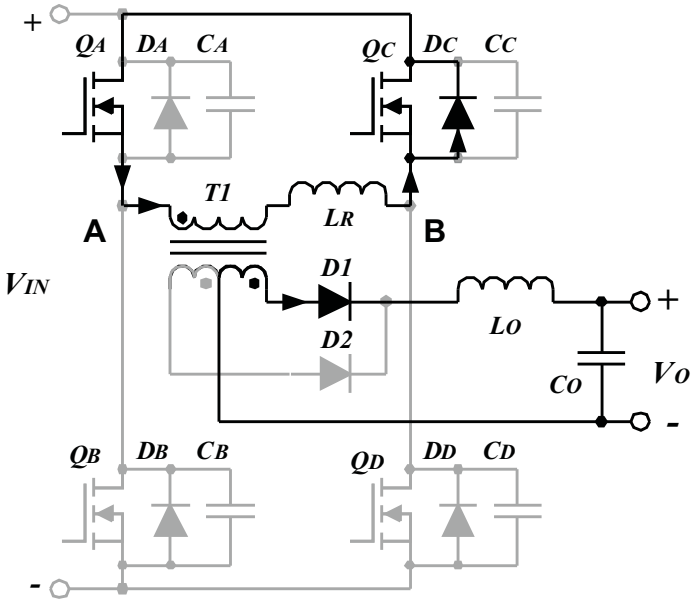


Figure 18. Clamped Free Wheeling Interval

9.2.2.6 Left Leg Transition Interval (Time: t(2) < t < t(3))

At time t(2) a residual current was flowing in the primary of the transformer which is slightly less than IP(t(0)) due to losses. Switch QC has been previously turned ON and switch QA will now be turned OFF. The primary current will continue to flow but the path has changed to the output capacitance (CA) of switch QA instead of its channel. The direction of current flowing causes the drain to source voltage of switch QA to increase and lowers its source from the upper to lower rail voltage. Just the opposite conditions have occurred to switch QB which previously had the full input across its terminals. The resonant transition now aligns switch QB with zero voltage across it, enabling lossless switching to occur.

Primary current continues to flow and is clamped by the body diode of switch QB, which is still OFF. This clamping into a short circuit is a necessary condition for fixed frequency, zero voltage switching. Once switch QB is turned ON, the transformer primary is placed across the input supply rails since switch QC is already ON and will begin to transfer power. Although zero voltage switching has already been established, turning ON switch QB the instant it reaches zero voltage will cause variable frequency operation.

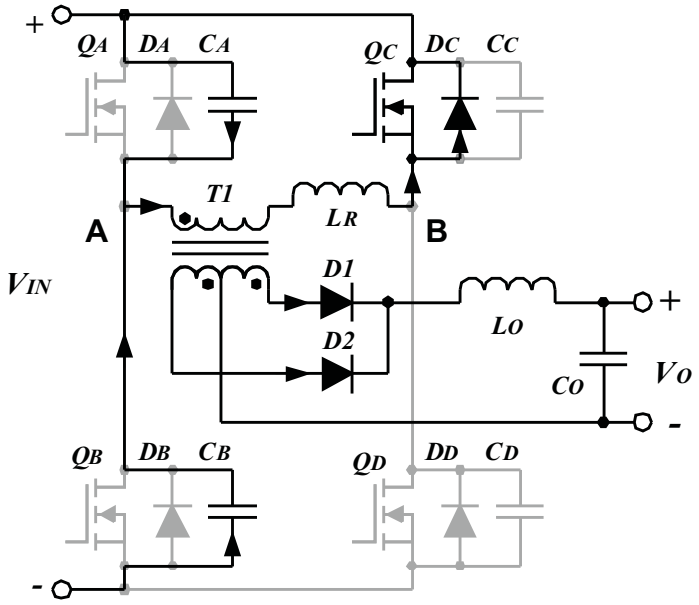


Figure 19. Left Leg Transition

Note that this left leg transition will require more time to complete than the right leg transition. Conduction losses in the primary switches, transformer winding and interconnections result in a net DC voltage drop due to the flowing primary current. Energy stored in the series resonant inductor and magnetizing inductance is no longer ideally clamped to zero voltage. This loss, in addition to the losses incurred during the previous transition, reduce the primary current below its initial IP(t(0)) value, thus causing a longer left leg transition time than the right leg.

Unlike conventional power conversion, one transistor in the diagonal pair of the phase shifted full bridge converter is ON just before power is transferred which simplifies the gate drive. An additional benefit is realized by designating these commutating switches as the high side switches of the converter, usually far more difficult to drive than their lower side counterparts.

9.2.2.7 Power Transfer Interval (Time: t(3) < t < t(4))

This interval of the phase shifted cycle is basically identical to that of conventional square wave power conversion. Two diagonal switches are ON which applies the full input voltage across the transformer primary. Current rises at a rate determined by VIN and the series primary inductance, however starts at a negative value as opposed to zero. The current will increase to a DC level equal to the output current divided by the turns ratio, IO/N. The two time variant contributors to primary current are the magnetizing current (IMAG) and the output inductor magnetizing contribution reflected to the primary, LO x N2. The exact switch ON time is a function of VIN, VO and N the transformer turns ratio, just as with conventional converters.

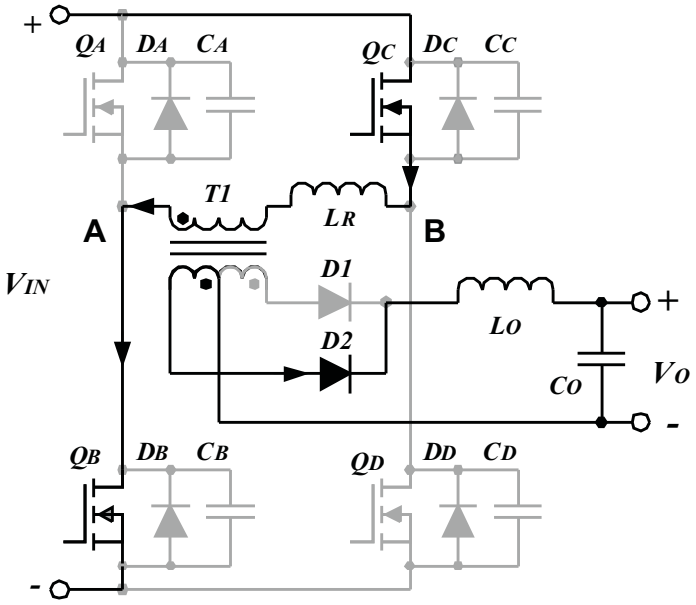


Figure 20. Power Transfer Interval

9.2.2.8 Switch Turn Off (Time: t(4))

One switching cycle is concluded at time t(4) when QC the upper right hand corner switch is turned OFF. Current stops flowing in QC's semiconductor channel but continues through the parasitic output capacitance, CC. This increases the drain-to-source voltage from essentially zero to the full input supply voltage, VIN. The output capacitance of the lower switch in the right hand leg (QD) is simultaneously discharged via the primary current. Transistor QD is then optimally positioned for zero voltage switching with no drain-to-source voltage. The current during this interval is assumed to be constant, simplifying the analysis. In actuality, it is slightly resonant as mentioned in the left leg transition, but the amplitude is negligible in comparison to the full load current. The power conversion interval is concluded at this point and an identical analysis occurs as for the opposite diagonal switch set which has thoroughly been described for the switch set QA and QD.

9.2.2.9 Resonant Tank Considerations

The design of the resonant tank begins with the selection of an acceptable switching frequency; one selected to meet the required power density. Second, the maximum transition time must also be established based on achievable duty cycles under all operating conditions. Experience may provide the best insight for acceptable results.

NOTE

The maximum transition time will occur during the converters left leg transition operating at the minimum output load current.

9.2.2.10 Resonant Circuit Limitations

Two conditions must be met by the resonant circuit at light load, and both relate to the energy stored in the resonant inductor. One, there must be enough inductive energy stored to drive the resonant capacitors to the opposite supply rail. Two, this transition must be accomplished within the allocated transition time. Lossy, non-zero voltage switching will result if either, or both are violated. The first condition will always be met when the latter is used as the resonant circuit limitation.

Designers can argue that some switching loss may be of little consequence in a practical application at very light loads - especially considering that there is a significant benefit at heavy loads. While this may be a pragmatic approach in many applications, and a valid concern, this presentation will continue using the fully lossless mode as the ultimate design goal.

The stored inductive energy requirement and specified maximum transition time have also defined the resonant frequency (ωR) of the tank circuit. Elements of this tank are the resonant inductor (LR) and capacitor (CR), formed by the two switch output capacitors, also in parallel with the transformer primary capacitance Cxfmr. The maximum transition time cannot exceed one-fourth of the self resonant period, (four times the self resonant frequency) to satisfy the zero voltage switching condition.

The resonant tank frequency, ωR:

$$\omega_R = \frac{1}{\sqrt{L_R \times C_R}} \quad (1)$$

$$t_{MAX}\ \text{transistion} = \frac{\pi}{2 \times \omega_R} \quad (2)$$

Coss, the specified MOSFET switch output capacitance will be multiplied by a 4/3 factor to accommodate the increase caused by high voltage operation. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to 8/3 x Coss. Transformer capacitance (Cxfmr) must also be added as it is NOT negligible in many high frequency applications.

The resonant capacitance, CR:

$$C_R = \frac{8}{3} \times C_{OSS} + Cxfmr \quad (3)$$

The capacitive energy required to complete the transition, W(CR) is:

$$W(C_R) = \frac{1}{2} \times C_R \times VPri^2 \quad (4)$$

This energy can also be expressed as:

$$W(C_R) = \left(\frac{4}{3} \times C_{OSS} + \frac{1}{2} Cxfmr \right) \times V_{IN}{}^2 \quad (5)$$

9.2.2.11 Stored Inductive Energy

The energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output and transformer capacitances of the leg in transition within the maximum transition time.

Inside the transformer, all of the energy is stored in the leakage inductance since the secondary current has clamped the transformers primary voltage to essentially zero. This causes high circulating primary current (as shown in figure 8) in the physical winding but has no effect on the stored energy used to perform the ZVS transition. More detail about the tradeoffs and design optimization is presented in the Design Procedure.

The energy stored in the resonant inductor, LR:

$$W(L_R) = \frac{1}{2} \times L_R \times I_{PRI}{}^2 \quad (6)$$

9.2.2.12 Resonant Circuit Summary

There are several ways to arrive at the solutions for the resonant inductor value and minimum primary current required for any application. Each of these is based upon the following fundamental relationships. The resonant tank frequency must be at least four times higher than the transition time to fully resonate within the maximum transition time tMAX at light load.

$$T_{RES} = 4 \times t_{MAX} \quad (7)$$

$$f_{RES} = \frac{1}{T_{RES}} \quad (8)$$

Where:

$$\omega_R = 2 \times \pi \times f_{RES} \quad (9)$$

$$\omega_R = \frac{2 \times \pi}{T_{RES}} \tag{10}$$

Reorganizing and combining these relationships;

$$\omega_R = \frac{2 \times \pi}{4 \times t_{MAX}} \tag{11}$$

$$\omega_R = \frac{\pi}{2 \times t_{MAX}} \tag{12}$$

The resonant radian frequency (ωR) is related to the resonant components by the equation:

$$\omega_R = \frac{1}{\sqrt{L_R \times C_R}} \tag{13}$$

Both sides of this can be squared to simplify the calculations and reorganized to solve for the exact resonant inductor value.

$$L_R = \frac{1}{\omega_R^2 \times C_R} \tag{14}$$

Previously outlined relationships for ωR and CR can be introduced to result in the following specific equation.

$$L_R = \frac{1}{\left(\frac{\pi}{2 \times t_{MAX}}\right)^2 \times \left(\frac{8}{3} \times C_{OSS} + \frac{1}{2} Cxfmr\right)} \tag{15}$$

NOTE

This figure indicates the exact resonant inductor value required to satisfy only the task of resonant transitions. This resonant inductor is in series with the transformer primary hence also defines the maximum primary current slew rate, dI/dt as a function of input voltage.

$$\frac{dI_{PRI}}{dt} = \frac{V_{IN}}{L_R} \tag{16}$$

If the resonant inductor value is too large it may take too long to reach the necessary load current within the conversion cycle. The calculated inductor value satisfies the light load condition, however full load operation must also be evaluated. Details of possible solutions to this are highlighted in the Practical Applications section of this paper.

9.2.2.13 Stored Energy Requirements

As detailed, the energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. The governing equations are summarized below.

$$\frac{1}{2} \times L_R \times I_{PRI(min)}^2 = \frac{1}{2} \times C_R \times V_{IN(max)}^2 \tag{17}$$

$$L_R \times I_{PRI(min)}^2 > C_R \times V_{IN(max)}^2 \tag{18}$$

Since CR and VIN are known or can be estimated for a given application, this term becomes a constant and LR has been quantified.

9.2.2.14 Minimum Primary Current

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation.

$$I_{PRI(min)} = \sqrt{\frac{C_R \times V_{IN(max)}^2}{L_R}} \quad (19)$$

This value can be supported by the calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower that IP(MIN) it can be used as a confirmation of the mathematics.

$$I_{R(average)} = C_R \times \frac{V_{IN}}{t_{MAX}} \quad (20)$$

Obtaining the necessary amount of primary current can be done in several ways. The most direct approach is to simply limit the minimum load current to the appropriate level. One alternative, however, is to design the transformer magnetizing inductance accordingly. Also assisting the magnetizing current is the reflected secondary inductor current contribution which is modeled in parallel. Any duty cycle variations modifying the peak charging current must also be taken into account.

Generally the magnetizing current alone is insufficient in many off-line high frequency converters. The transformer is usually core loss limited which means numerous primary turns and a high magnetizing inductance. Shunting the transformer primary with an external inductor to develop the right amount of primary current is one possibility. Incorporating the output filter inductor magnetizing current to assist resonance on the primary side is also an alternative.

9.2.3 Application Curve

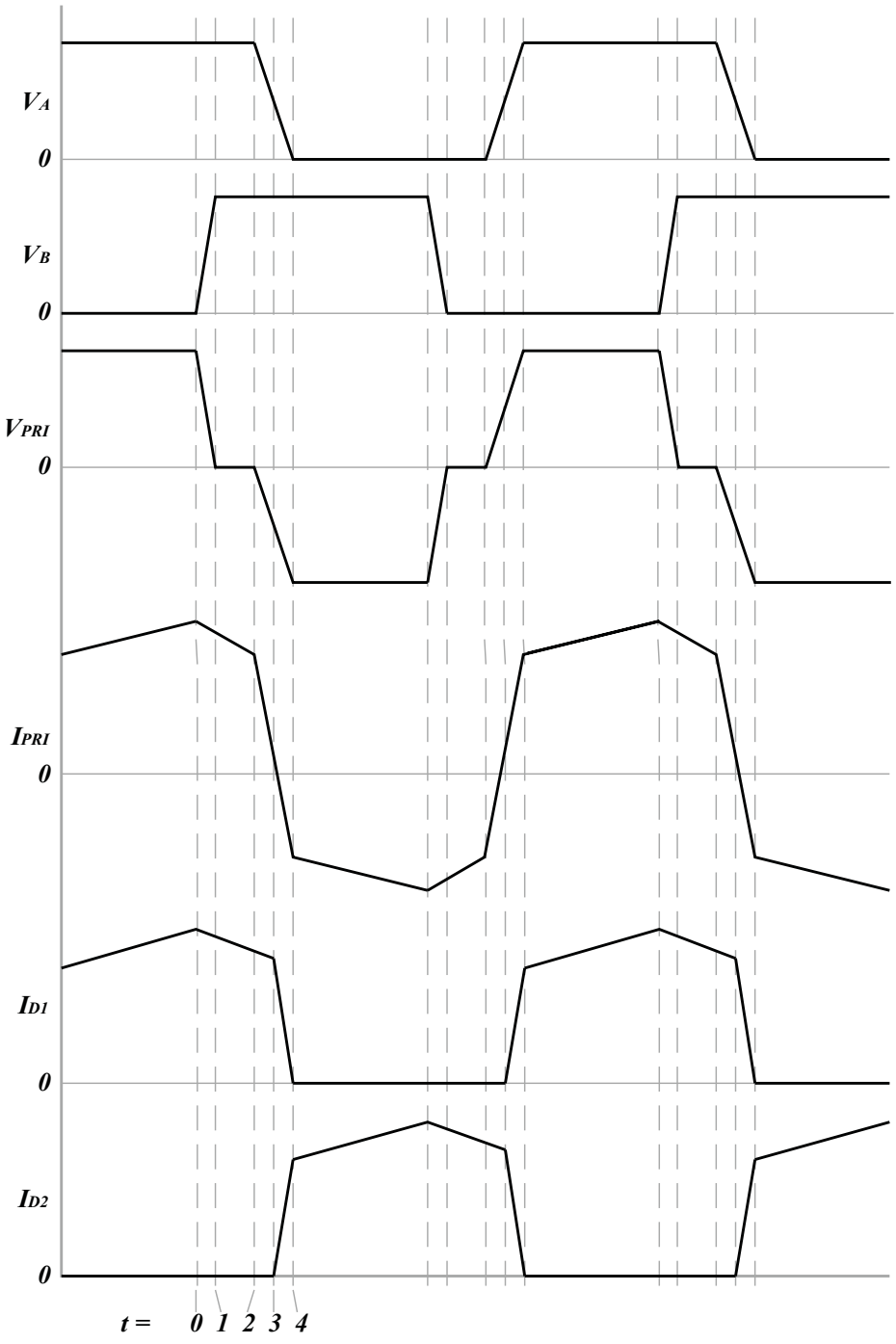


Figure 21. Operational Waveforms

10 Power Supply Recommendations

Power can be converted efficiently using any of several standard topologies. Design tradeoffs of cost, size, and performance generally narrow the field to one that is most appropriate. This demonstration application uses the full-bridge phase-shifted configuration.

11 Layout

11.1 Layout Guidelines

Connect Vin pin to bias supply from 10.75 V to 18 V range. Place high quality, low ESR and ESL, at least 1-μF ceramic bypass capacitor CVDD from this pin to GND. It is recommended to use 10-Ω resistor in series to VDD pin to form RC filter with CVDD capacitor.

11.1.1 Ground (GND)

All signals are referenced to this node. It is recommended to have a separate quite analog plane connected in one place to the power plane. The analog plane combines the components related to the pins VREF, E/A out, EA+, EA-, CS+, SoftStart, DELAYSET A-B, DELAYSET C-D, VC, RAMP, SLOPE, CLOCKSYNC, FREQSET, GND and VIN. The power plane combines the components related to the pins OUT A, OUT B, OUT C, OUT D, PWRGND, An example of layout and ground planes connection is shown

11.1.2 Bias Supply (VCC)

A bias supply generating Vcc voltage can be configured as flyback or forward operating off of Wide input voltage range in order to bias the UC1875-SP IC.

Always use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

11.1.3 Feedback Traces

Run the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

11.1.4 Compensation Components

External compensation components for stability should also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to the magnetic componets such as output transformer or output inductor.

11.1.5 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere. The inductor, output capacitors, and output diode should be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards the use of vias will be required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace will need to conduct a significant amount of current from one plane to the other. Arrange the components so that the switching current loops curl in the same direction.

Layout Guidelines (continued)

11.1.6 Current Transformer

As highlighted in the layout and schematic current is sensed in the input side and not in series with the main transformer. This is to ensue that the current transformer volt-second are balanced i does not flux-walk and saturate. If the current transformer were to be placed in series with the main transformer, if the main transformer were to flux-walk the current transformer will also saturate. Thus having the current transformer in the input side it will ensure to take corrective action to prevent main transformer from saturation.

11.2 Layout Example

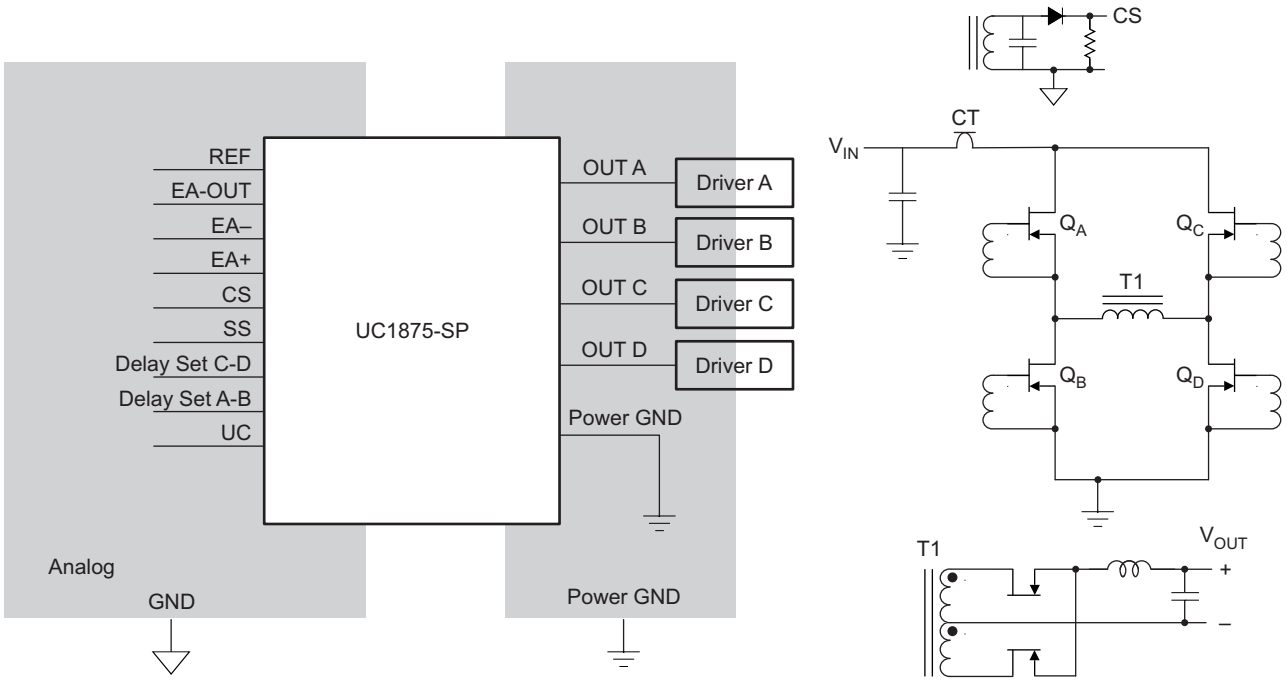


Figure 22. UC1875-SP Based Phase-Shifted Full-Bridge Converter

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9455501VRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9455501VRA UC1875JQMLV	Samples
5962-9455502VKA	ACTIVE	CFP	W	24	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9455502VKA UC1875W-SP	Samples
5962-9455502VRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9455502VRA UC1875J-SP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

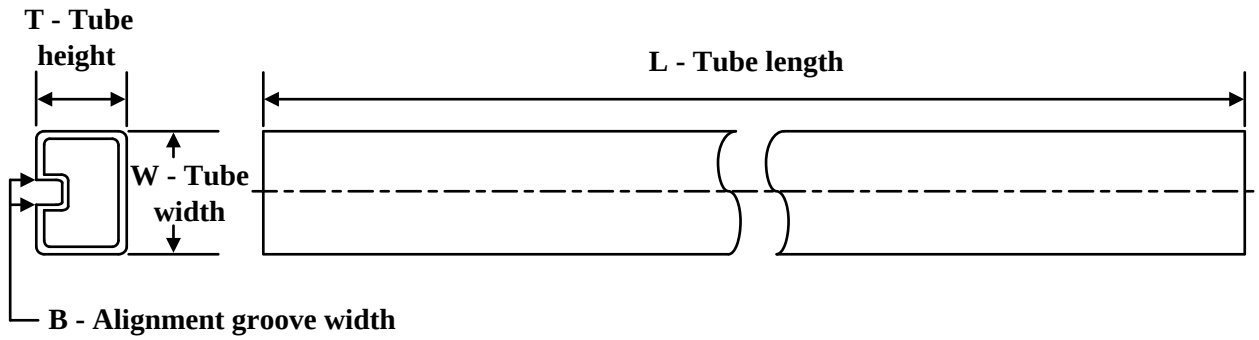
OTHER QUALIFIED VERSIONS OF UC1875-SP :

- Catalog : UC1875

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

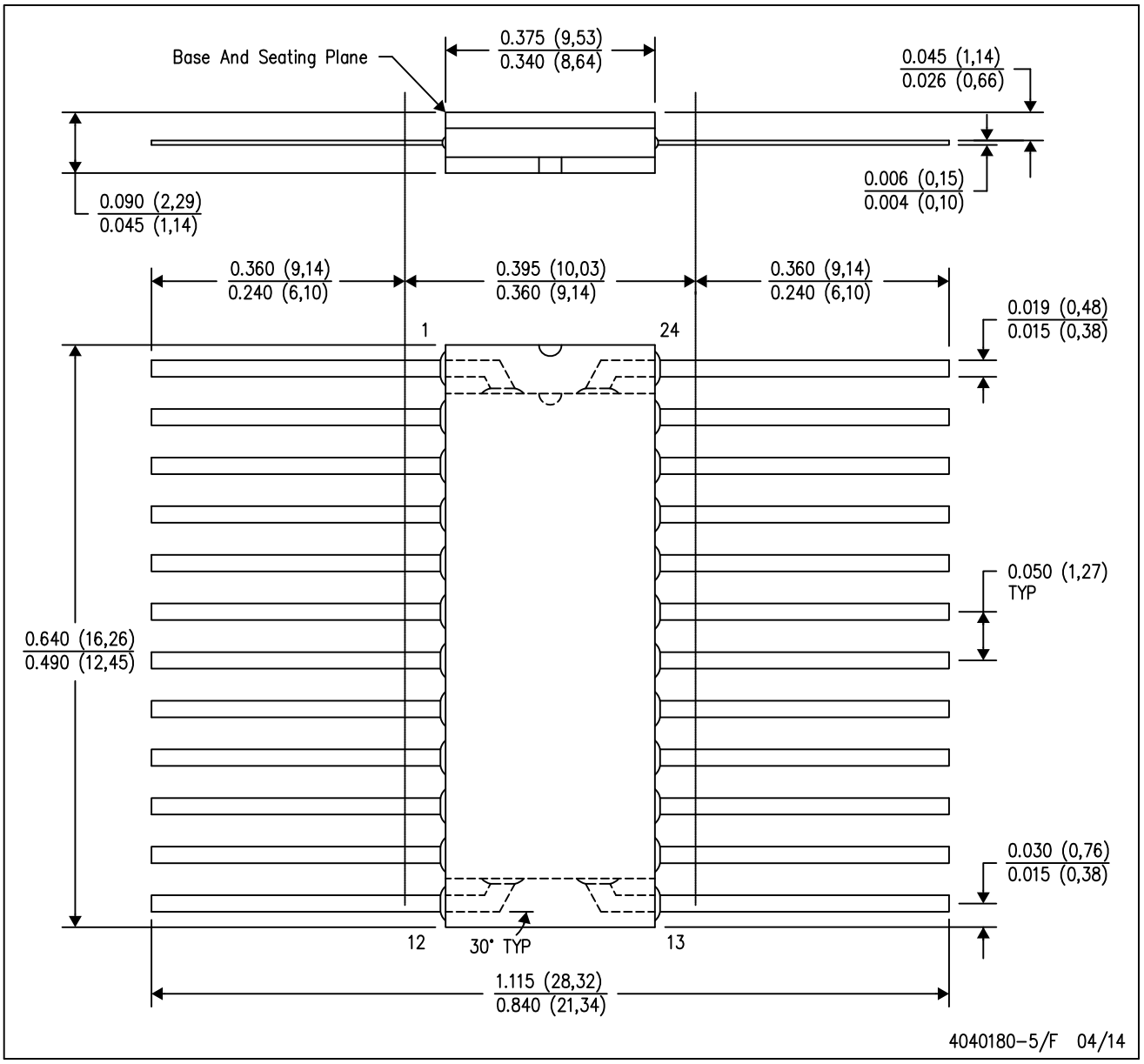
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9455502VKA	W	CFP	24	25	506.98	26.16	6220	NA
5962-9455502VRA	J	CDIP	20	20	506.98	15.24	13440	NA

W (R–GDFP–F24) CERAMIC DUAL FLATPACK

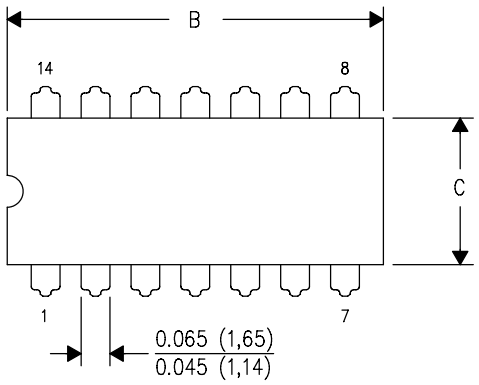


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

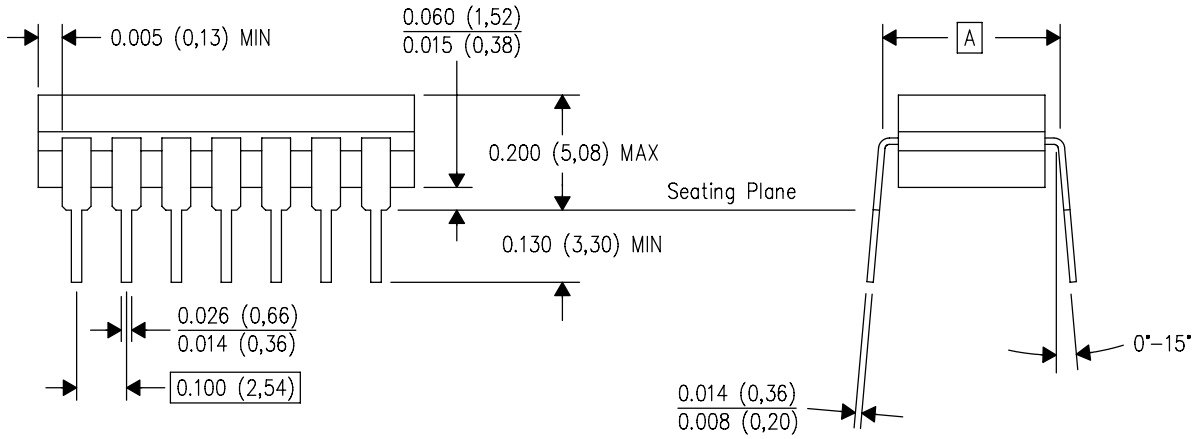
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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