INTEGRATED CIRCUITS
UNITRODE

UC1840
UC2840
UC3840

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current, Off-Line Start Circuit
- Feed-Forward Line Regulation over 4 to 1 Input Range
- PWM Latch for Single Pulse per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On and Maximum Duty-Cycle Clamp
- Shutdown Upon Over-or Under-Voltage Sensing
- Latch Off or Continuous Retry after Fault
- Remote, Pulse-Commandable Start/Stop
- PWM Output Switch Usable to 1A Peak Current
- 1% Reference Accuracy
- 500kHz Operation
- 18-pin DIL package

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operations over a wide input voltage range.

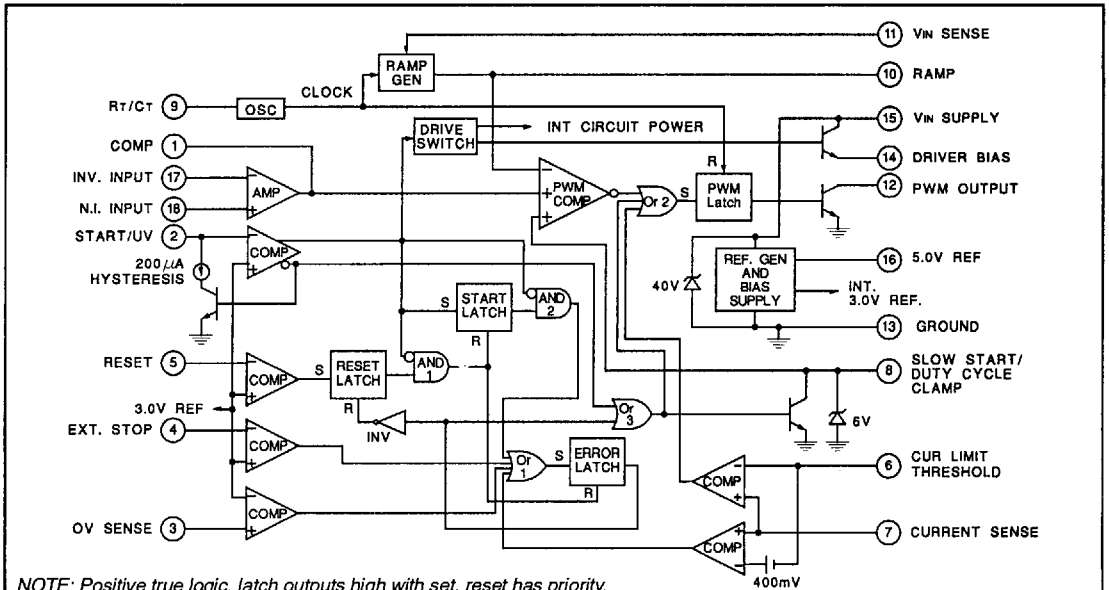
In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package. The UC1840 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2840 and UC3840 are designed for operation from -25°C to +85°C and 0°C to +70°C, respectively.

NOTE: THIS DEVICE NOT RECOMMENDED FOR NEW DESIGNS.

BLOCK DIAGRAM



NOTE: Positive true logic, latch outputs high with set, reset has priority.

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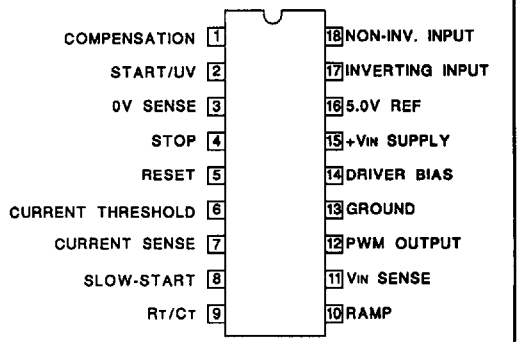
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, +VIN (Pin 15)
  Voltage Driven ..... +32V
  Current Driven, 100mA maximum ..... Self-limiting
PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20μJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
VIN Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Comparator Inputs (Pins 2, 3, 4, 5, 17, 18) ..... -0.3 to +32V
Power Dissipation at TA = 25°C 1000mW
Power Dissipation at TC = 25°C 2000mW
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) ..... +300°C

Note: 1. All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal.

CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1840, -25°C to + 85°C for the UC2840, and 0°C to + 70°C for the UC3840; VIN = 20V, RT = 20k, CT = .001mfd, CR = .001mfd, Current Limit Threshold = 200mV, TA=TJ.

PARAMETER	TEST CONDITIONS	UC1840 / UC2840			UC3840			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	VIN = 30V, Pin 2 =2.5V, TJ = 25°C		4	5.5		4	5.5	mA
Start-Up Current T.C.*	VIN = 30V, Pin 2 = 2.5V		-0.1	-0.2		-0.1	-0.2	%/°C
Operating Current	VIN = 30V, Pin 2 = 3.5V	5	10	15	5	10	15	mA
Supply OV Clamp	IIN = 20mA	33	40	45	33	40	48	V
Reference Section								
Reference Voltage	TJ = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	VIN = 8 to 30V		10	15		10	20	mV
Load Regulation	IL = 0 to 20mA		10	20		10	30	mV
Temperature Coefficient*	Over Operating Temperature Range			±0.4			±0.4	mV/°C
Short Circuit Current	VREF = 0, TJ = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	TJ = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	VIN = 8 to 30V		0.5	1		0.5	1	%
Temperature Coefficient*	Over Operating Temperature Range			±.08			±.08	%/°C
Maximum Frequency	RT = 2kΩ, CT = 330pF	500			500			kHz
Ramp Generator								
Ramp Current, Minimum	ISENSE = -10μA	-14	-11		-14	-11		μA
Ramp Current, Maximum	ISENSE = 1.0mA		-.95	-0.9		-.95	-0.9	mA
Ramp Valley		0.3	0.5	0.7	0.3	0.5	0.7	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

** These parameters are guaranteed by design but not 100% tested in production.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to + 125°C for the UC1840, -25°C to + 85°C for the UC2840, and 0°C to + 70°C for the UC3840; V_{IN} = 20V, R_T = 20k, C_T = .001mfd, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

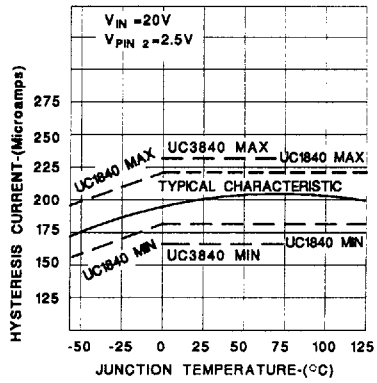
PARAMETER	TEST CONDITIONS	UC1840 / UC2840			UC3840			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range, Ramp Peak < 4.2V	ɔ		95	5		95	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	µA
Comparator Delay*	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 4, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 4, 5 = 0V		-1.0	-3.0		-1.0	-3.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V, T_J = 25°C	180	200	220	170	200	230	µA
Input Leakage	Input V = 20V		0.1	10		0.1	10	µA
Driver Bias Saturation Voltage, V_{IN} - V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 2mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range*		-0.4		3.0	-0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

** These parameters are guaranteed by design but not 100% tested in production.*

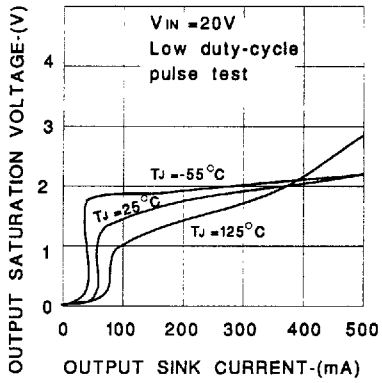
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where Kc is a first order correction factor ≈ 0.3 log (C_T X 10^{12}).
2. Ramp Generator	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected ≤ C_T and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable.
4. Reference Generator	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two possible inputs.
6. PWM Latch	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense	This comparator performs three functions — With an increasing voltage, it generates a turn-on signal at a start threshold. With a decreasing voltage, it generates a UV fault signal at a lower level separated by a 200µA hysteresis current. At the UV threshold, it also resets the Error Latch if the Reset Latch has been set.
2. Drive Switch	Disables most of the chip to hold internal current consumption low, and Driver Bias off, until input voltage reaches start threshold.
3. Driver Bias	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start	Clamps low to hold PWM off. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider $R_S R_{DC}$.
5. Start Latch	Keeps low input voltage at initial turn-on from being defined as a UV fault . Sets at start level to monitor for UV fault.
6. Reset Latch	When reset, this latch insures no reset signal to either Start or Error Latches so that first fault will lock the PWM off. When set, this latch resets the Start and and Error latches at the UV low threshold, allowing a restart.
PROTECTION FUNCTIONS	
1. Error Latch	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. UV low (after turn-on) b. OV high c. Stop low d. Current Sense 400mV over threshold. Error Latch resets at UV threshold if Reset Latch is set.
2. Current Limiting	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV above threshold, a shutdown signal is sent to error latch.

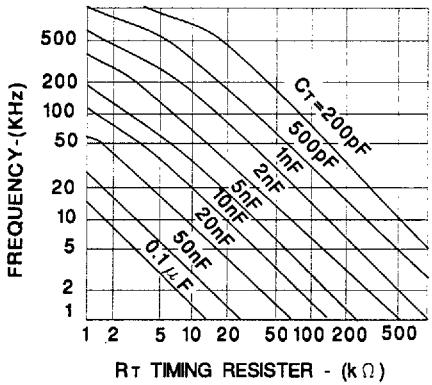
Start/UV Hysteresis Current



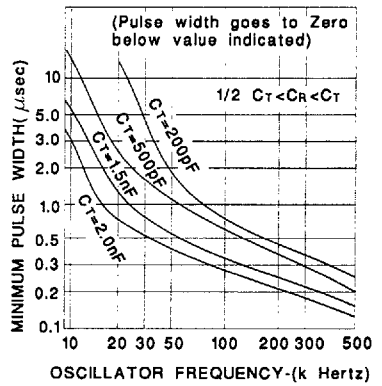
PWM Output Saturation Voltage



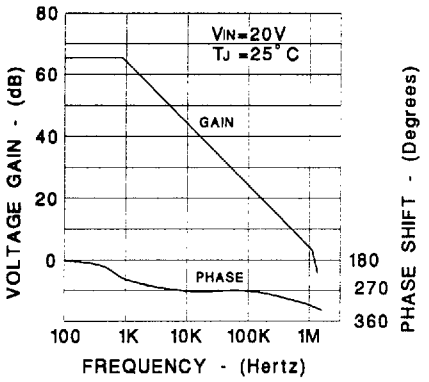
Oscillator Frequency



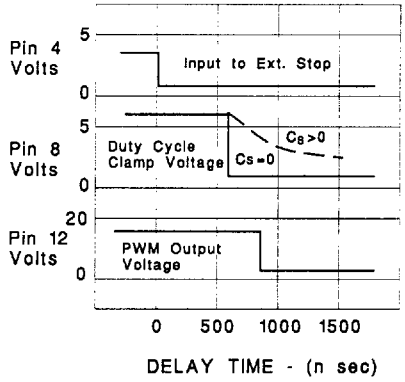
PWM Output Minimum Pulse Width



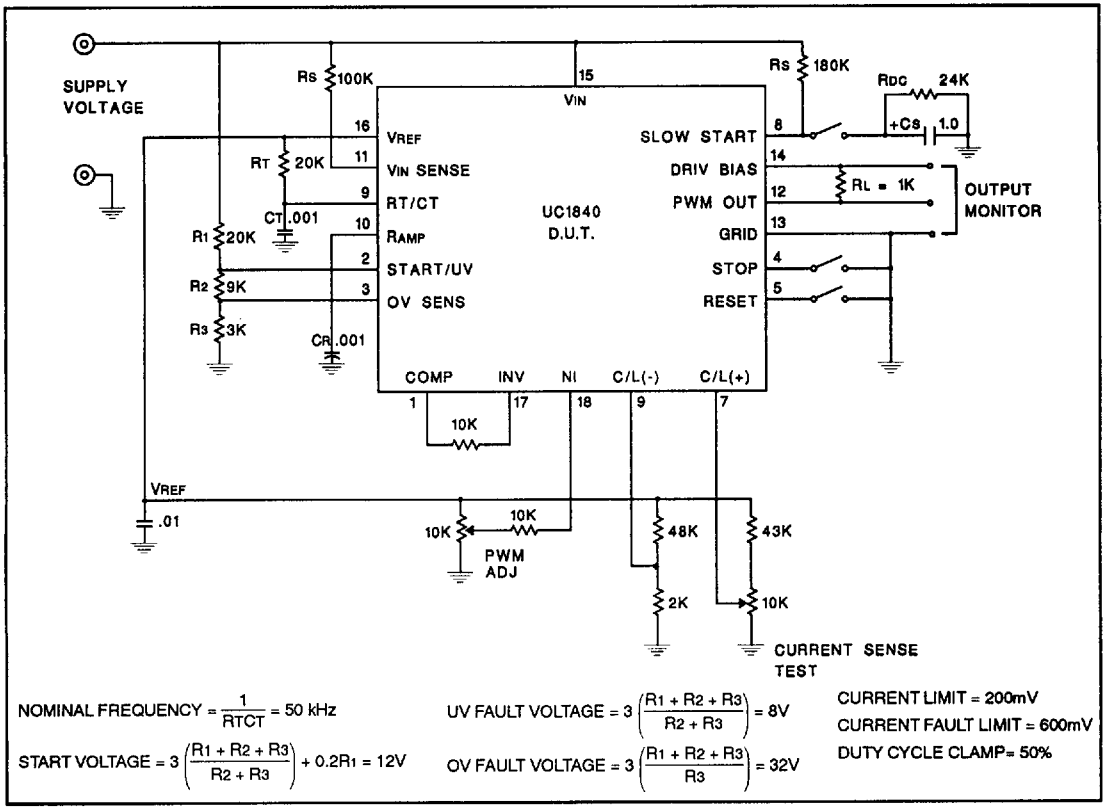
Error Amplifier Open-Loop Gain and Pulse



Shutdown Timing



OPEN-LOOP TEST CIRCUIT



FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by RIN and CIN during start-up, and by a primary- referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1840's feed-forward line regulation.

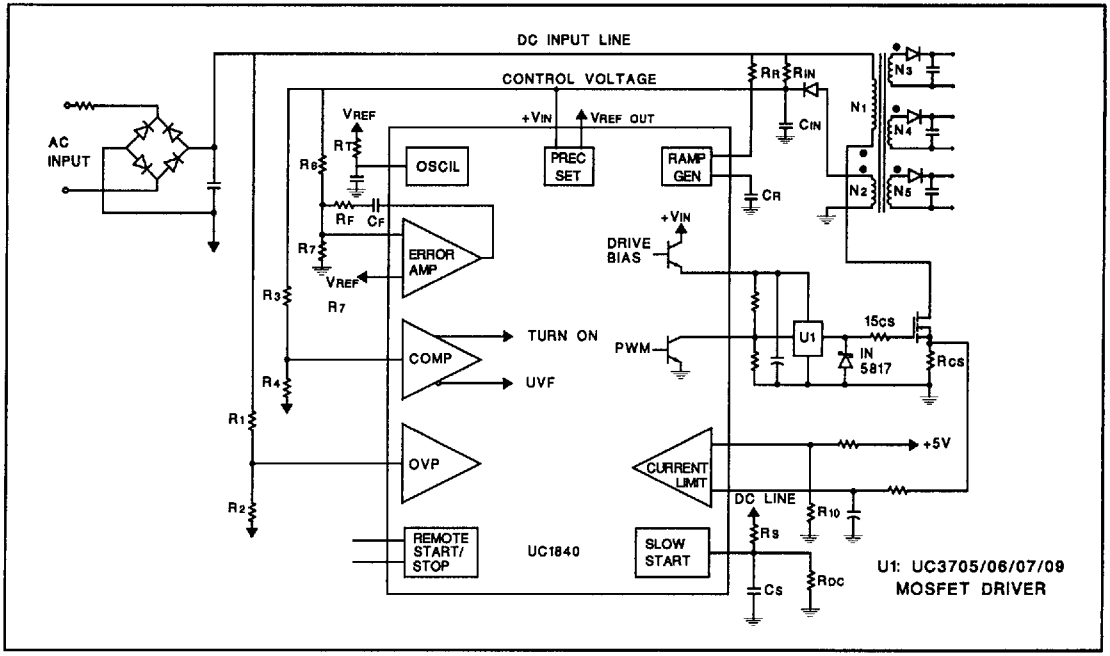
An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output. The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

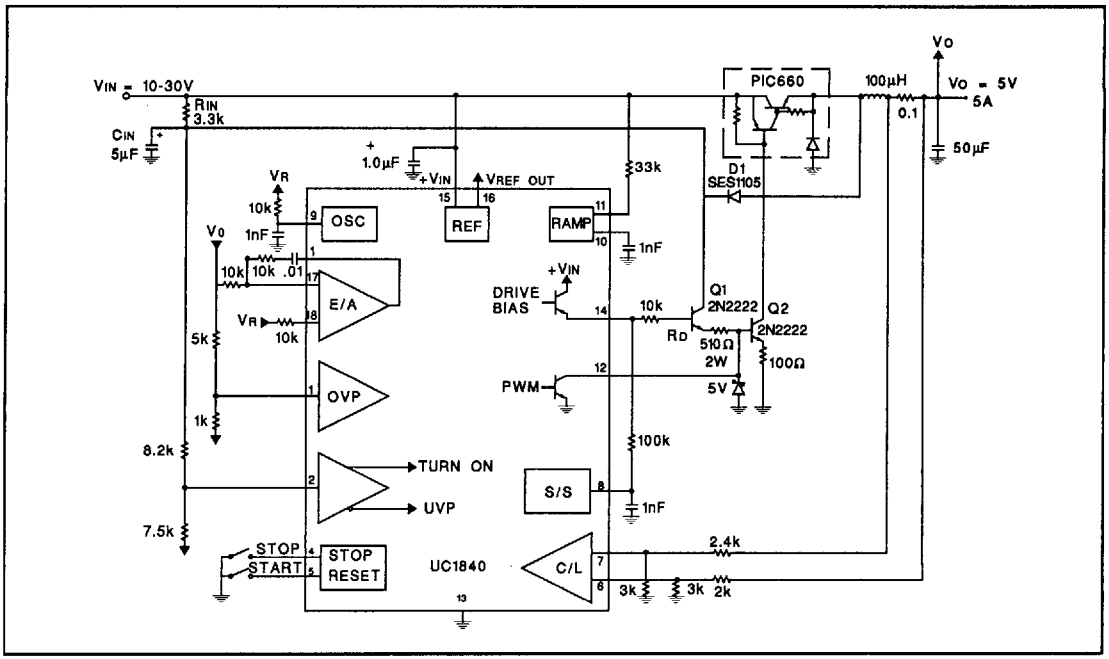
REGULATOR APPLICATION (B)

Although primarily intended for transformer-coupled power systems, the UC1840's advantages of feed-forward for high ripple-rejection, a fully contained fault monitoring system and remote start/stop capability make it worth considering for other types of regulators. Since the fault logic within the UC1840 requires recycling the voltage sensed by the Start/UV comparator to reset the error latch, a need for automatic restart must be addressed in a manner similar to that shown in Figure B (next page). In this simple, non-isolated, buck regulator; diode D1 provides a low-impedance bootstrapped drive power source after start-up is achieved through RIN and CIN. When a fault shutdown terminates switching action, the loading of Q1 and RD will lower the voltage on pin 2 to effect an automatic re-start attempt which will continuously recycle until the fault is removed.

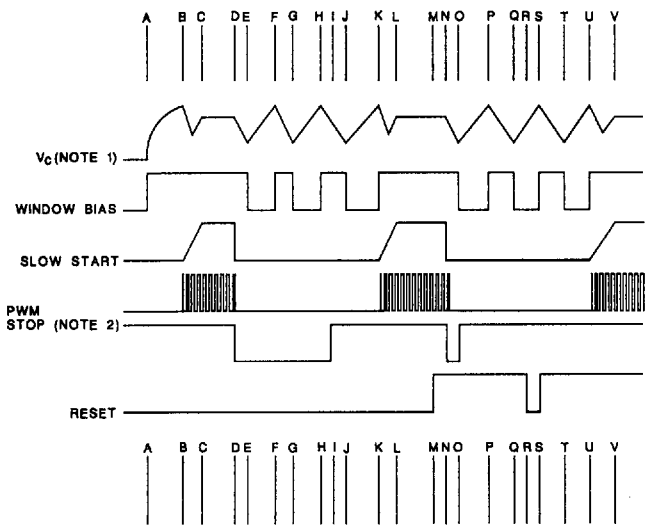
UC1840 Programmable Pwm Controller in a Simplified Flyback Regulator (A)



UC1840 Controls a High-Current Non-Isolated Buck Regulator (B)



UC1840 POWER SEQUENCING FUNCTIONS

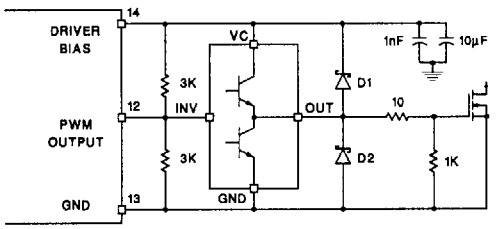


TIME	EVENT
A	Initial turn-on, Vc rises with load
B	Start threshold. Driver Bias loads Vc
C	Operating PWM regulates Vc
D	Stop input sets Error Latch turning off PWM
E	UV low threshold, Error Latch remains set
F	Start turns on Driver bias but Error Latch still set
G, H	Vc and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at UV low threshold
K	Start threshold now removes slow-start clamp
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
O	Error Latch does not reset as Reset Latch is reset
P, Q	Vc and Driver Bias recycle with no turn-on.
R	Reset Latch set is set with momentary Reset signal
S	Vc must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

Notes 1: Vc represents an analog of the output voltage generated by a primary referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and, in most cases, is the supply voltage, VIN, for the UC1840.

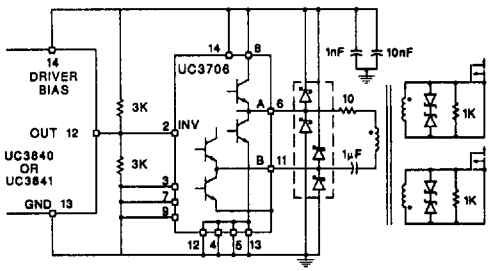
Note 2: Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

Power MOSFET Drive Circuit Using UC3705/3706/3707 or 3709 Drivers



D1, D2: UC3611 Schottky Diode

UC3706 Converts Single Output PWMs to High Current Push-Pull Configuration



UC3611 Quad Schottky Diode Array

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