



## General Description

The UC3842B/3B/4B/5B, series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

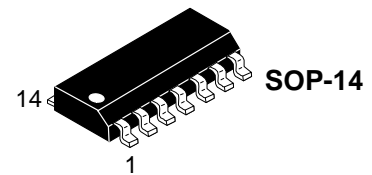
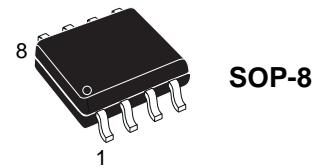
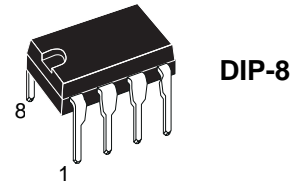
These devices are available in an 8-pin dual-in-line and surface mount (SO-8) plastic package as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UC3842B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UC3843B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

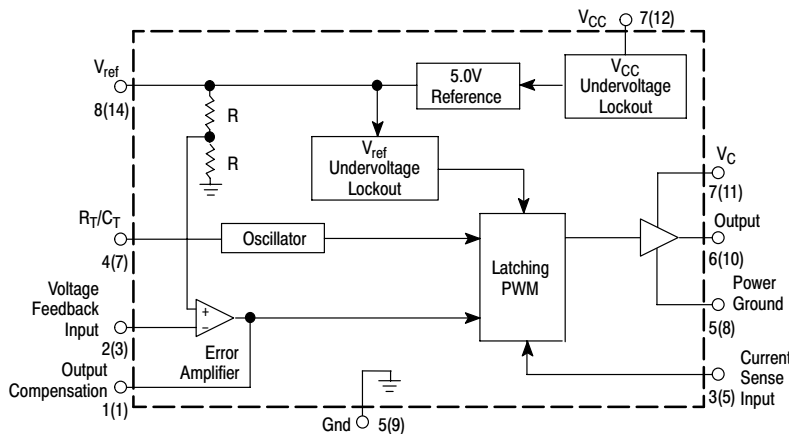
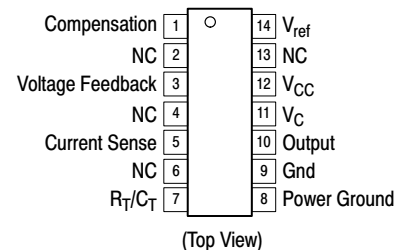
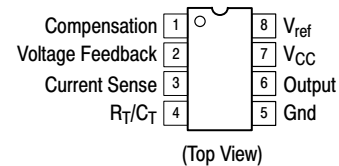
## Features

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

## Package outline



## Pin Connections



Pin numbers in parenthesis are for the D suffix SO-14 package.

**Figure 1. Simplified Block Diagram**



# UC3842B/3B/4B/5B, UC2842B/3B

## Maximum Ratings

Rating	Symbol	Value	Unit
Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec)	$V_{CC}, V_C$	30	V
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	$I_O$	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	$\mu\text{J}$
Current Sense and Voltage Feedback Inputs	$V_{in}$	-0.3 to +5.5	V
Error Amp Output Sink Current	$I_O$	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SO-14 Case 751A			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	862	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	145	$^\circ\text{C/W}$
D1 Suffix, Plastic Package, SO-8 Case 751			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	702	mW
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	178	$^\circ\text{C/W}$
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.25	W
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Operating Junction Temperature	$T_J$	+150	$^\circ\text{C}$
Operating Ambient Temperature	$T_A$		$^\circ\text{C}$
UC3842B/3B/4B/5B		0 to +70	
UC2842B/3B		-25 to +85	
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

**Electrical Characteristics** ( $V_{CC} = 15\text{ V}$  [Note 2],  $R_T = 10\text{ k}$ ,  $C_T = 3.3\text{ nF}$ . For typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A$  is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB			Unit
		Min	Typ	Max	Min	Typ	Max	

## Reference Section

Reference Output Voltage ( $I_O = 1.0\text{ mA}$ , $T_J = 25^\circ\text{C}$ )	$V_{ref}$	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation ( $V_{CC} = 12\text{ V to } 25\text{ V}$ )	$Reg_{line}$	-	2.0	20	-	6.0	20	mV
Load Regulation ( $I_O = 1.0\text{ mA to } 20\text{ mA}$ )	$Reg_{load}$	-	3.0	25	-	6.0	25	mV
Temperature Stability	$T_S$	-	0.2	-	-	0.2	-	mV/ $^\circ\text{C}$
Total Output Variation over Line, Load, and Temperature	$V_{ref}$	4.9	-	5.1	4.82	-	5.18	V
Output Noise Voltage ( $f = 10\text{ Hz to } 10\text{ kHz}$ , $T_J = 25^\circ\text{C}$ )	$V_n$	-	50	-	-	50	-	$\mu\text{V}$
Long Term Stability ( $T_A = 125^\circ\text{C}$ for 1000 Hours)	S	-	5.0	-	-	5.0	-	mV
Output Short Circuit Current	$I_{SC}$	-30	-85	-180	-30	-100	-180	mA

## Oscillator Section

Frequency	$f_{osc}$							kHz
$T_J = 25^\circ\text{C}$		49	52	55	47	50	55	
$T_A = T_{low}$ to $T_{high}$		48	-	56	47	52	56	
$T_J = 25^\circ\text{C}$ ( $R_T = 6.2\text{ k}$ , $C_T = 1.0\text{ nF}$ )		225	250	275	225	250	275	
Frequency Change with Voltage ( $V_{CC} = 12\text{ V to } 25\text{ V}$ )	$\Delta f_{osc}/\Delta V$	-	0.2	1.0	-	0.2	1.0	%
Frequency Change with Temperature, $T_A = T_{low}$ to $T_{high}$	$\Delta f_{osc}/\Delta T$	-	1.0	-	-	0.5	-	%
Oscillator Voltage Swing (Peak-to-Peak)	$V_{osc}$	-	1.6	-	-	1.6	-	V
Discharge Current ( $V_{OSC} = 2.0\text{ V}$ )	$I_{dischg}$							mA
$T_J = 25^\circ\text{C}$		7.8	8.3	8.8	7.8	8.3	8.8	
$T_A = T_{low}$ to $T_{high}$ (UC284XB, UC384XB)		7.5	-	8.8	7.6	-	8.8	

- Maximum Package power dissipation limits must be observed.
- Adjust  $V_{CC}$  above the Startup threshold before setting to 15 V.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.  
 $T_{low} = 0^\circ\text{C}$  for UC3842B/3B/4B/5B;  $-25^\circ\text{C}$  for UC2842B/3B  
 $T_{high} = +70^\circ\text{C}$  for UC3842B/3B/4B/5B;  $+85^\circ\text{C}$  for UC2842B/3B



# UC3842B/3B/4B/5B, UC2842B/3B

**Electrical Characteristics** ( $V_{CC} = 15\text{ V}$  [Note 4],  $R_T = 10\text{ k}$ ,  $C_T = 3.3\text{ nF}$ . For typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A$  is the operating ambient temperature range that applies [Note 5], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB			Unit
		Min	Typ	Max	Min	Typ	Max	

## Error Amplifier Section

Voltage Feedback Input ( $V_O = 2.5\text{ V}$ )	$V_{FB}$	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current ( $V_{FB} = 5.0\text{ V}$ )	$I_{IB}$	–	–0.1	–1.0	–	–0.1	–2.0	$\mu\text{A}$
Open Loop Voltage Gain ( $V_O = 2.0\text{ V}$ to $4.0\text{ V}$ )	$A_{VOL}$	65	90	–	65	90	–	dB
Unity Gain Bandwidth ( $T_J = 25^\circ\text{C}$ )	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio ( $V_{CC} = 12\text{ V}$ to $25\text{ V}$ )	PSRR	60	70	–	60	70	–	dB
Output Current Sink ( $V_O = 1.1\text{ V}$ , $V_{FB} = 2.7\text{ V}$ ) Source ( $V_O = 5.0\text{ V}$ , $V_{FB} = 2.3\text{ V}$ )	$I_{Sink}$ $I_{Source}$	2.0 –0.5	12 –1.0	– –	2.0 –0.5	12 –1.0	– –	mA
Output Voltage Swing High State ( $R_L = 15\text{ k}$ to ground, $V_{FB} = 2.3\text{ V}$ ) Low State ( $R_L = 15\text{ k}$ to $V_{ref}$ , $V_{FB} = 2.7\text{ V}$ ) (UC284XB, UC384XB)	$V_{OH}$ $V_{OL}$	5.0 –	6.2 0.8	– 1.1	5.0 –	6.2 0.8	– 1.1	V

## Current Sense Section

Current Sense Input Voltage Gain (Notes 6 & 7) (UC284XB, UC384XB)	$A_V$	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 6) (UC284XB, UC384XB)	$V_{th}$	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio ( $V_{CC} = 12\text{ V}$ to $25\text{ V}$ , Note 6)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	$I_{IB}$	–	–2.0	–10	–	–2.0	–10	$\mu\text{A}$
Propagation Delay (Current Sense Input to Output)	$t_{PLH}(I_{In}/Out)$	–	150	300	–	150	300	ns

## Output Section

Output Voltage Low State ( $I_{Sink} = 20\text{ mA}$ ) ( $I_{Sink} = 200\text{ mA}$ ) (UC284XB, UC384XB)	$V_{OL}$	– –	0.08 1.4	0.4 2.2	– –	0.08 1.4	0.4 2.2	V
High State ( $I_{Source} = 20\text{ mA}$ ) (UC284XB, UC384XB) ( $I_{Source} = 200\text{ mA}$ )	$V_{OH}$	13 12	13.5 13.0	– –	13 12	13.5 13.0	– –	V
Output Voltage with UVLO Activated ( $V_{CC} = 6.0\text{ V}$ , $I_{Sink} = 1.0\text{ mA}$ )	$V_{OL}(UVLO)$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time ( $C_L = 1.0\text{ nF}$ , $T_J = 25^\circ\text{C}$ )	$t_r$	–	45	150	–	45	150	ns
Output Voltage Fall Time ( $C_L = 1.0\text{ nF}$ , $T_J = 25^\circ\text{C}$ )	$t_f$	–	35	150	–	35	150	ns

## Undervoltage Lockout Section

Startup Threshold ( $V_{CC}$ ) UCX842B/4B UCX843B/5B	$V_{th}$	15 7.8	16 8.4	17 9.0	14.5 7.8	16 8.4	17.5 9.0	V
Minimum Operating Voltage After Turn-On ( $V_{CC}$ ) UCX842B/4B UCX843B/5B	$V_{CC(min)}$	9.0 7.0	10 7.6	11 8.2	8.5 7.0	10 7.6	11.5 8.2	V

- Adjust  $V_{CC}$  above the Startup threshold before setting to  $15\text{ V}$ .
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.  
 $T_{low} = 0^\circ\text{C}$  for UC3842B/3B/4B/5B;  $-25^\circ\text{C}$  for UC2842B/3B  
 $T_{high} = +70^\circ\text{C}$  for UC3842B/3B/4B/5B;  $+85^\circ\text{C}$  for UC2842B/3B
- This parameter is measured at the latch trip point with  $V_{FB} = 0\text{ V}$ .
- Comparator gain is defined as:  $A_V = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$



# UC3842B/3B/4B/5B, UC2842B/3B

**Electrical Characteristics** ( $V_{CC} = 15\text{ V}$  [Note 8],  $R_T = 10\text{ k}$ ,  $C_T = 3.3\text{ nF}$ , for typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A$  is the operating ambient temperature range that applies [Note 9], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, BV			Unit
		Min	Typ	Max	Min	Typ	Max	

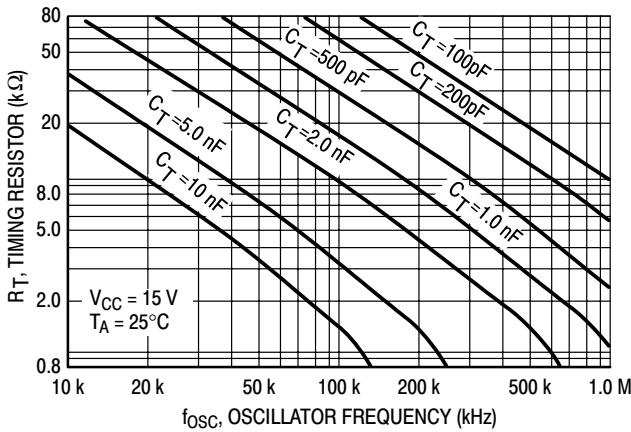
### Pwm Section

Duty Cycle								
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	94	96	–	94	96	–	%
Minimum	$DC_{(min)}$	–	–	0	–	–	0	

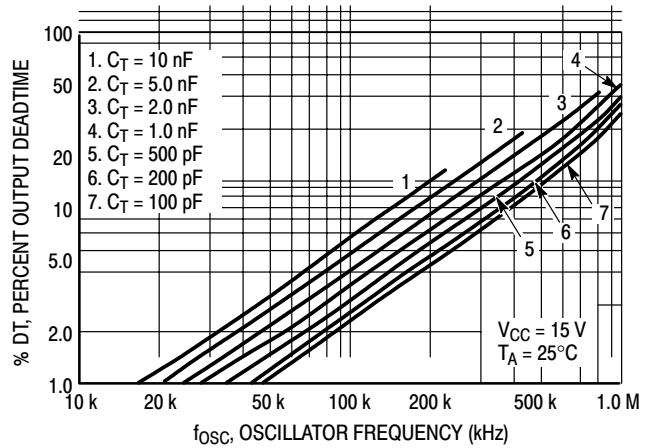
### Total Device

Power Supply Current								
Startup ( $V_{CC} = 6.5\text{ V}$ for UCX843B, $V_{CC} = 14\text{ V}$ for UCX842B)	$I_{CC} + I_C$	–	0.17	0.3	–	0.17	0.3	mA
Operating (Note 8)		–	13	17	–	13	17	
Power Supply Zener Voltage ( $I_{CC} = 25\text{ mA}$ )	$V_Z$	30	36	–	30	36	–	V

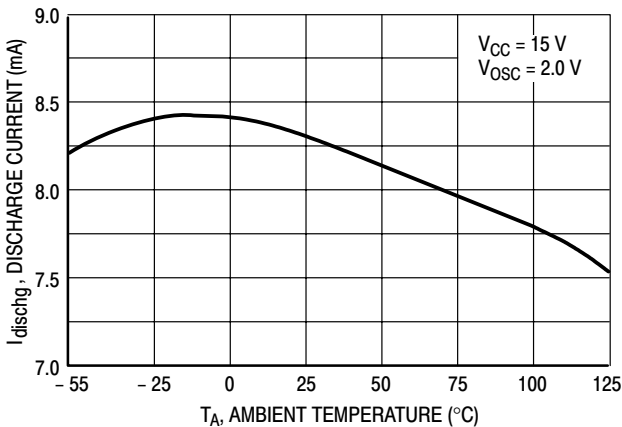
- Adjust  $V_{CC}$  above the Startup threshold before setting to 15 V.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.  
 $T_{low} = 0^\circ\text{C}$  for UC3842B/3B/4B/5B;  $-25^\circ\text{C}$  for UC2842B/3B  
 $T_{high} = +70^\circ\text{C}$  for UC3842B/3B/4B/5B;  $+85^\circ\text{C}$  for UC2842B/3B



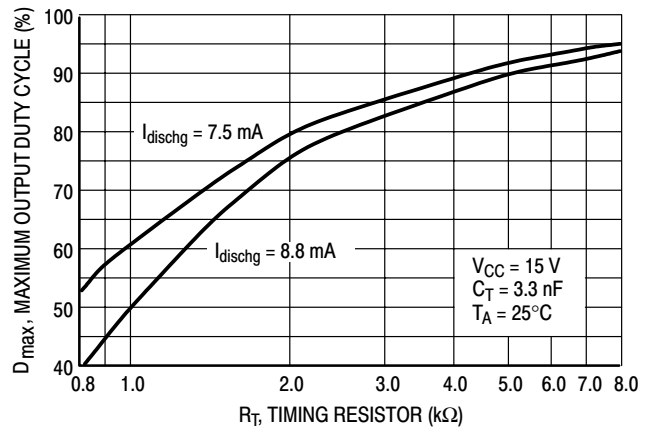
**Figure 2. Timing Resistor versus Oscillator Frequency**



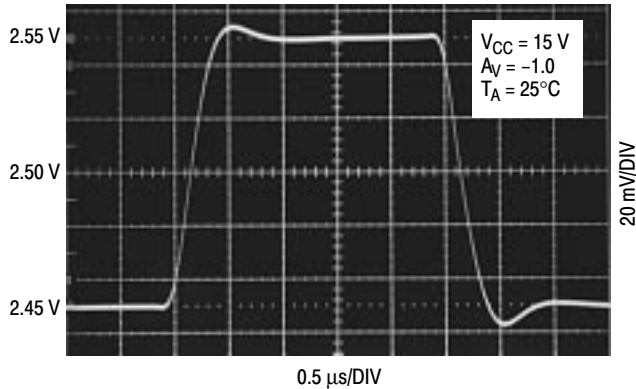
**Figure 3. Output Deadtime versus Oscillator Frequency**



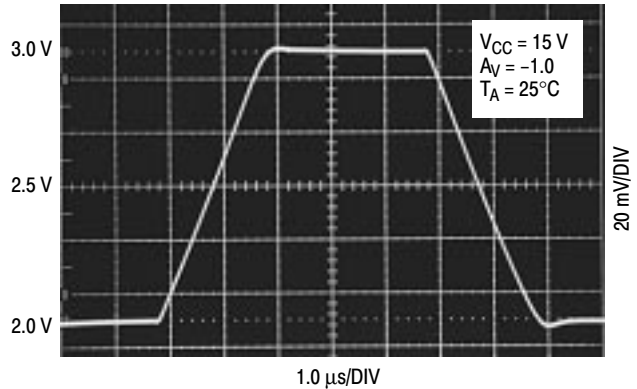
**Figure 4. Oscillator Discharge Current versus Temperature**



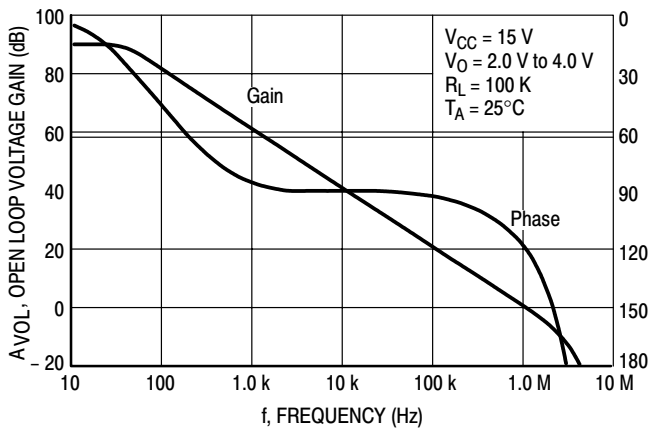
**Figure 5. Maximum Output Duty Cycle versus Timing Resistor**



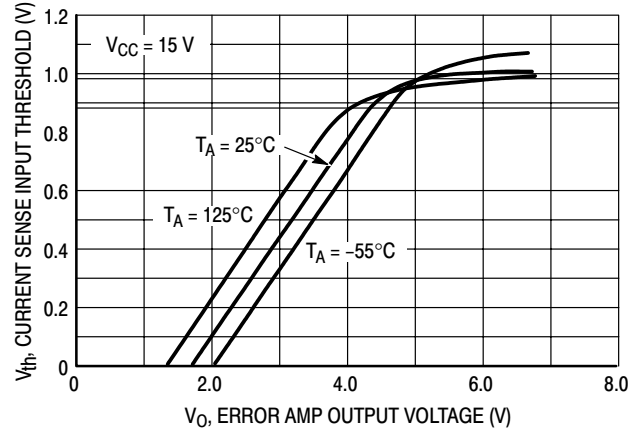
**Figure 6. Error Amp Small Signal Transient Response**



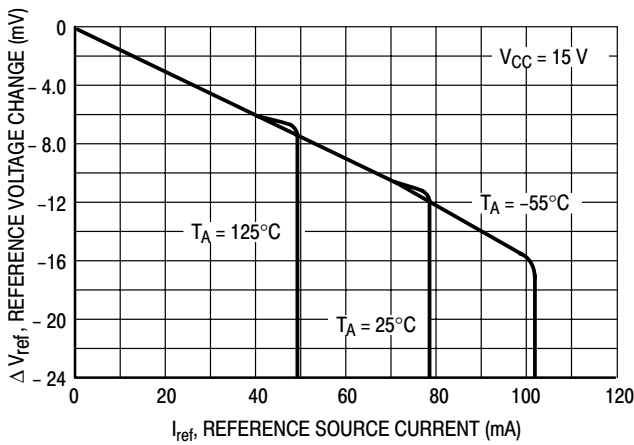
**Figure 7. Error Amp Large Signal Transient Response**



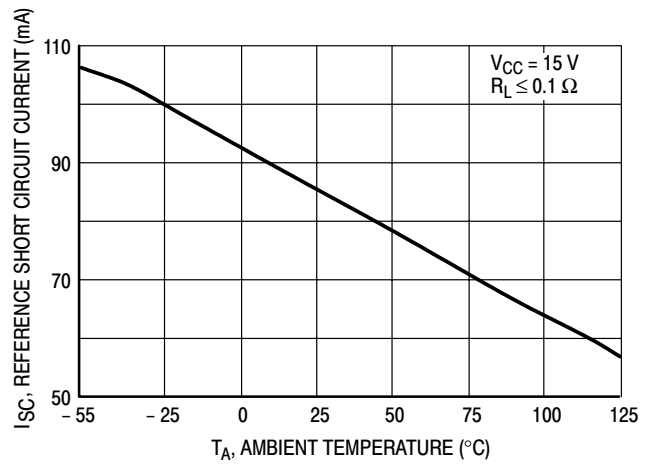
**Figure 8. Error Amp Open Loop Gain and Phase versus Frequency**



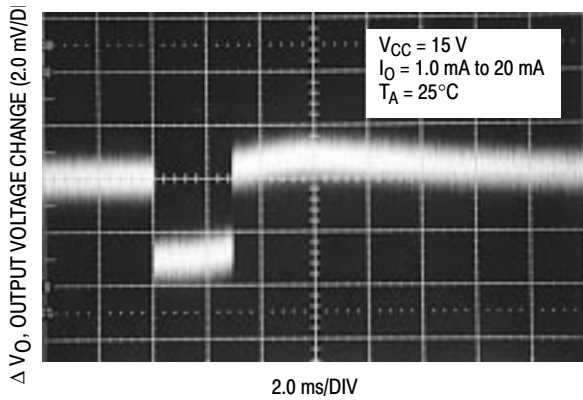
**Figure 9. Current Sense Input Threshold versus Error Amp Output Voltage**



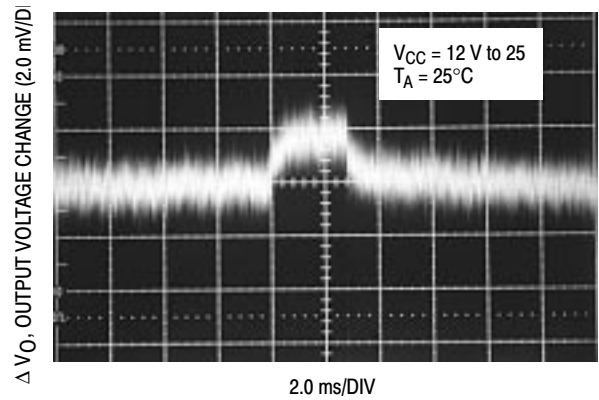
**Figure 10. Reference Voltage Change versus Source Current**



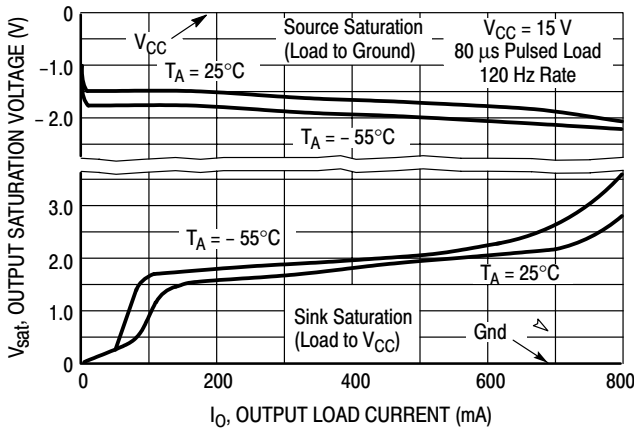
**Figure 11. Reference Short Circuit Current versus Temperature**



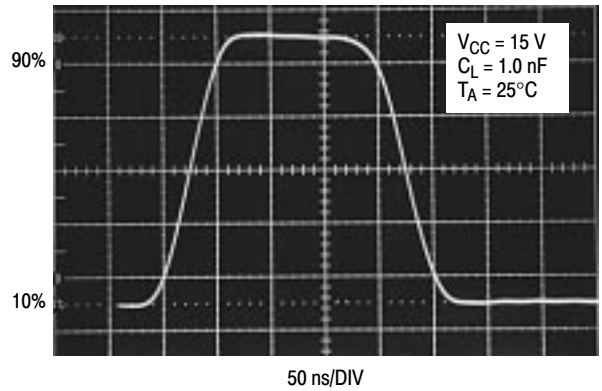
**Figure 12. Reference Load Regulation**



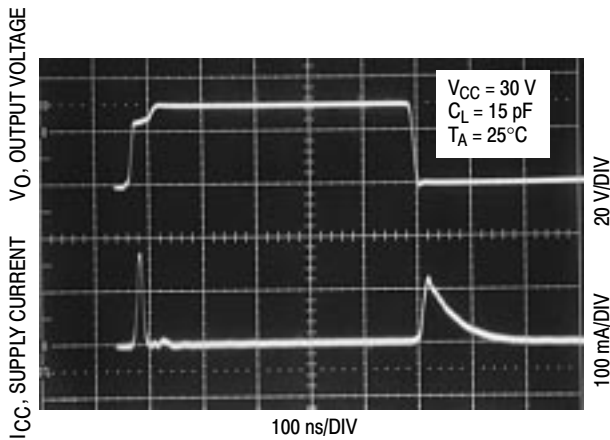
**Figure 13. Reference Line Regulation**



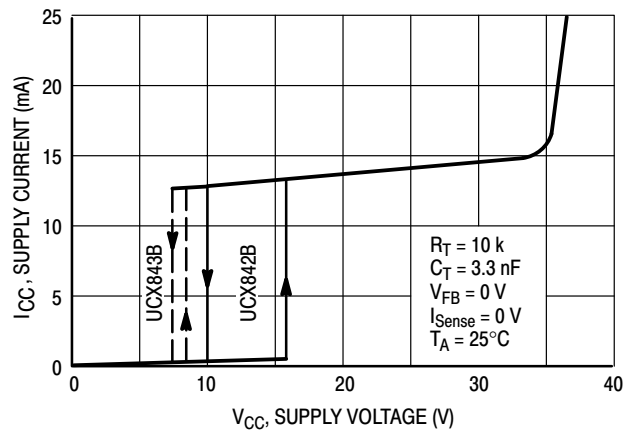
**Figure 14. Output Saturation Voltage versus Load Current**



**Figure 15. Output Waveform**



**Figure 16. Output Cross Conduction**

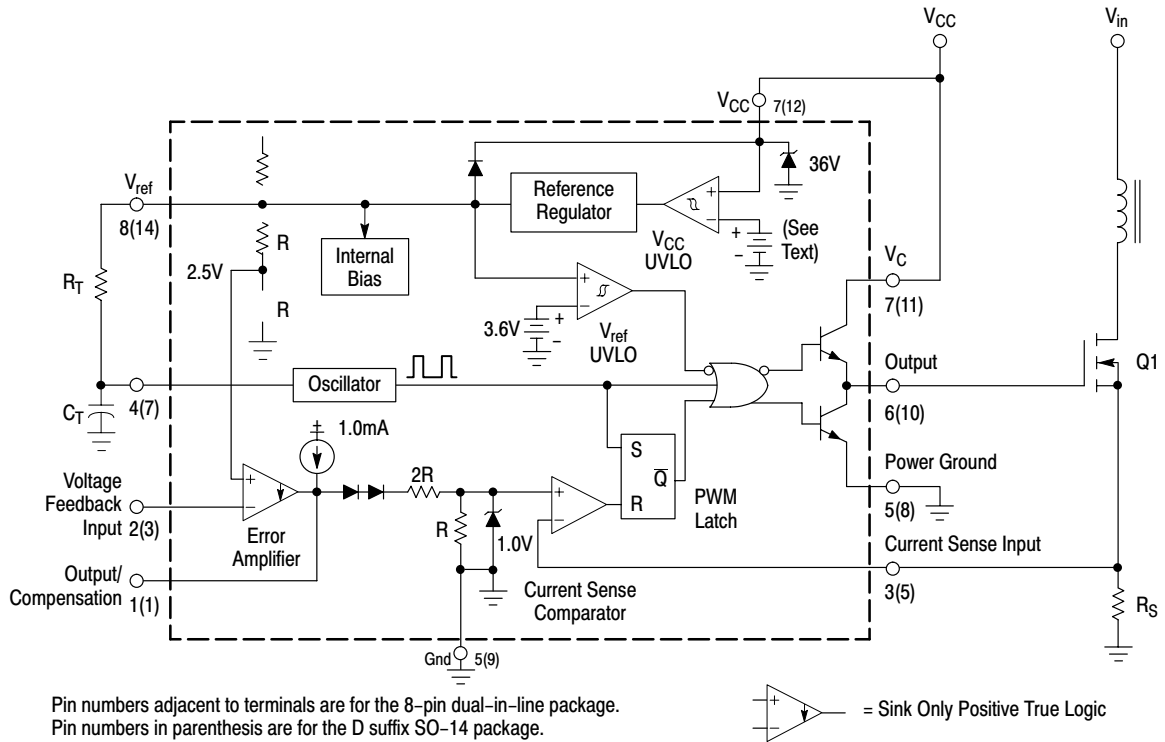


**Figure 17. Supply Current versus Supply Voltage**

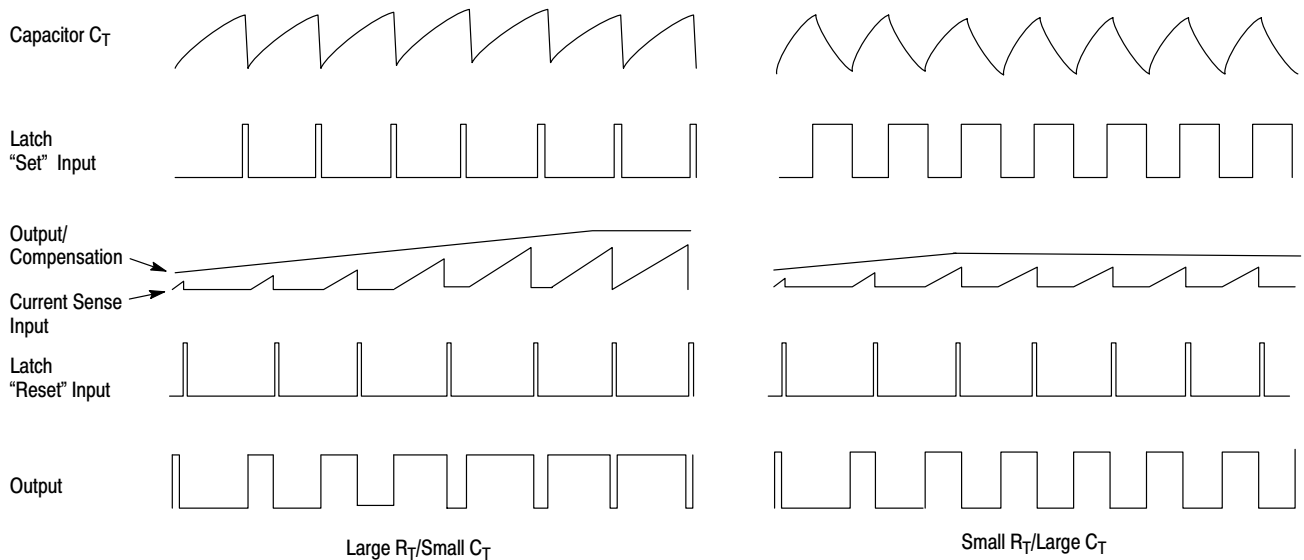


## Pin Function Description

Pin		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	$R_T/C_T$	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor $R_T$ to $V_{ref}$ and capacitor $C_T$ to ground. Operation to 500 kHz is possible.
5		Gnd	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	$V_{CC}$	This pin is the positive supply of the control IC.
8	14	$V_{ref}$	This is the reference output. It provides charging current for capacitor $C_T$ through resistor $R_T$ .
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	$V_C$	The Output high state ( $V_{OH}$ ) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	Gnd	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

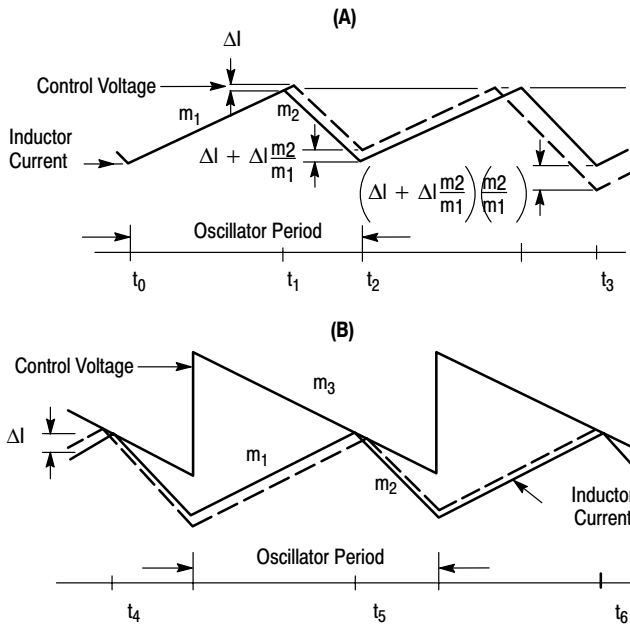


**Figure 18. Representative Block Diagram**

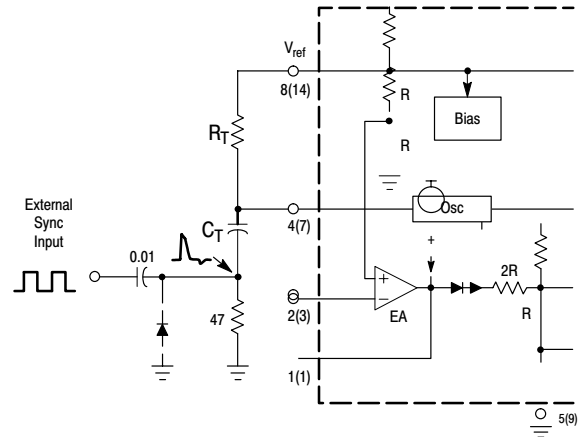


**Figure 19. Timing Diagram**



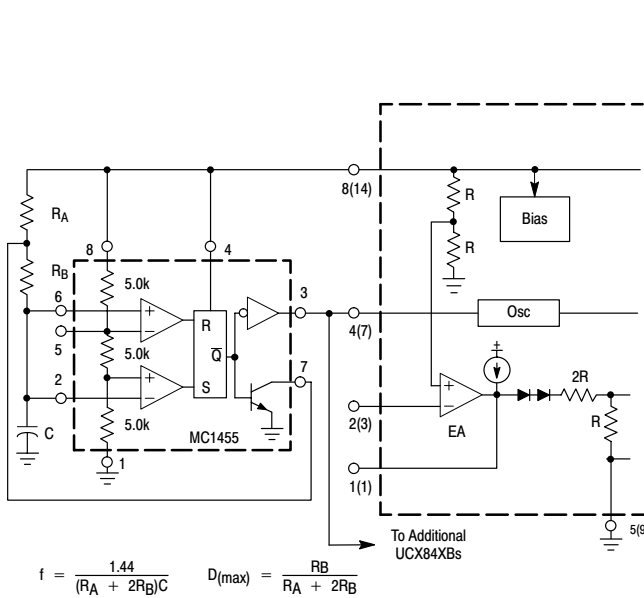


**Figure 20. Continuous Current Waveforms**

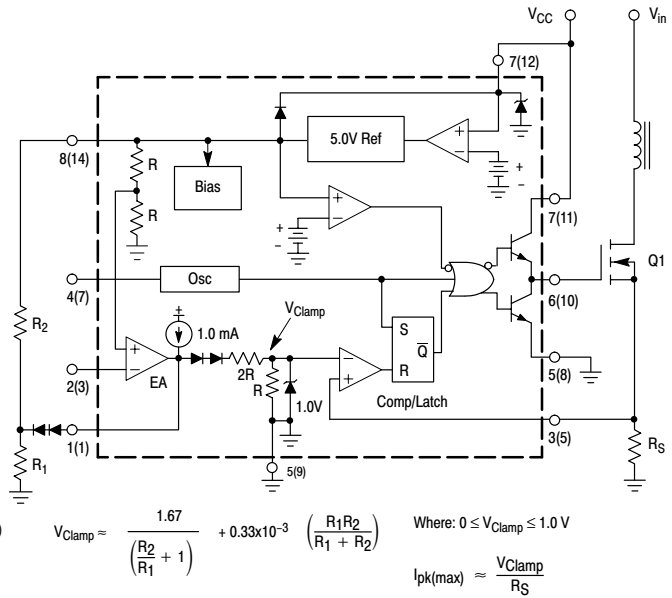


The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of  $C_T$  to go more than 300 mV below ground.

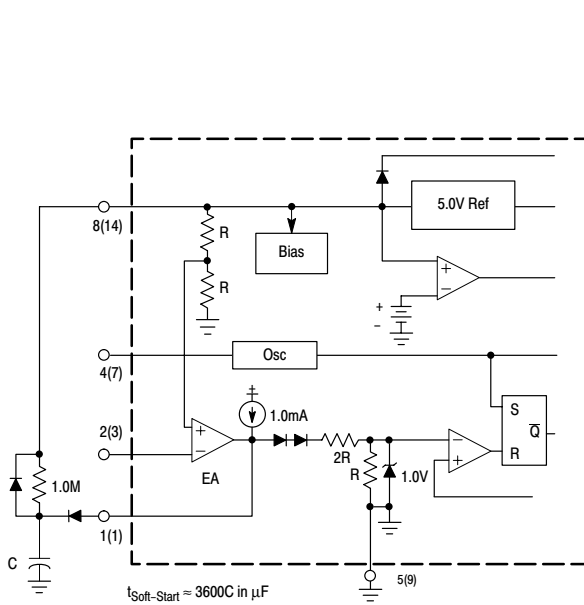
**Figure 21. External Clock Synchronization**



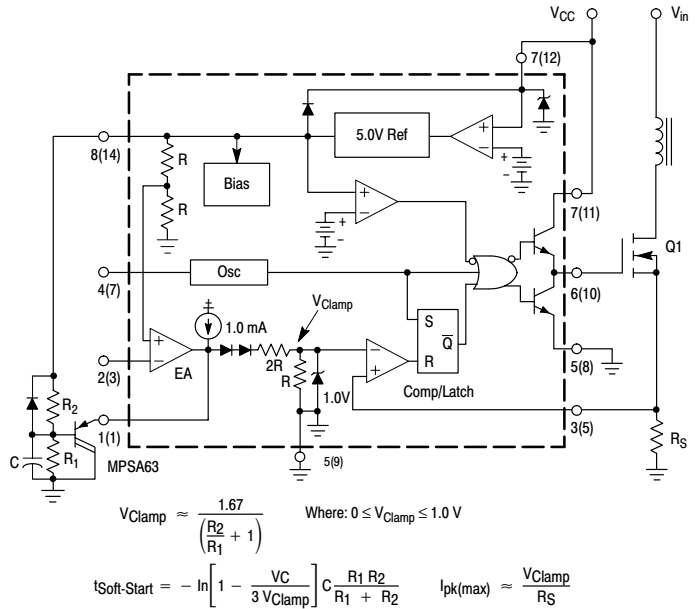
**Figure 22. External Duty Cycle Clamp and Multi-Unit Synchronization**



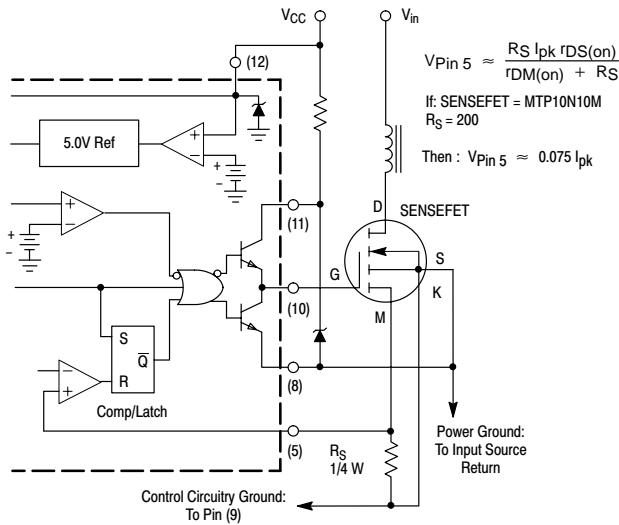
**Figure 23. Adjustable Reduction of Clamp Level**



**Figure 24. Soft-Start Circuit**

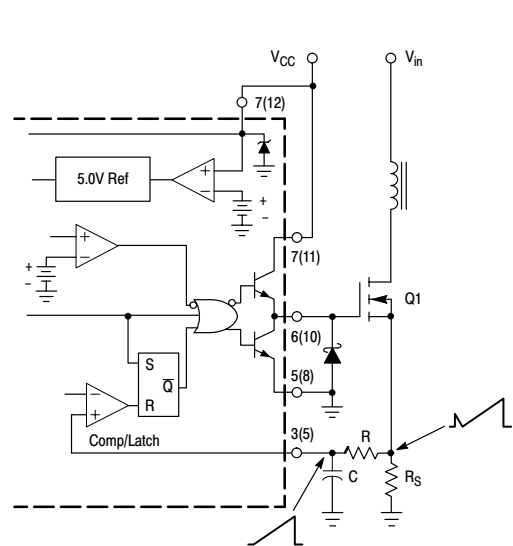


**Figure 25. Adjustable Buffered Reduction of Clamp Level with Soft-Start**



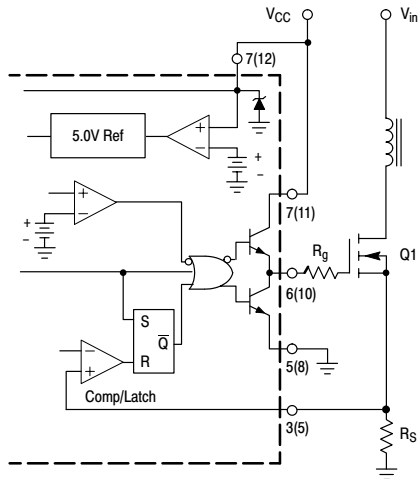
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over-current conditions, a reduction of the  $I_{pk(max)}$  clamp level must be implemented. Refer to Figures 23 and 25.

**Figure 26. Current Sensing Power MOSFET**



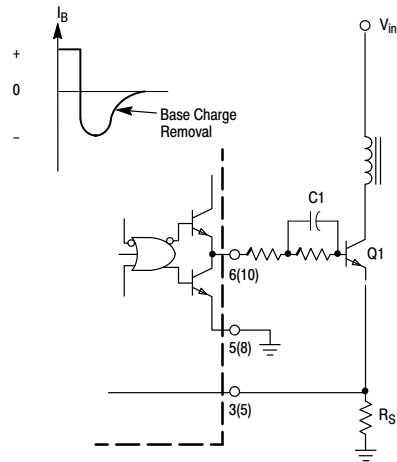
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

**Figure 27. Current Waveform Spike Suppression**



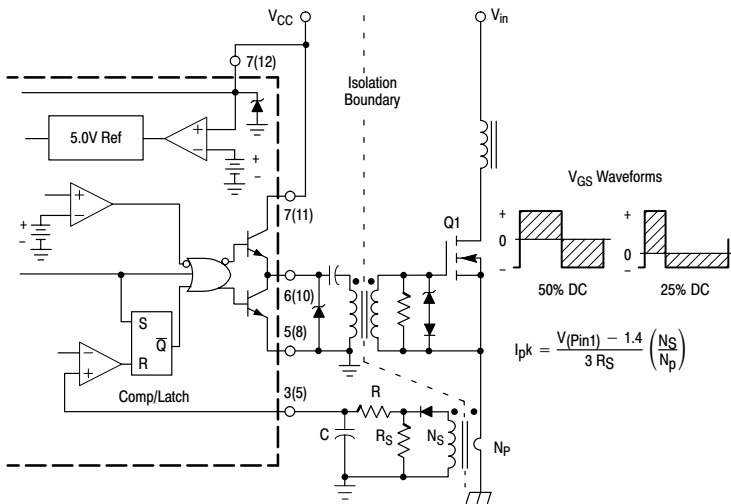
Series gate resistor  $R_g$  will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

**Figure 28. MOSFET Parasitic Oscillations**

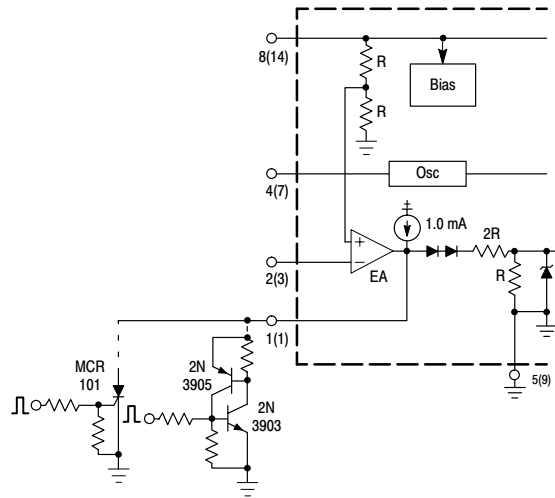


The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor  $C_1$ .

**Figure 29. Bipolar Transistor Drive**

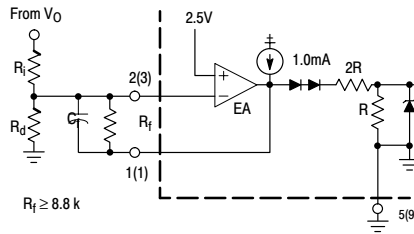


**Figure 30. Isolated MOSFET Drive**

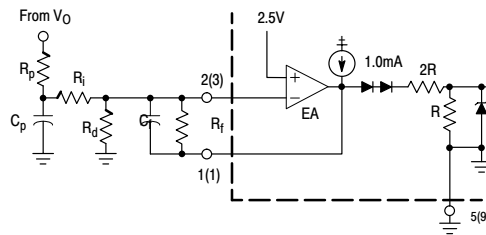


The MCR101 SCR must be selected for a holding of  $< 0.5 \text{ mA}$  @  $T_{A(\text{min})}$ . The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

**Figure 31. Latched Shutdown**

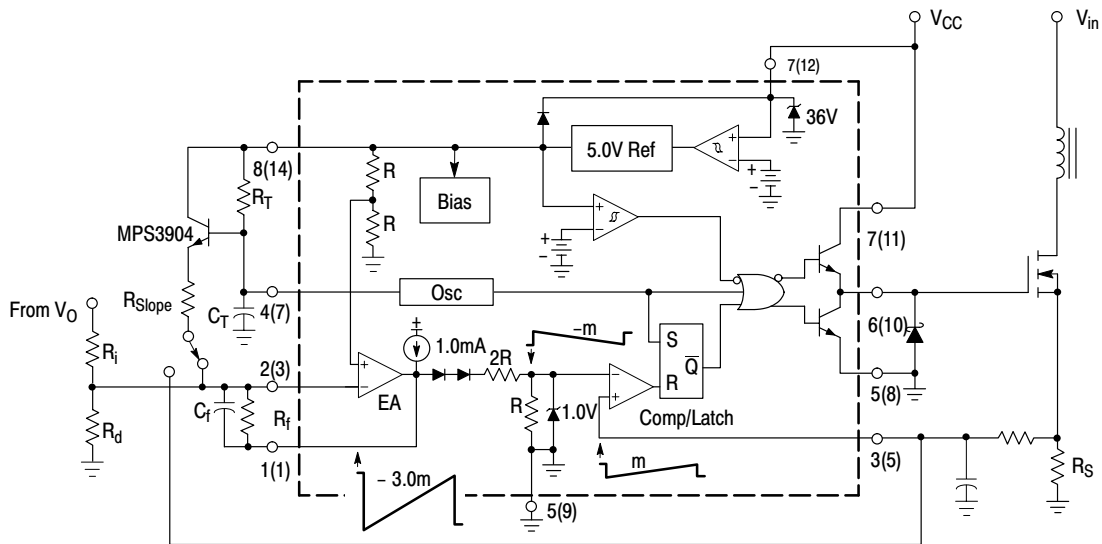


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



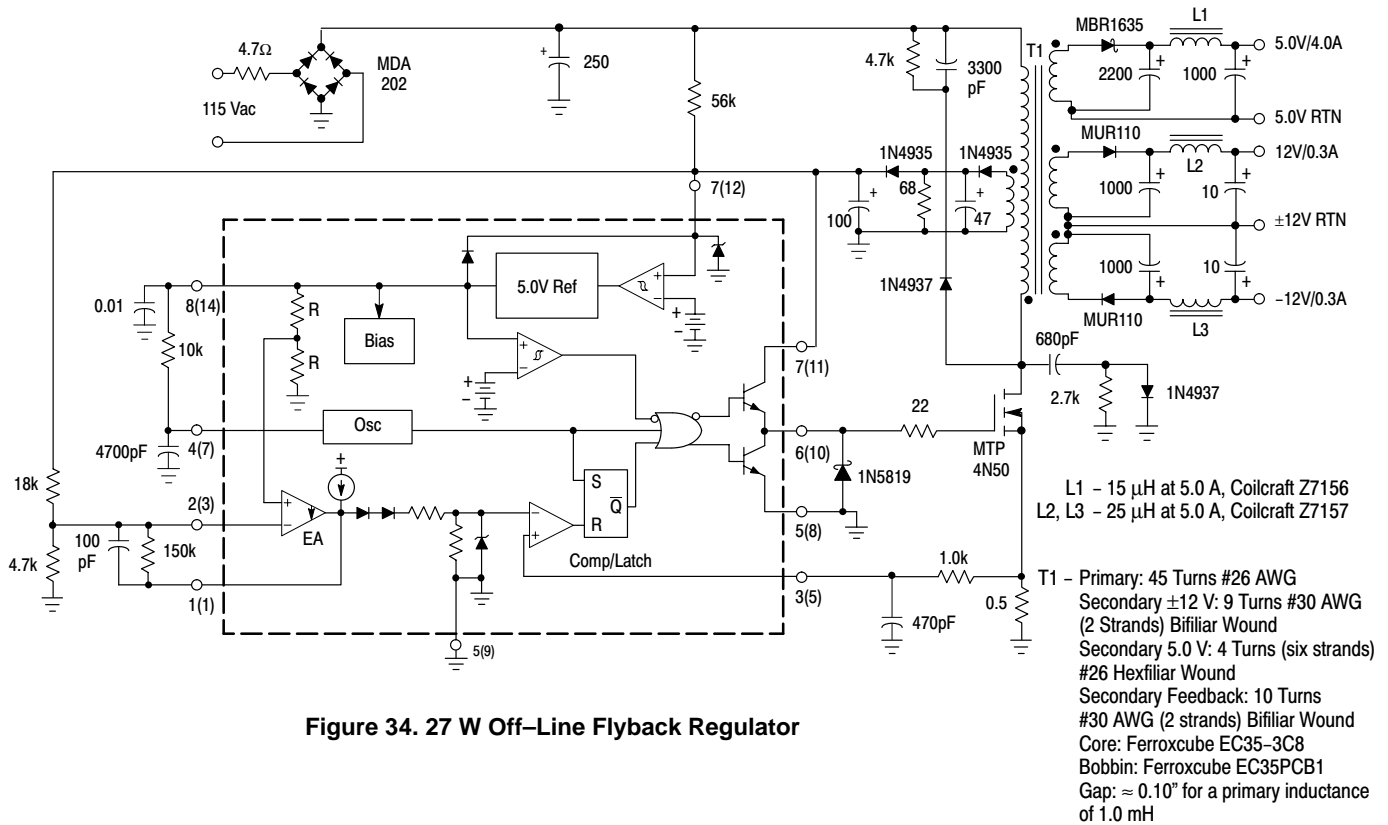
Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

**Figure 32. Error Amplifier Compensation**



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

**Figure 33. Slope Compensation**



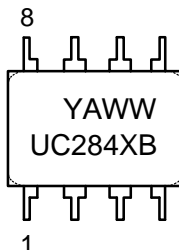
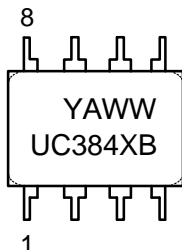
**Figure 34. 27 W Off-Line Flyback Regulator**

Test	Conditions	Results
Line Regulation: 5.0 V $\pm$ 12 V	$V_{in} = 95$ to 130 Vac	$\Delta = 50$ mV or $\pm 0.5\%$ $\Delta = 24$ mV or $\pm 0.1\%$
Load Regulation: 5.0 V $\pm$ 12 V	$V_{in} = 115$ Vac, $I_{out} = 1.0$ A to 4.0 A $V_{in} = 115$ Vac, $I_{out} = 100$ mA to 300 mA	$\Delta = 300$ mV or $\pm 3.0\%$ $\Delta = 60$ mV or $\pm 0.25\%$
Output Ripple: 5.0 V $\pm$ 12 V	$V_{in} = 115$ Vac	40 mV <sub>pp</sub> 80 mV <sub>pp</sub>
Efficiency	$V_{in} = 115$ Vac	70%

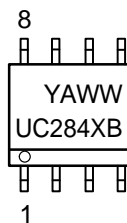
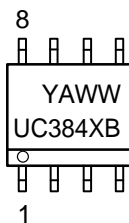
All outputs are at nominal load currents, unless otherwise noted

## Marking Diagrams

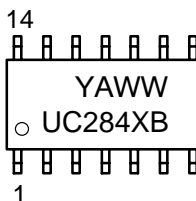
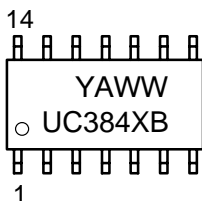
### DIP-8



### SOP-8



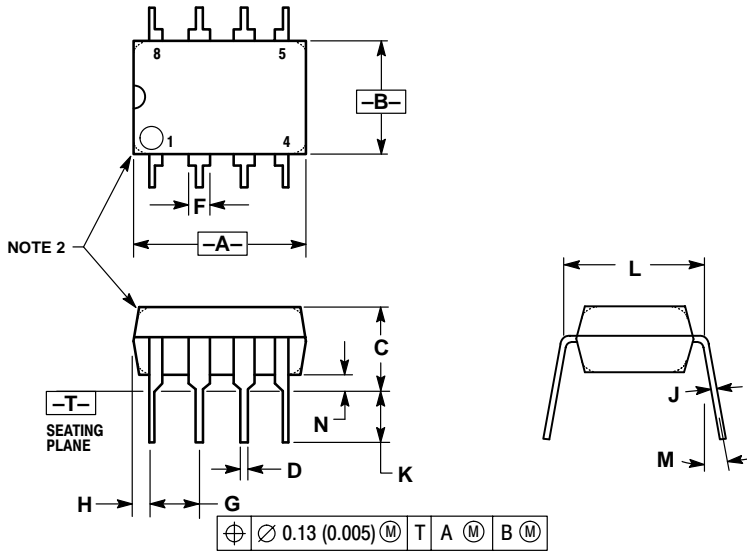
### SOP-14



Y = Year  
 A = Assembly Location  
 WW = Work Week  
 UCX84XB = Device Code  
 x = 2, 3, 4 or 5

## Package Dimensions

### DIP-8

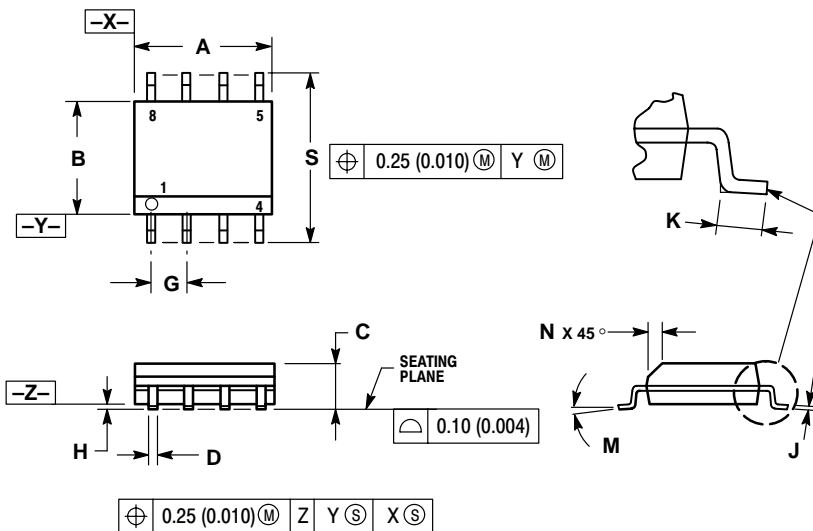


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

### SOP-8



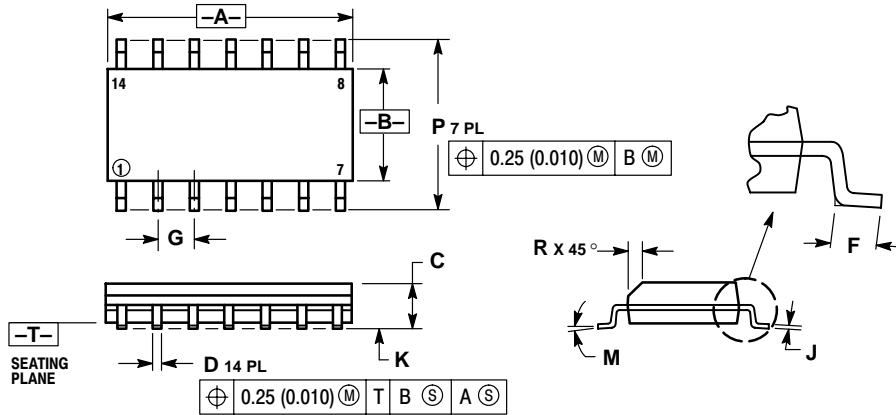
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## Package Dimensions

SOP-14



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019