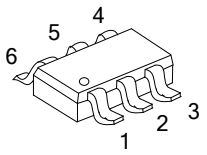
UC3833L

LINEAR INTEGRATED CIRCUIT

ADVANCED GREEN-MODE PWM CONTROLLER WITH FREQUENCY TRIPLE FOR PEAK POWER



SOT-26

■ DESCRIPTION

The UTC **UC3833L** is a high performance current Mode PWM controller, which is built-in with frequency triple, multi-protections and EMI-improved solution in a SOT-26 package. It's ideal for applications requiring a cost-effective solution, minimum component counts and circuit space.

The internal slope compensation improves system stability at high PWM duty cycle output. The UTC **UC3833L** incorporates frequency triple function and adjustable OLP timer to handle the peak power with delay time. The frequency triple function can reduce the transformer flux and core size.

Furthermore, the frequency swapping function is to reduce the noise level and thus helps the power circuit designers for EMI suppression with minimum amount of component cost and developing time.

■ FEATURES

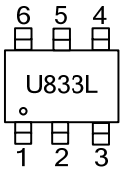
* Very low startup current (<18μA)
* Ultra low operating current at light load (<1mA)
* Frequency triple for peak power (195kHz)
* Adjustable soft start time
* Adjustable OLP (over load protection) delay timer(automatic recovery)
* UVLO (Under Voltage Lockout)
* LEB (Leading-Edge Blanking) on CS Pin
* Current mode control with Green Mode Operation out pin clamping
* OVP (Over Voltage Protection) on V_{DD} Pin (latch shut down in UTC **UC3833L**)
* Internal frequency swapping for EMI improved
* ON-Chip OTP (Over Temperature Protection, latch shut down in UTC **UC3833L**)

■ ORDERING INFORMATION

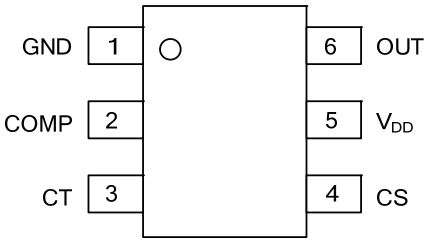
Ordering Number	Package	Packing
UC3833LG-AG6-R	SOT-26	Tape Reel

UC3833LG-AG6-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AG6: SOT-26 (3) G: Halogen Free and Lead Freee

■ MARKING



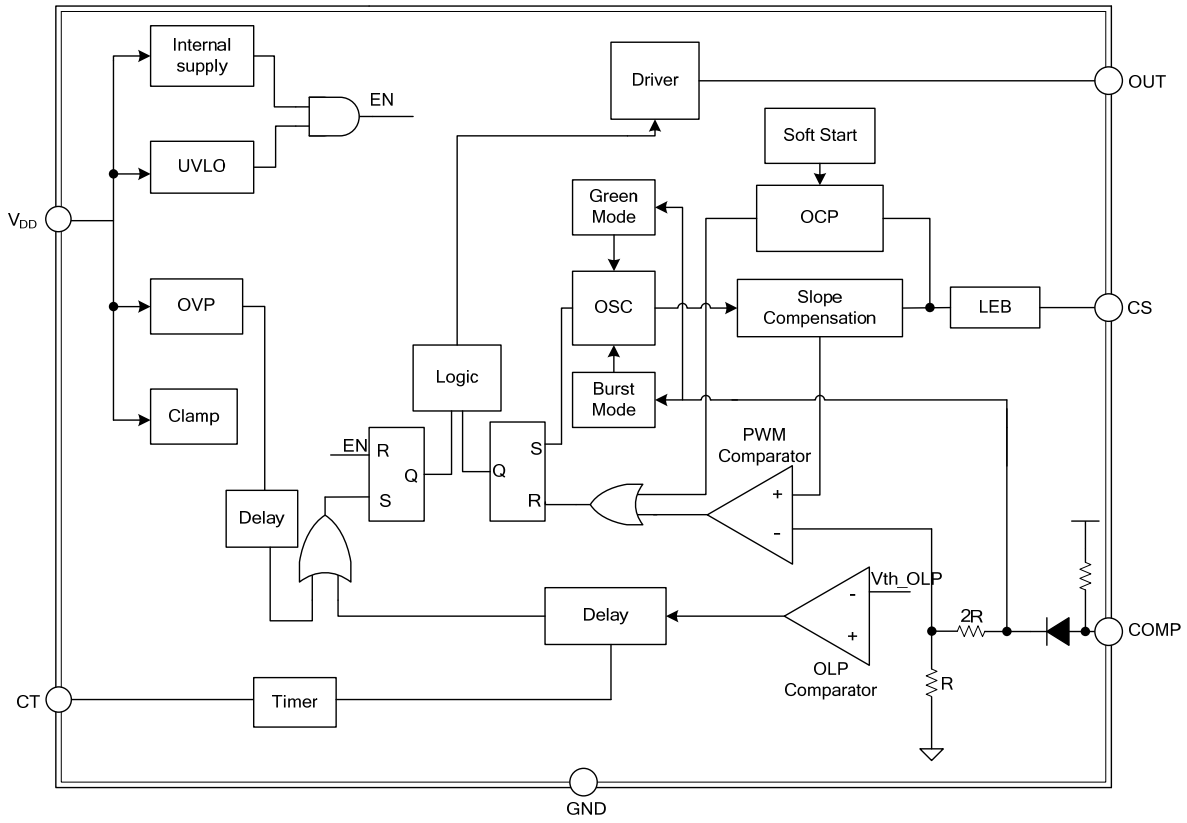
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground
2	COMP	Voltage feedback pin, connect a photo-coupler to close the control loop and achieve the regulation.
3	CT	This pin is to program the frequency of the low frequency timer. connecting a capacitor to ground sets the trembling frequency and OLP delay time.
4	CS	Current sense pin, connect it to sense the MOSFET current
5	V_{DD}	Supply voltage pin
6	OUT	Gate drive output to drive the external MOSFET

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C unless otherwise stated)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.3 ~ 32	V
COMP, CT, CS		-0.3 ~ 7	V
OUT		-0.3 ~ V_{CC}+0.3	V
Power Dissipation	P_D	250	mW
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-65 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance	θ_{JA}	500	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	10		24	V
dCOMP Pin Capacitor Value		4.7		220	nF
CT Pin Capacitor Value		0.047		0.47	μF
Operating Ambient Temperature	T_A	-20		+85	°C

■ ELECTRICAL CHARACTERISTICS (V_{CC}=15.0V, T_A=25°C unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (V_{CC} Pin)						
Startup Current	V_{CC}	V_{DD}=$V_{DD(ON)}$-0.5V		2	15	μA
Operating Current (with 1nF Load on OUT Pin)	$I_{CC(OPR)}$	V_{FB}=3.5V		1.5	2.5	mA
Start Threshold Voltage	$V_{THD(ON)}$		18	20	22	V
Min. Operating Voltage	$V_{DD(MIN)}$		6.5	8	9.5	V
V_{CC} Over Voltage Protection Threshold	V_{OVP}		25	27	29	V
V_{DD} Over Voltage Protection	V_{DD_CLAMP}	$I_{\_CLAMP}$=20mA	28	30	32	V
Latch Release Threshold	V_{TH_LATCH}	UTC UC3833L		4.6		V
Voltage Feedback (Comp Pin)						
Open Loop Voltage		COMP Pin Open		5.4		V
Peak Load Mode Threshold Voltage		F_{SW}=FREQ1		3.1		V
Normal Mode Threshold Voltage		F_{SW}=FREQ2		2.6		V
Burst-Mode Out FB Voltage	$V_{FB(OUT)}$	V_{CS} =0		1.8		V
Burst-Mode Enter FB Voltage	$V_{FB(IN)}$	V_{CS} =0		1.6		V
Current Sensing (CS Pin)						
Peak Current Flat Threshold Voltage	V_{CS-F}			0.92		V
Peak Current Valley Threshold Voltage	V_{CS-V}	V_{FB}=3.9V, Duty=0%	0.68	0.74	0.8	V
Leading Edge Blanking Time	T_{LEB}		200	350	500	ns
Oscillator for Switching Frequency						
Peak Load Mode Frequency	FREQ1		180	195	210	KHz
Normal Mode Frequency	FREQ2		60	65	70	KHz
Green Mode Frequency	FREQG		20			KHz
Trembling Frequency			-9		+9	%
Temp. Stability		(-20°C~110°C)			10	%
Voltage Stability		(V_{CC}=10V-25V)			10	%
Gate Drive Output (OUT Pin)						
Output Low Level	V_{OL}	V_{CC}=15V, Io=20mA			0.8	V
Output High Level	V_{OH}	V_{CC}=15V, Io=20mA	10			V
Output Clamp Level		V_{CC}=20V		16		V
Rising Time	T_R	Load Capacitance=1000pF		100		ns
Falling Time	T_F	Load Capacitance=1000pF		60		ns
Max. Duty			70	80	90	%
OLP (Over Load Protection)						
OLP Trip Level		Vcomp (OLP)		4.2		V
OLP Delay Time		CT Pin=0.047μF	30	40	50	ms
On Chip OTP (Over Temperature)						
OTP Level				140		°C
Soft Start Duration						
Soft Start Duration		CT Pin=0.047μF		6		ms

■ OPERATION DESCRIPTION

The UTC **UC3833L** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC **UC3833L** series.

Startup Current and Start up Control

Startup current of UTC **UC3833L** is designed to be very low so that V_{DD} could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adapter with universal input range design, a 2MΩ, 1/2 W startup resistor could be used together with a V_{DD} capacitor to provide a fast startup and yet low power dissipation design solution.

Power-Saving Mode Operation

The proprietary Power-Saving Mode function provides linearly decreasing the switching frequency under light-load conditions for higher efficiency. The feedback voltage, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback voltage dropped below the threshold voltage, the switching frequency starts to decrease. This Power-Saving Mode function dramatically reduces power consumption under light-load conditions. The 22KHz minimum frequency control also eliminates the audio noise at any loading conditions.

At zero load condition, the magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. The UTC **UC3833L** enter burst mode at standby condition to minimize the switching loss and reduces the standby power consumption. Power supplies using the UTC **UC3833L** can easily meet even the strictest regulations regarding standby power consumption.

Switch Frequency Set

The UTC **UC3833L** is an advanced Green Mode PWM controller which built-in with frequency triple as followed Fig.1. The typical frequency is fixed to 65KHz and Switch frequency is modulated by output power P_{OUT} during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower switch frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, The IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between f_{SW} and $P_{OUT}/P_{OUT\ (MAX)}$ as followed Fig.2.

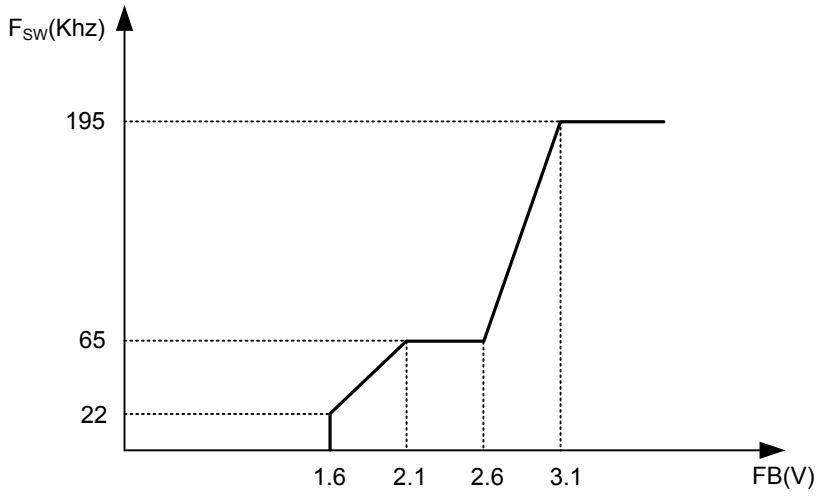


Fig.1 Frequency tripple

■ OPERATION DESCRIPTION (Cont.)

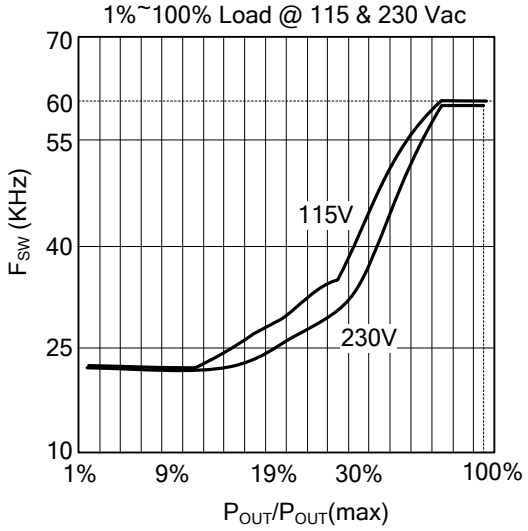


Fig.2 The relation curve between f_{SW} and relative output power P_{OUT}/ $P_{OUT\ (MAX)}$

Frequency Hopping For EMI Improvement

The Frequency hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed Fig.3. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

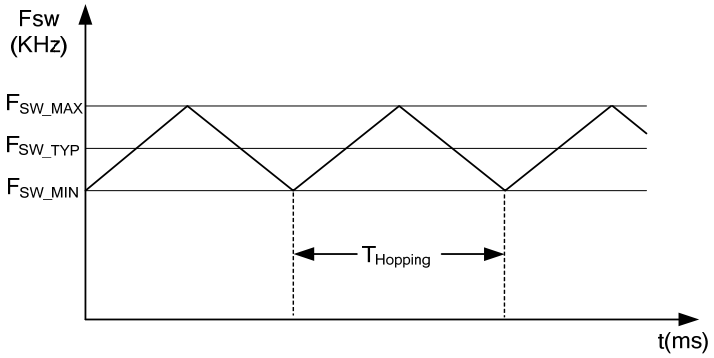


Fig.3 Frequency Hopping

Built-in Slope Compensation

Built-in slope compensation circuit greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation.

Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a T_{LEB} time leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

■ OPERATION DESCRIPTION (Cont.)

Constant Output Power Limit

When the SENSE voltage, across the sense resistor R_S, reaches the threshold voltage, around V_{CS-V}, the output GATE drive will be turned off after a small propagation delay t_D. This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate this variation for wide AC input range, the threshold voltage is adjusted by the V_{IN} current. Since V_{IN} pin is connected to the rectified input line voltage through a resistor R_{VIN}, a higher line voltage will generate higher V_{IN} current into the V_{IN} pin. The threshold voltage is decreased if the V_{IN} current is increased. Smaller threshold voltage, forces the output GATE drive to terminate earlier, thus reduce the total PWM turn-on time and make the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for wide AC input voltage from 90VAC to 264VAC.

Under Voltage Lockout (UVLO)

The turn-on and turn-off thresholds of the UTC **UC3833L** are fixed internally at $V_{THD(ON)}/V_{DD(MIN)}$ During start-up, the hold-up capacitor must be charged to $V_{THD(ON)}$ through the start-up resistor, so that the UTC **UC3833L** will be enabled. The hold-up capacitor will continue to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below $V_{DD(MIN)}$ during this start-up process. This UV

Output

The UTC **UC3833L** output stage is a fast totem pole gate driver. Cross conduction has bee LO hysteresis window ensures that hold-up capacitor will be adequate to supply V_{DD} during start-up. avoided to minimize heat dissipation, increase efficiency, and enhance reliability. A good tradeoff is achieved through dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 16V clamp is added for MOSFET gate protection at higher than expected V_{DD} input.

Protection Controls

The IC takes on more protection functions such as OVP, OLP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. Driver is reset after failure is eliminated.

OVP

The OVP will shut down the switching of the power MOSFET whenever V_{DD} >V_{OVP} for continual time. The OVP event as followed Fig.4.

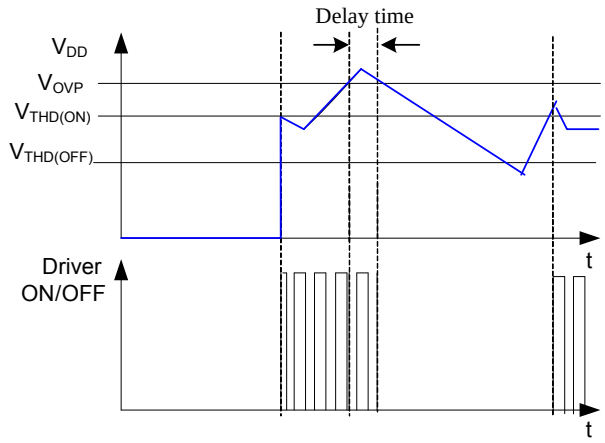


Fig.4 OVP case

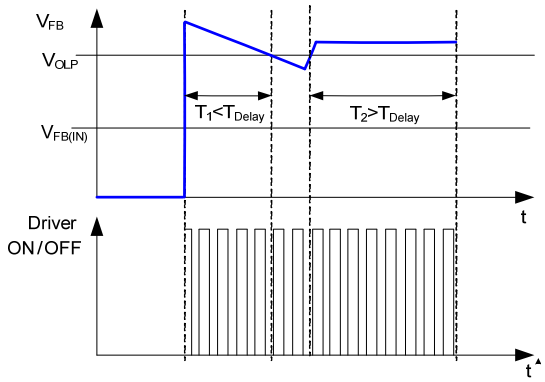


Fig.5 OLP case

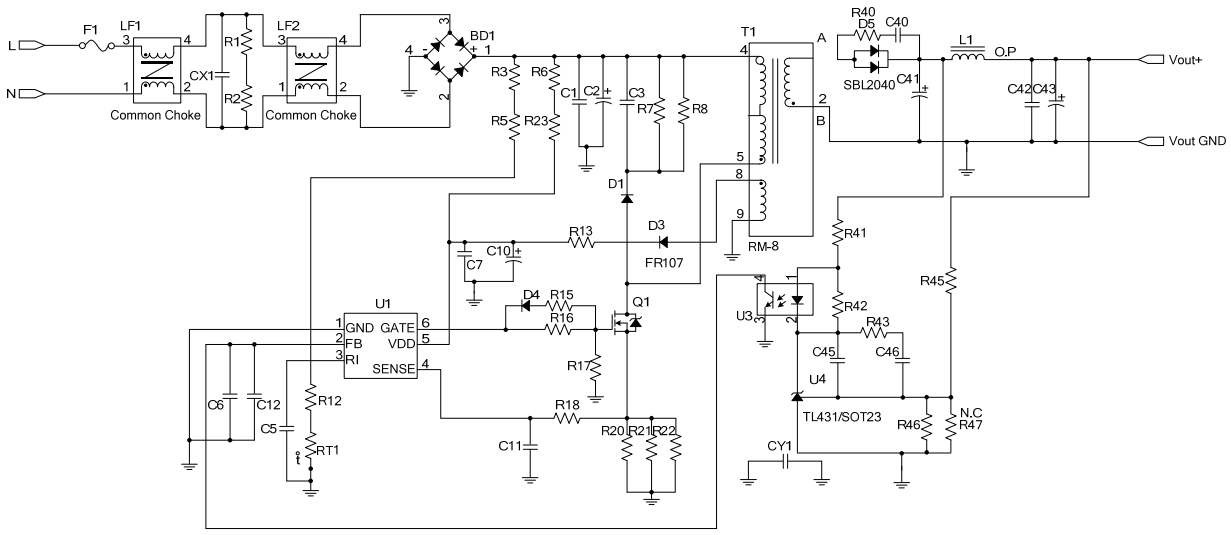
OLP

OLP will shut down driver when V_{FB}> V_{OLP} for continual time. The OLP event as followed Fig.5.

OTP

The internal OTP circuit is implemented to detect the Temperature. As soon as the Temperature is higher than the 140°C, the driver will shut down.

■ TYPICAL APPLICATION CIRCUIT (19V / 2.05A)

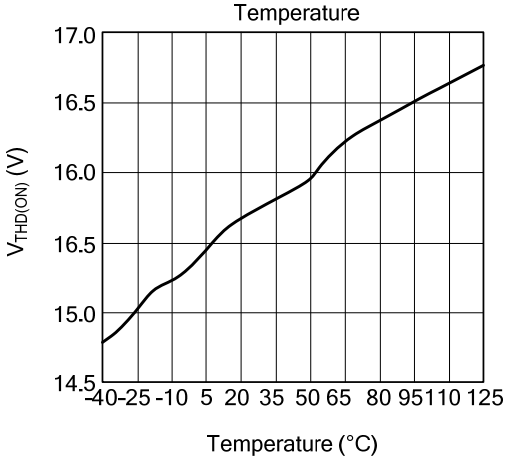


BOM

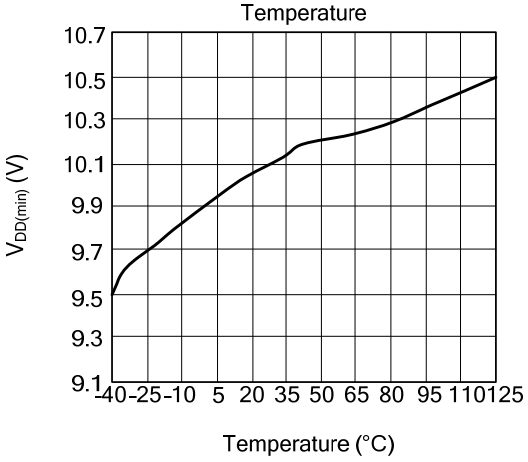
Reference	Component	Reference	Component
F1	2A/250V	C11	68pF/50V X7R SMD
FL1, FL2	Choke	C6, C12	1nF/50V X7R SMD
CX1	0.33uF/275V	C5	47n/50V X7R SMD
BD1	2A/600V	U1	IC , PWM controller **UC3833L** SOT-26
C2	EC 33uF/400V 105°C ±20%	D4	1N4148, 0.15A/75V, SMD
C10	EC 10uF/50V 105°C ±20%	D3	BAV20WG, 1A/200V,SOD-123
Q1	MOSFET,10A/650V	D1	1N4007, 1A/1000V, SMA
T1	RM-8	U3	IC, TL431
CY1	Y1, 1000pF/400V, 105°C, ±20%	U4	IC, Opto-Coupler, LTV-357-T-C, SMD
D5	Schottky, 20A/100V	R40	47Ω SMD
C41, C43	EC 680uF/25V, 105°C, ±20%	R41	820Ω SMD
L1	Choke	R42	2.2K SMD
R1, R2	1.5M SMD	R43	680Ω SMD
R6, R23	1.5M SMD	R45	68K SMD
R20	1.8Ω SMD	R46	10K SMD
R21, R22	1.5Ω SMD	C45	10nF/50V, X7R, SMD
R13	2.2Ω SMD	C46	0.1uF/50V, X7R, SMD
R7, R8	180K SMD	C40	100pF/1KV, NPO, SMD
R18	1K SMD	C42	N.C
R15	10Ω SMD	R47	N.C
R16	47Ω SMD	R3, R5	N.C
R17	10K SMD	R12	N.C
C1, C3	1nF/1KV X7R SMD	RT1	N.C
C7	0.1uF/50V X7R SMD		

■ TYPICAL CHARACTERISTICS

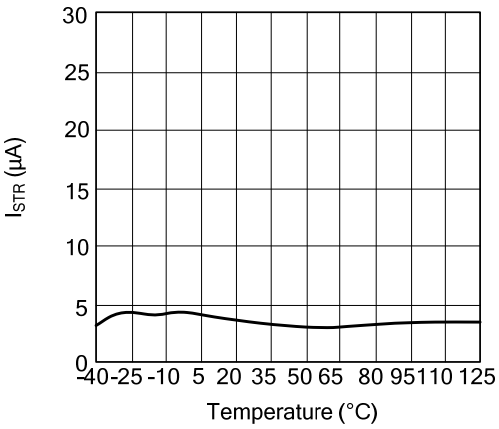
Start-up Threshold Voltage ($V_{THD(ON)}$) vs. Temperature



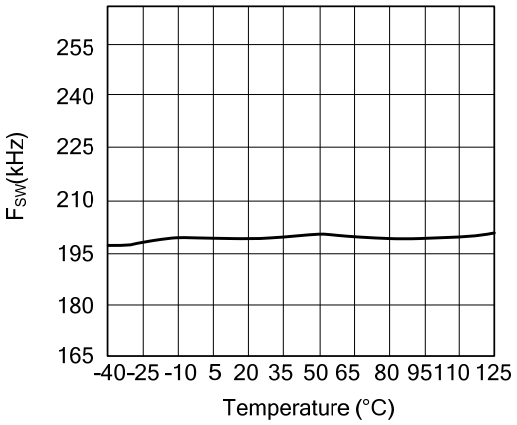
Min. Operating Voltage ($V_{DD\ (min)}$) vs. Temperature



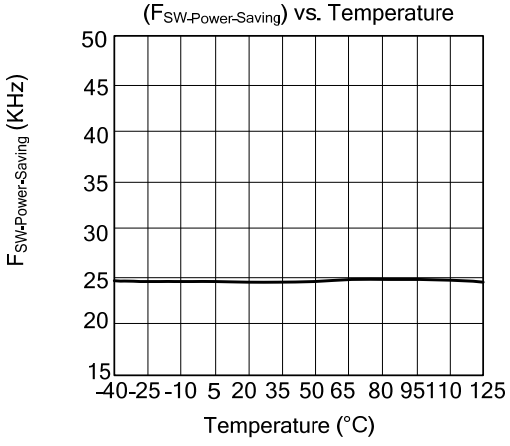
Start-up Crrent (I_{STR}) vs. Temperature



Switch Frequency (F_{SW}) vs. Temperature



Frequency in Power-Saving mode ($F_{SW\text{-}Power\text{-}Saving}$) vs. Temperature



Max. Duty Cycle (D_{MAX}) vs. Temperature