



■ **Features:**

- Vcc operation voltage : 3.0 V~ 3.6V
- Low power consumption :
20mA (Max.) operating current
2uA (Typ.) CMOS standby current
- High Speed Access time :
25ns (Max.) at Vcc = 3.0V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Data retention supply voltage as low as 1.2V
- Easy expansion with CE\ and OE\ options

■ **Description**

The UC62LS4096 is a high performance, low power CMOS Static Random Access Memory organized as 262,144 words by 16 and operates from 3.0V to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 2uA and maximum access time of 25ns in 3.0V operation.

Easy memory expansion is provided enable (CE\), and active LOW output enable (OE\), and three-state output drivers.

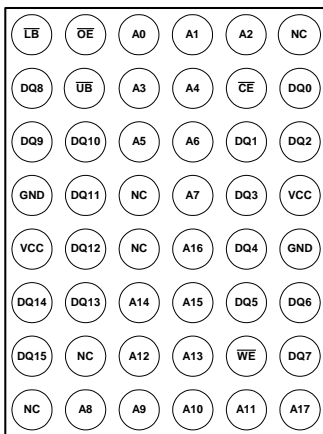
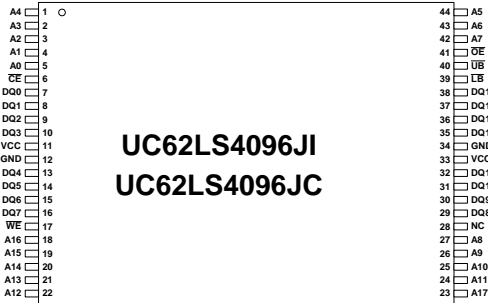
The UC62LS4096 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The UC62LS4096 is available in the JEDEC standard 44 pin TSOP (Type II) and 48 pin mini-BGA.

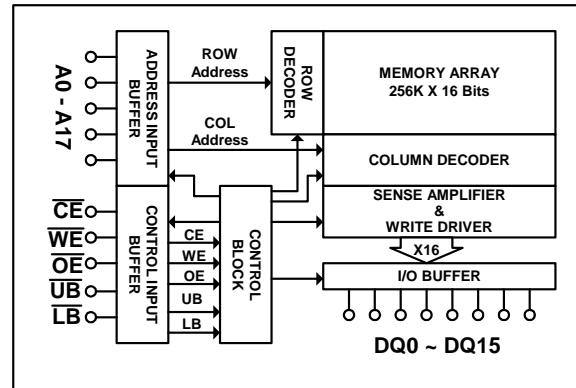
■ **PRODUCT FAMILY**

| Product Family | Operating Temperature | Vcc Range | Speed (ns) | Power Consumption | | Package Type |
|----------------|-----------------------|-------------|----------------|-------------------|----------------|--------------|
| | | | | STANDBY | Operating | |
| | | | Vcc=3.0V(Max.) | Vcc=3.3V(Typ.) | Vcc=3.6V(Max.) | |
| UC62LS4096JC | 0 ~ 70 | 3.0V ~ 3.6V | 20/25 | 2uA | 20mA | TSOPII-44 |
| UC62LS4096KC | | | | | | BGA-48 |
| UC62LS4096AC | | | | | | DICE |
| UC62LS4096JI | -40 ~ 85 | 3.0V ~ 3.6V | 20/25 | 2uA | 20mA | TSOPII-44 |
| UC62LS4096KI | | | | | | BGA-48 |
| UC62LS4096AI | | | | | | DICE |

■ **PIN CONFIGURATIONS**



■ **BLOCK DIAGRAM**



■ PIN DESCRIPTION

| Name | Type | Function |
|-----------------------------------|-------|--|
| A0 – A17 | Input | Address inputs for selecting one of the 262,144 x 16 bit words in the RAM |
| CE \setminus | Input | CE \setminus is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and not in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected. |
| WE \setminus | Input | The Write enable input is active LOW and controls read and write operations. With the chip selected, when WE \setminus is HIGH and OE \setminus is LOW, output data will be present on the DQ pins, when WE \setminus is LOW, the data present on the DQ pins will be written into the selected memory location. |
| OE \setminus | Input | The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when OE \setminus is inactive. |
| UB \setminus and LB \setminus | Input | Lower byte and upper byte data input/output control pins. |
| DQ0 – DQ15 | I/O | These 16 bi-directional ports are used to read data from or write data into the RAM. |
| V _{cc} | Power | Power Supply |
| Gnd | Power | Ground |

■ TRUTH TABLE

| Mode | WE \setminus | CE \setminus | OE \setminus | LB \setminus | UB \setminus | I/O 0 ~ 7 | I/O 8 ~ 15 | V _{cc} Current |
|-----------------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------------------------------------|
| Not Selected | X | H | X | X | X | High Z | High Z | I _{SB1} , I _{SB1} |
| Output Disabled | H | L | H | X | X | High Z | High Z | I _{cc} |
| | X | L | X | H | H | | | |
| Read | H | L | L | L | H | D _{OUT} | High Z | I _{cc} |
| | H | L | L | H | L | High Z | D _{OUT} | |
| | H | L | L | L | L | D _{OUT} | D _{OUT} | |
| Write | L | L | X | L | H | D _{IN} | High Z | I _{cc} |
| | L | L | X | H | L | High Z | D _{IN} | |
| | L | L | X | L | L | D _{IN} | D _{IN} | |

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| SYMBOL | PARAMETER | RATING | UNIT |
|-------------------|--------------------------------------|------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{cc} +0.5 | V |
| T _{BIAS} | Temperature Under Bias | -40 to 125 | |
| T _{STG} | Storage Temperature | -50 to 150 | |
| PT | Power Dissipation | 0.5 | W |
| I _{OUT} | DC Output Current | 10 | mA |

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

| RANGE | AMBIENT TEMPERATURE | V _{cc} |
|------------|---------------------|-----------------|
| Commercial | 0 to 70 | 3.0V ~ 3.6V |
| Industrial | -40 to 85 | 3.0V ~ 3.6V |

■ CAPACITANCE⁽¹⁾(TA=25 °C, f=1.0MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|-----------------|--------------------------|---------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} =0V | 6 | pF |
| C _{DQ} | Input/Output Capacitance | V _{DQ} | 8 | pF |

1. This parameter is guaranteed and not 100% tested.


■ DC ELECTRICAL CHARACTERISTICS (TA=0 to 70)

| Symbol | Comment | Test Condition | MIN. | TYP. ⁽¹⁾ | MAX. | UNITS |
|------------------|--|---|------|---------------------|----------------------|-------|
| V _{IL} | Guaranteed Input Low Voltage ⁽²⁾ | V _{CC} =2.4V | -0.5 | - | 0.8 | V |
| V _{IH} | Guaranteed Input High Voltage ⁽²⁾ | V _{CC} =3.6V | 2.0 | - | V _{CC} -0.2 | V |
| I _L | Input Leakage Current | V _{CC} =3.6V V _{IN} =0V to V _{CC} | - | - | 1 | uA |
| I _{OL} | Output Leakage Current | V _{CC} =3.6V CE\=V _{IH} or OE\=V _{IH} V _{IO} =0V t V _{CC} | - | - | 1 | uA |
| V _{OL} | Output Low Voltage | V _{CC} =3.6V, I _{OL} =2mA | - | - | 0.4 | V |
| V _{OH} | Output High Voltage | V _{CC} =3.0V, I _{OH} =-1mA | 2.4 | - | - | V |
| I _{CC} | Operating Power Supply Current | CE\=V _{IL} , I _{DQ} =0mA, F=F _{max} ⁽³⁾ | - | - | 20 | mA |
| I _{SB1} | TTL Standby Current | CE\=V _{IH} , V _{IN} =V _{IH} to V _{IL} | - | - | 1 | mA |
| I _{SB2} | CMOS Standby Current | CE\ V _{CC} -0.2V, V _{IN} =V _{CC} -0.2V or 0.2V, F=0 ⁽⁴⁾ | - | 2 | 10 | uA |

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3. F_{max} = 1/t_{RC} .

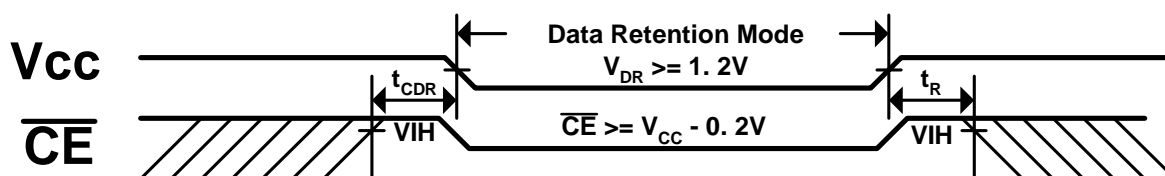
4. F=0 means input signals must be keep in static state.

■ DATA RETENTION CHARACTERISTICS (TA=0 to 70)

| Symbol | Comment | Test Condition | MIN. | TYP. ⁽¹⁾ | MAX. | UNITS |
|-------------------|--------------------------------------|---|--------------------------------|---------------------|------|-------|
| V _{DR} | V _{CC} to Data Retention | CE\ V _{CC} - 0.2V V _{IN} V _{CC} -0.2V or V _{IN} 0.2V | 1.2 | - | - | V |
| I _{CCDR} | Data Retention Current | CE\ V _{CC} - 0.2V V _{IN} V _{CC} -0.2V or V _{IN} 0.2V | - | 0.1 | 1 | uA |
| t _{DR} | Chip Deselect to Data Retention Time | See Retention Waveform | 0 | - | - | ns |
| t _R | Operation Recovery Time | | T _{RC} ⁽²⁾ | - | - | ns |

1. V_{CC} = 1.5V, TA = 25 .

2. t_{RC} = Read Cycle Time

■ LOW VCC DATA RETENTION WAVEFORM⁽¹⁾ (CE\ Controlled)




**Low Power CMOS SRAM
256K X 16**

**UC62LS4096
-20/-25**

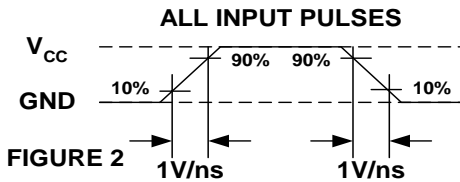
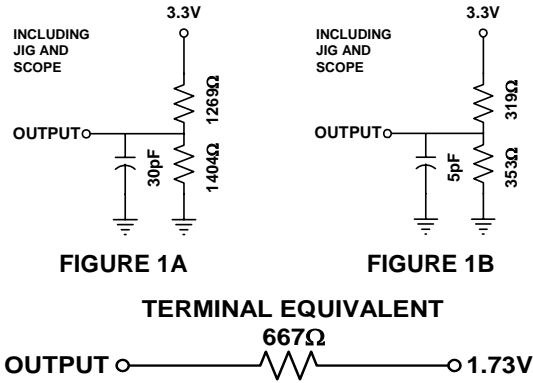
AC TEST CONDITIONS

| | |
|---|--------------------|
| Input Pulse Levels | VCC to 0V |
| Input Rise and Fall Times | 1V/ns |
| Input and Output Timing Reference Level | 0.5V _{CC} |

KEY TO SWITCHING WAVEFORMS

| WAVEFORMS | INPUTS | OUTPUTS |
|-----------|---------------------------------|---|
| | MUST BE STEADY | MUST BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGE FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGE FROM L TO H |
| | DON'T CARE ANY CHANGE PERMITTED | CHANGE STATE UNKNOWN |
| | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE OFF STATE |

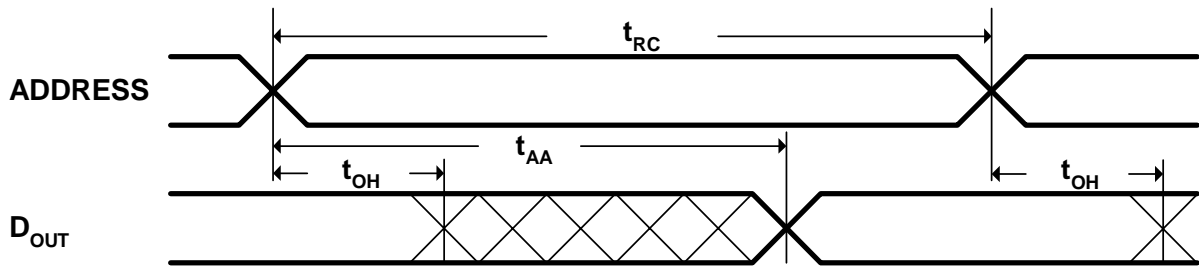
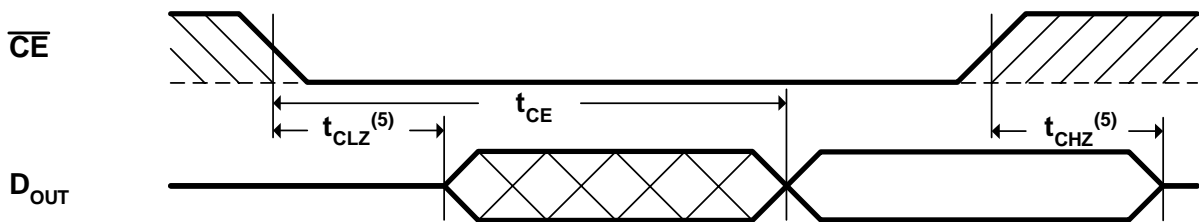
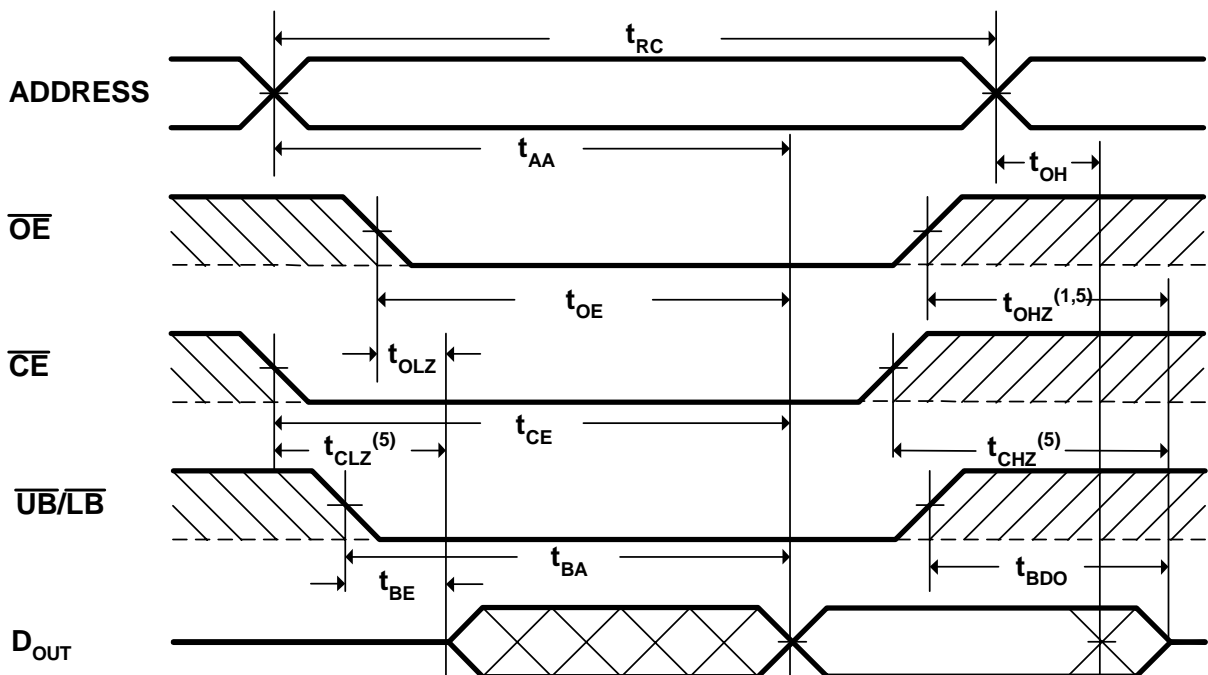
AC TEST LOADS AND WAVEFORMS



AC ELECTRICAL CHARACTERISTICS (TA=0 to 70 , VCC=3.0V~3.6V)

READ CYCLE

| JEDEC PARAMETER NAME | PARAMETER NAME | DESCRIPTION | UC62LS4096-20 | | | UC62LS4096-25 | | | UNIT |
|----------------------|------------------|------------------------------------|---------------|-----|-----|---------------|-----|-----|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| t _{AVAX} | t _{RC} | Read Cycle Time | 20 | - | - | 25 | - | - | ns |
| t _{AVQV} | t _{AA} | Address Access Time | - | - | 20 | - | - | 25 | ns |
| t _{ELQV} | t _{CE} | Chip Select Access Time | - | - | 20 | - | - | 25 | ns |
| t _{BA} | t _{BA} | Data Byte Control Access Time | | | 10 | | | 10 | ns |
| t _{GLQV} | t _{OE} | Output Enable to Output Valid | - | - | 10 | - | - | 10 | ns |
| t _{ELQX} | t _{CLZ} | Chip Select to Output Low Z | 5 | - | - | 5 | - | - | ns |
| t _{GLQX} | t _{OLZ} | Output Enable to Output Low Z | 3 | - | - | 3 | - | - | ns |
| t _{BE} | t _{BE} | Data Byte Control To Output Low Z | 5 | | | 5 | | | ns |
| t _{EHQZ} | t _{CHZ} | Chip Deselect to Output in High Z | - | - | 10 | - | - | 10 | ns |
| t _{GHQZ} | t _{OHZ} | Output Disable to Output in High Z | - | - | 10 | - | - | 10 | ns |
| t _{BDO} | t _{BDO} | Data Byte Control To Output High Z | - | | 10 | - | | 10 | ns |
| t _{AXOX} | t _{OH} | Address Chang to Output Change | 5 | - | - | 5 | - | - | ns |


SWITCHING WAVEFORMS (READ CYCLE)
READ CYCLE1 ^(1,2,4)

READ CYCLE2 ^(1,3,4)

READ CYCLE3 ^(1,4)

NOTES:

1. WE is high in read cycle.
2. Device is continuously selected when $\overline{CE} = \text{VIL}$
3. Address valid prior to or coincident with \overline{CE} transition low.
4. $\overline{OE} = \text{VIL}$.
5. Transition is measured $\pm 500\text{mV}$ from steady state with $CL=5\text{pF}$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.



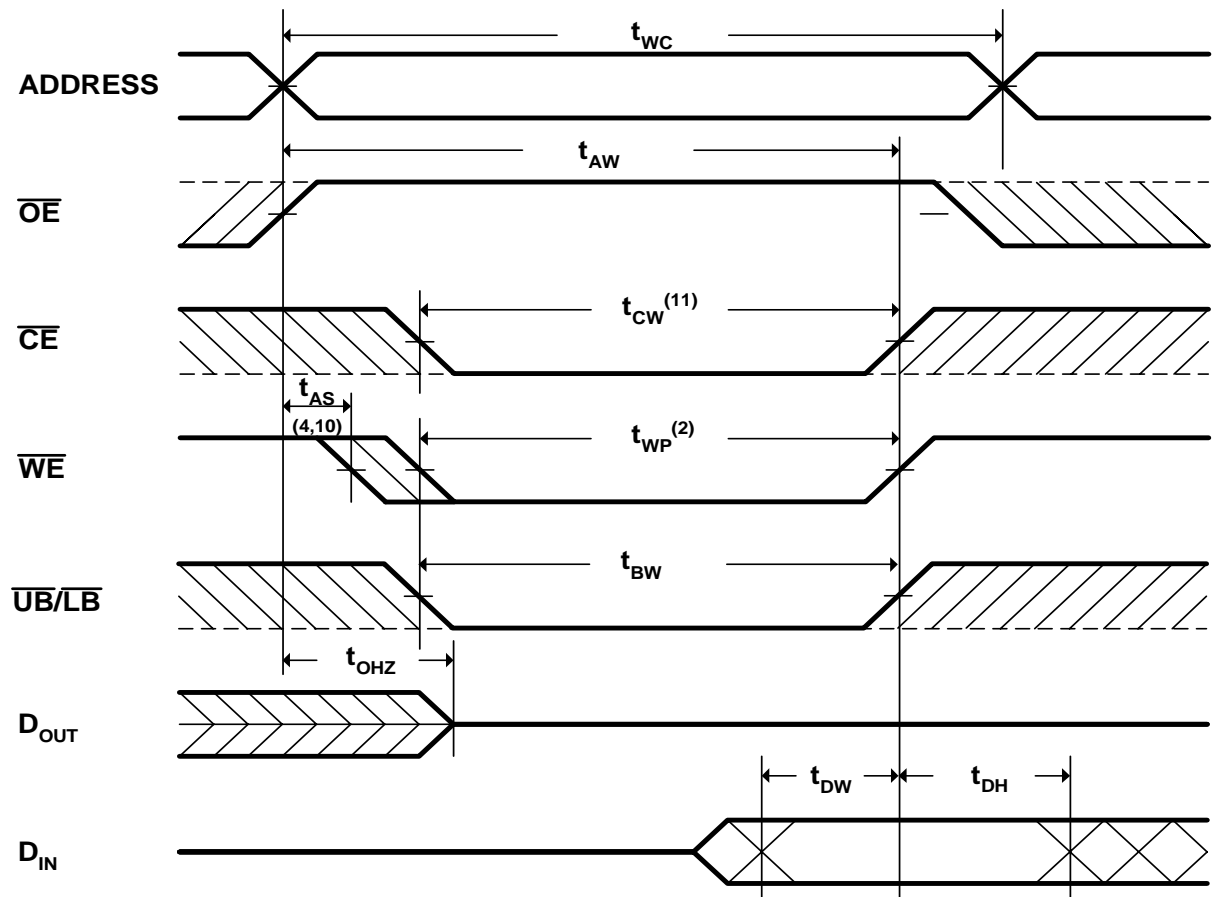
■ **AC ELECTRICAL CHARACTERISTICS (TA=0 to 70 , VCC=3.0V~3.6V)**

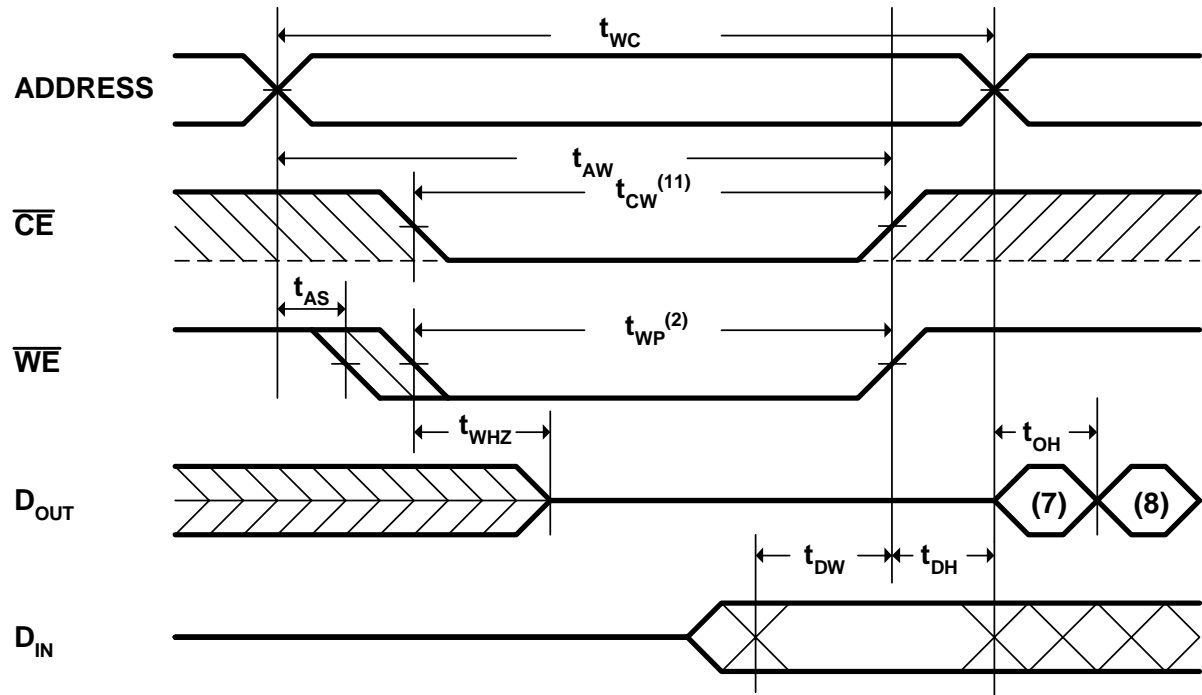
WRITE CYCLE

| JEDEC PARAMETER NAME | PARAMETER NAME | DESCRIPTION | UC62LS4096-20 | | | UC62LS4096-25 | | | UNIT |
|----------------------|------------------|------------------------------------|---------------|-----|-----|---------------|-----|-----|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| t _{AVAX} | t _{WC} | Write Cycle Time | 20 | - | - | 25 | - | - | ns |
| t _{E1LWH} | t _{CW} | Chip Select to END of Write | 15 | - | - | 15 | - | - | ns |
| t _{AVWL} | t _{AS} | Address Setup Time | 0 | - | - | 0 | - | - | ns |
| t _{AVWH} | t _{AW} | Address valid to End of Write | 15 | - | - | 15 | - | - | ns |
| t _{BW} | t _{BW} | Data Byte Control End of Write | 15 | - | - | 15 | - | - | Ns |
| t _{WLWH} | t _{WP} | Write Pulse Width | 15 | - | - | 15 | - | - | ns |
| t _{WHAX} | t _{WR} | Write Recovery Time | 0 | - | - | 0 | - | - | ns |
| t _{WLOZ} | t _{WHZ} | Write to Output in High Z | - | - | 8 | - | - | 10 | ns |
| t _{DVWH} | t _{DW} | Data to Write Time Overlap | 8 | - | - | 10 | - | - | ns |
| t _{WHDX} | t _{DH} | Data Hold Time for Write End | 0 | - | - | 0 | - | - | ns |
| t _{GHOZ} | t _{OHz} | Output Disable to Output In High Z | - | - | 8 | - | - | 10 | ns |
| t _{WHQX} | t _{OW} | End of Write to Output Active | 5 | - | - | 5 | - | - | ns |

■ **SWITCHING WAVEFORMS (WRITE CYCLE)**

WRITECYCLE1⁽¹⁾




WRITE CYCLE2^(1,6)

NOTES:

1. WE\ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE\ and WE\ low. All signals must be active to initiate a write and any one can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of CE\ or WE\ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE\ low transition occurs simultaneously with the WE\ low transitions or after the WE\ transition, output remain in a high impedance state.
6. OE\ is continuously low ($OE\ = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CE\ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured 500mV from steady state with $C_L = 5pF$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. TCW is measured from the later of CE\ going low to the end of write.



■ ORDERING INFORMATION

UC62LS4096 AB -- YY

A => GRADE

J :TSOP(II)

K :BGA

A :DICE

B => GRADE

C :COMMERCIAL (0 ~ 70)

I :INDUSTRIAL (-40 ~ 85)

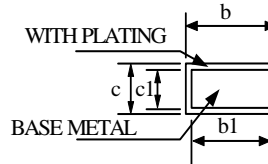
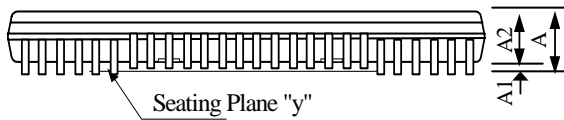
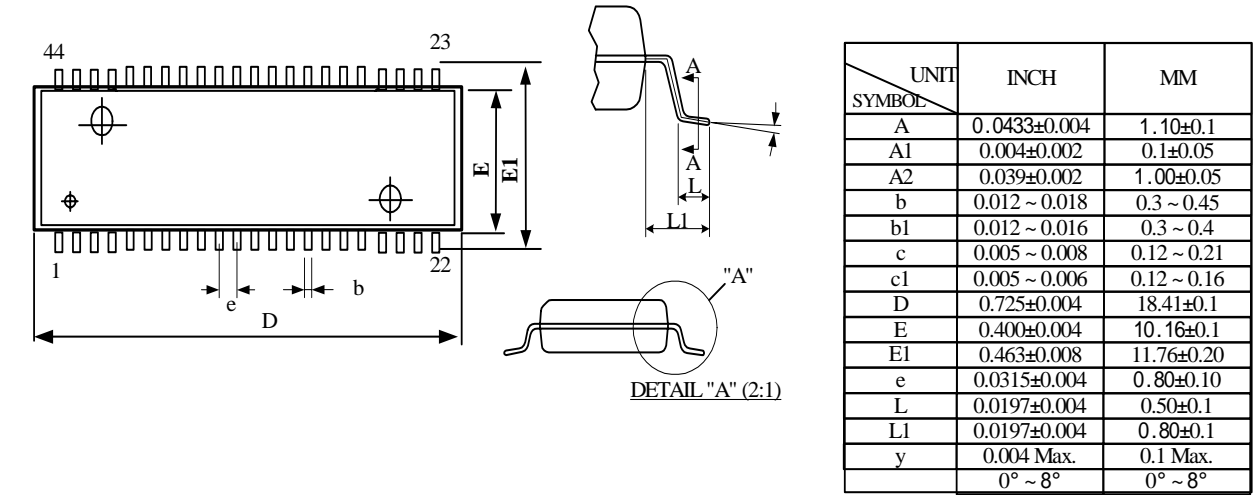
YY => SPEED

20: 20ns

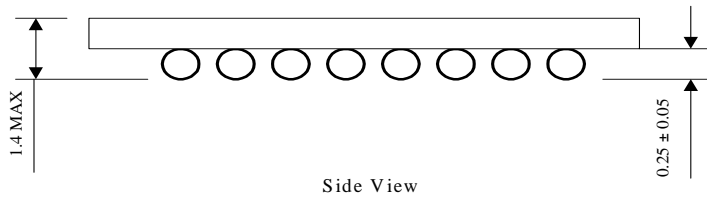
25: 25ns



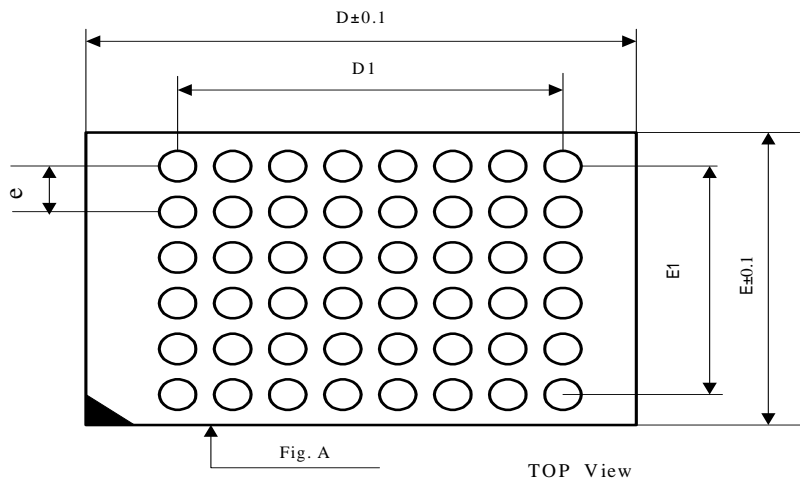
PACKAGE DIMENSIONS



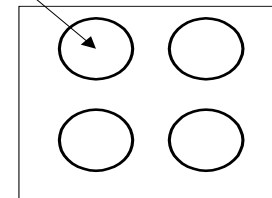
TSOPII - 44



| Ball pitch e=0.75 | | | |
|-------------------|-----|------|------|
| D | E | D1 | E1 |
| 8.0 | 6.0 | 5.25 | 3.75 |



Solder Ball diameter = 0.35 ± 0.05



48 Mini-BGA 6*8mm