■ Features:

- Vcc operation voltage : 1.5 V~ 3.6V
- Low power consumption :
  35mA (Max.) operating current
  2uA (Typ.) CMOS standby current
- High Speed Access time :
  70ns (Max.) at Vcc = 1.5V
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Data retention supply voltage as low as 1.2V
- Easy expansion with CE\ and OE\ options

■ Description

The UC62LV4096 is a high performance, low power CMOS Static Random Access Memory organized as 262,144 words by 16 and operates from 1.5 V to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 2uA and maximum access time of 70ns in 1.5V operation.

Easy memory expansion is provided enable (CE\), and active LOW output enable (OE\) and three-state output drivers.

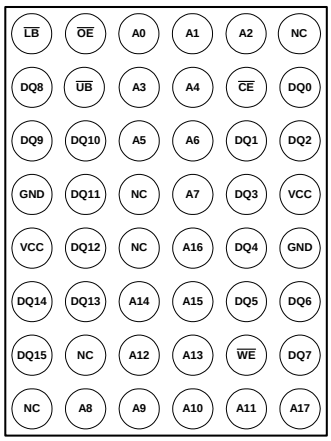
The UC62LV4096 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The US62LV4096 is available in the JEDEC standard 44 pin TSOP (Type II) and 48 pin mini-BGA.

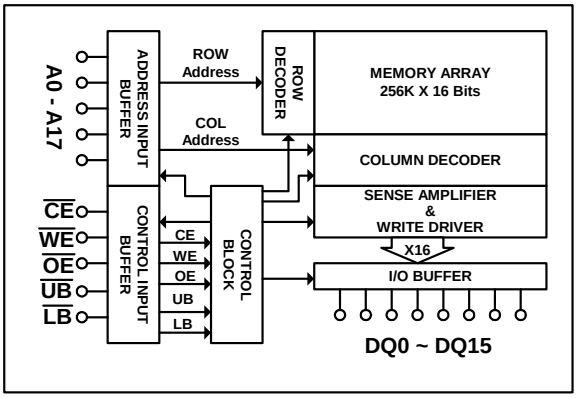
■ PRODUCT FAMILY

Product Family	Operating Tempature	Vcc Range	Speed (ns)	Power Consumption		Package Type
				STANDBY	Operating	
			Vcc=1.5V(Max.)	Vcc=3.3V(Typ.)	Vcc=3.6V(Max.)	
UC62LV4096JC	0℃ ~ 70℃	1.5V ~ 3.6V	55/70	2uA	35mA	TSOP-44
UC62LV4096KC						BGA-48
UC62LV4096AC						DICE
UC62LV4096JI	-40℃ ~ 85℃	1.5V ~ 3.6V	55/70	2uA	35mA	TSOP-44
UC62LV4096KI						BGA-48
UC62LV4096AI						DICE

■ PIN CONFIGURATIONS



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Name	Type	Function
A0 – A17	Input	Address inputs for selecting one of the 262,144 x 16 bit words in the RAM
CE\	Input	CE\ is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and not in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected.
WE\	Input	The Write enable input is active LOW and controls read and write operations. With the chip selected, when WE\ is HIGH and OE\ is LOW, output data will be present on the DQ pins, when WE\ is LOW, the data present on the DQ pins will be written into the selected memory location.
OE\	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when OE\ is inactive.
UB\ and LB\	Input	Lower byte and upper byte data input/output control pins.
DQ0 – DQ15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Gnd	Power	Ground

■ TRUTH TABLE

Mode	WE\	CE\	OE\	LB\	UB\	I/O 0 ~ 7	I/O 8 ~ 15	Vcc Current
Not Selected	X	H	X	X	X	High Z	High Z	I_{SB},I_{SB1}
Output Disabled	H	L	H	X	X	High Z	High Z	I_{CC}
	X	L	X	H	H			
Read	H	L	L	L	H	D_{OUT}	High Z	I_{CC}
	H	L	L	H	L	High Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High Z	I_{CC}
	L	L	X	H	L	High Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

■ ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to V_{CC}+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to 125	℃
T_{STG}	Storage Temperature	-50 to 150	℃
PT	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	10	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0℃ to 70℃	1.5V ~ 3.6V
Industrial	-40℃ to 85℃	1.5V ~ 3.6V

■ CAPACITANCE(1)(TA=25℃,f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output Capacitance	VDQ	8	pF

1. This parameter is guaranteed and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS (TA=0℃ to 70℃)

Symbol	Comment	Test Condition	MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)	V_{CC}=2.4V	-0.5	-	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)	V_{CC}=3.6V	2.0	-	Vcc-0.2	V
I_L	Input Leakage Current	V_{CC}=3.6V V_{IN}=0V to V_{CC}	-	-	1	uA
I_{OL}	Output Leakage Current	V_{CC}=3.6V CE\=V_{IH} or OE\=V_{IH} V_{IO}=0V t V_{CC}	-	-	1	uA
V_{OL}	Output Low Voltage	V_{CC}=3.6V, I_{OL}=2mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC}=3.0V, I_{OH}=-1mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	CE\=V_{IL},I_{DQ}=0mA, F=Fmax(3)	-	-	35	mA
I_{SB1}	TTL Standby Current	CE\=V_{IH}, V_{IN}=V_{IH} to V_{IL}	-	-	1	mA
I_{SB2}	CMOS Standby Current	CE\≧V_{CC}-0.2V, V_{IN}=V_{CC}-0.2V or 0.2V , F=0(4)	-	2	10	uA

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.

3. Fmax = 1/tRC .

4. F=0 means input signals must be keep in static state.

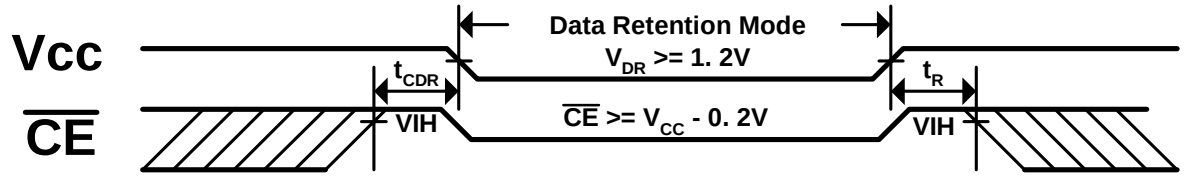
■ DATA RETENTION CHARACTERISTICS (TA=0℃ to 70℃)

Symbol	Comment	Test Condition	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	VCC to Data Retention	CE\≧V_{CC} - 0.2V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	1.2	-	-	V
I_{CCDR}	Data Retention Current	CE\≧V_{CC} - 0.2V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	-	0.1	1	uA
t_{DR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		T_{RC}(2)	-	-	ns

1. V_{CC} = 1.5V, TA = 25℃.

2. t_{RC} = Read Cycle Time

■ LOW VCC DATA RETENTION WAVEFORM(1) (CE\ Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	VCC to 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	$0.5V_{CC}$

■ AC TEST LOADS AND WAVEFORMS

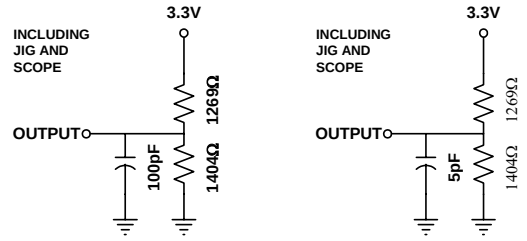
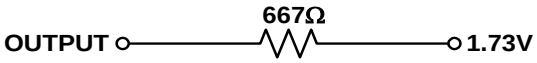


FIGURE 1A FIGURE 1B

TERMINAL EQUIVALENT



ALL INPUT PULSES

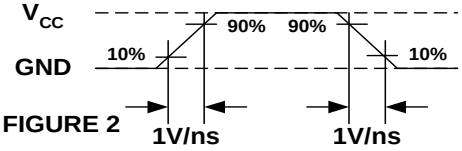


FIGURE 2

■ KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

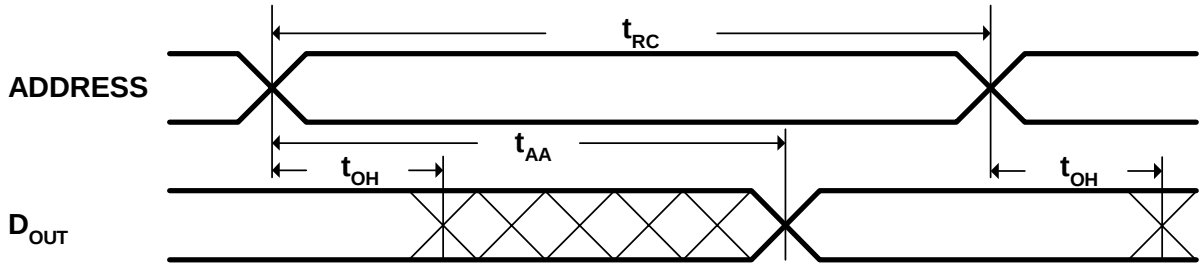
■ AC ELECTRICAL CHARACTERISTICS (TA=0℃ to 70℃, V_{CC}=1.5 V~3.6V)

READ CYCLE

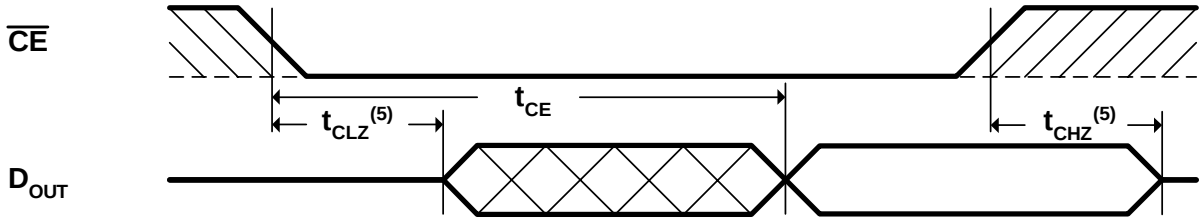
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	UC62LV4096-55			UC62LV4096-70			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{AVAX}	t_{RC}	Read Cycle Time	55	-	-	70	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	-	55	-	-	70	ns
t_{ELQV}	t_{CE}	Chip Select Access Time	-	-	55	-	-	70	ns
t_{BA}	t_{BA}	Data Byte Control Access Time			30			35	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	-	30	-	-	35	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z	10	-	-	10	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	5	-	-	5	-	-	ns
t_{BE}	t_{BE}	Data Byte Control To Output Low Z	10			10			ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	-	-	20	-	-	20	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	-	20	-	-	20	ns
t_{BDO}	t_{BDO}	Data Byte Control To Output High Z	-		20	-		20	ns
t_{AXOX}	t_{OH}	Address Chang to Output Change	10	-	-	10	-	-	ns

■ SWITCHING WAVEFORMS (READ CYCLE)

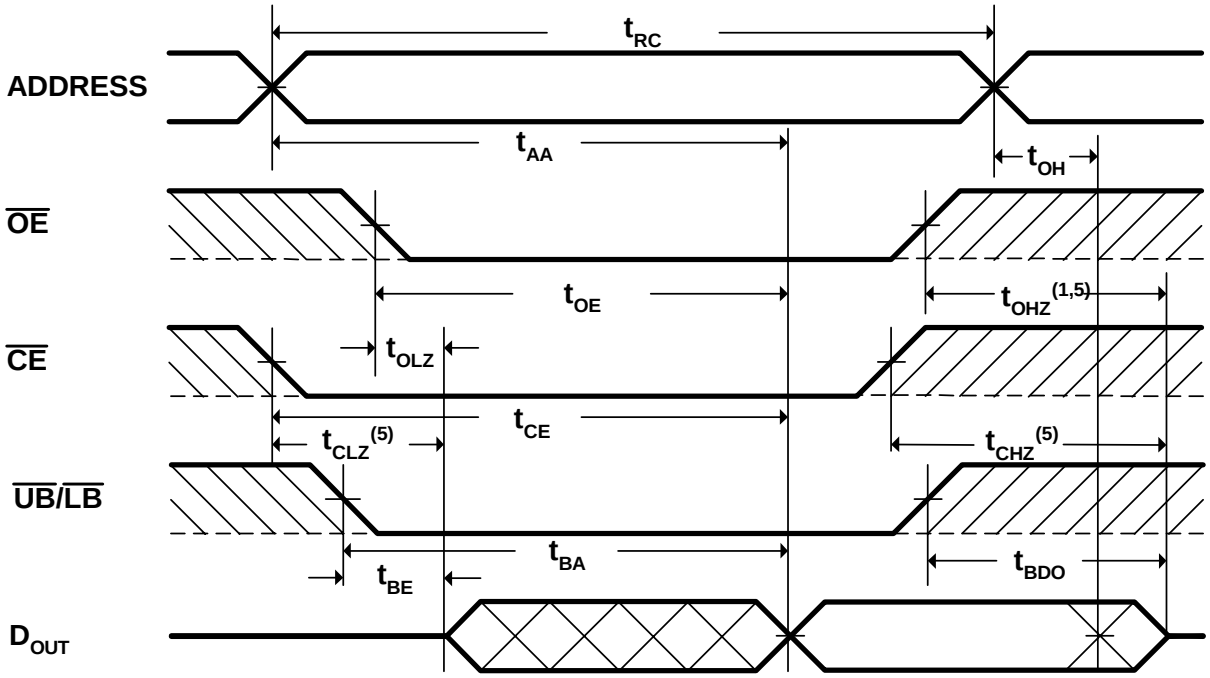
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:

1. WE\ is high in read cycle.
2. Device is continuously selected when CE\ = VIL
3. Address valid prior to or coincident with CE\ transition low.
4. OE\ = VIL.
5. Transition is measured ±500mV from steady state with CL=5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
6.

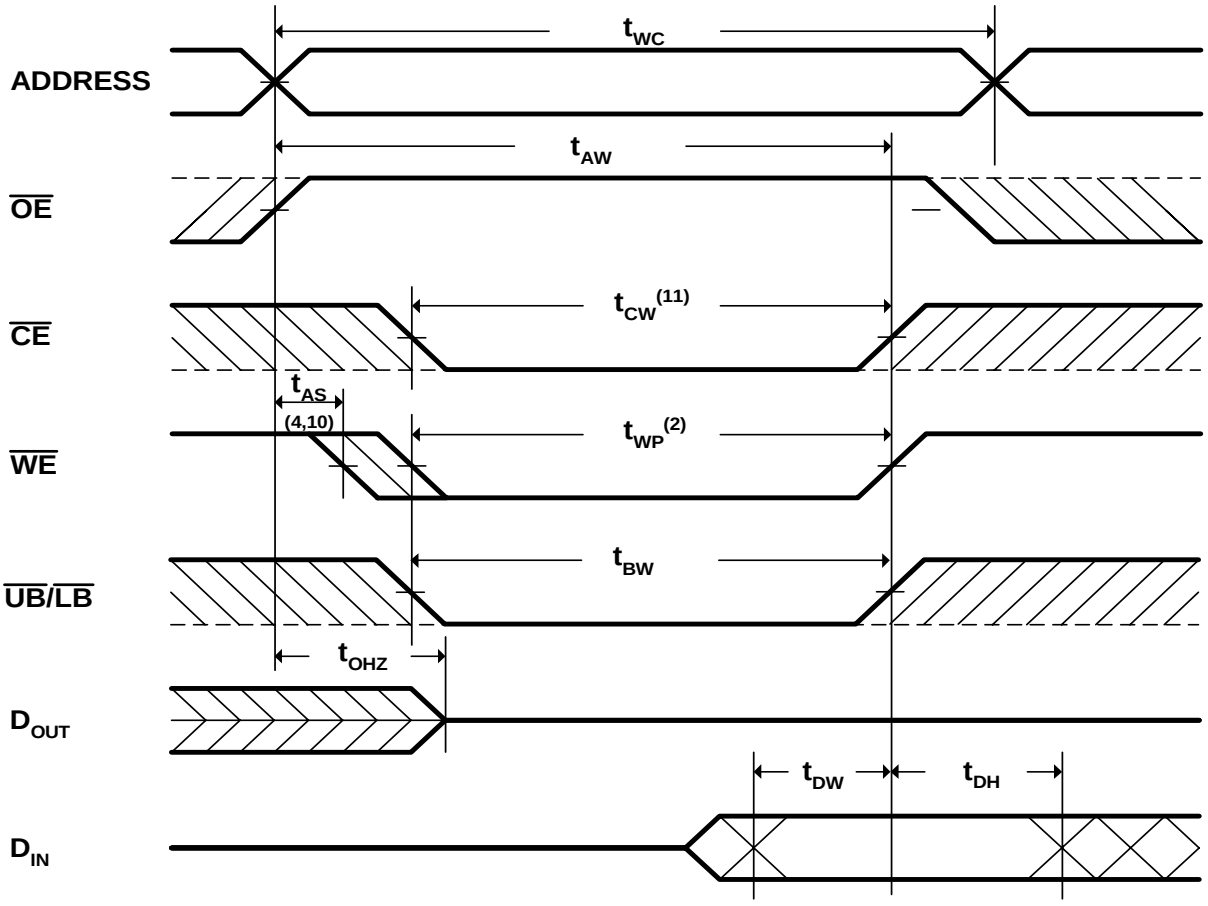
■ AC ELECTRICAL CHARACTERISTICS (TA=0℃ to 70℃, VCC=1.5V~3.6V)

WRITE CYCLE

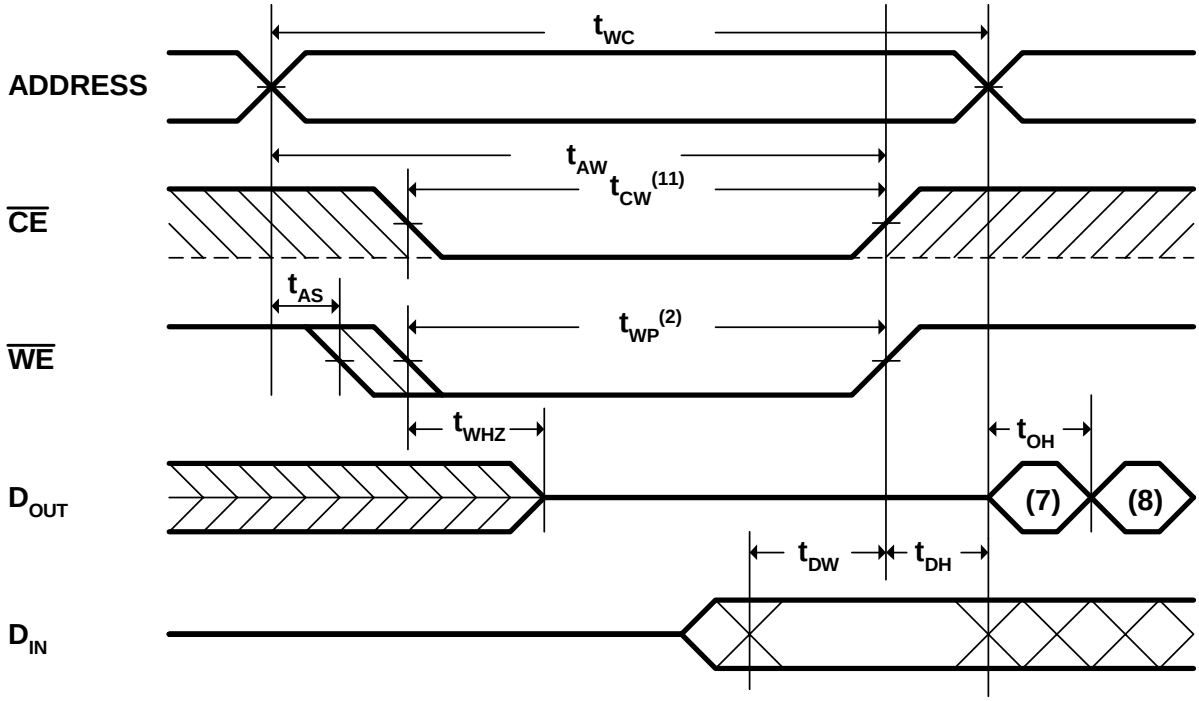
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	UC62LV4096-55			UC62LV4096-70			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{AVAX}	t_{WC}	Write Cycle Time	55	-	-	70	-	-	ns
t_{E1LWH}	t_{CW}	Chip Select to END of Write	40	-	-	50	-	-	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address valid to End of Write	40	-	-	50	-	-	ns
t_{BW}	t_{BW}	Data Byte Control End of Write	40			50			Ns
t_{WLWH}	t_{WP}	Write Pulse Width	40	-	-	50	-	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	-	0	-	-	ns
t_{WLOZ}	t_{WHZ}	Write to Output in High Z	-	-	20	-	-	20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	35	-		40	-		ns
t_{WHDX}	t_{DH}	Data Hold Time for Write End	0	-	-	0	-	-	ns
t_{GHOZ}	t_{OHZ}	Output Disable to Output In High Z	-	-	20	-	-	20	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	10	-	-	10	-	-	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITECYCLE1(1)



WRITE CYCLE2(1,6)



NOTES:

1. WE\ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE\ and WE\ low. All signals must be active to initiate a write and any one can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of CE\ or WE\ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE\ low transition occurs simultaneously with the WE\ low transitions or after the WE\ transition, output remain in a high impedance state.
6. OE\ is continuously low (OE\ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CE\ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured 500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. TCW is measured from the later of CE\ going low to the end of write.

■ ORDERING INFORMATION

UC62LV4096 AB -- YY

A => GRADE

- **J :TSOP**
- **K :BGA**
- **A :DICE**

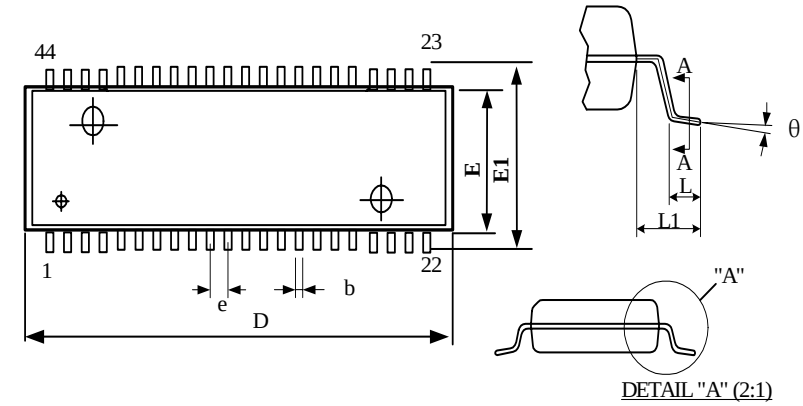
B => GRADE

- **C :COMMERCIAL (0 ~ 70℃)**
- **I :INDUSTRIAL (-40 ~ 85℃)**

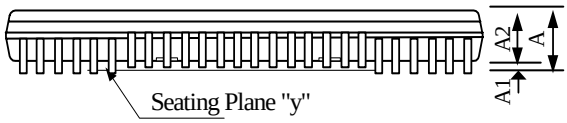
YY => SPEED

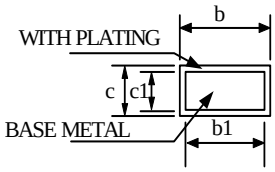
- **55: 55ns**
- **70: 70ns**

PACKAGE DIMENSIONS

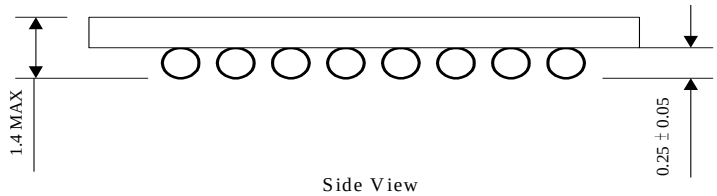


UNIT / SYMBOL	INCH	MM
A	0.0433±0.004	1.10±0.1
A1	0.004±0.002	0.1±0.05
A2	0.039±0.002	1.00±0.05
b	0.012 ~ 0.018	0.3 ~ 0.45
b1	0.012 ~ 0.016	0.3 ~ 0.4
c	0.005 ~ 0.008	0.12 ~ 0.21
c1	0.005 ~ 0.006	0.12 ~ 0.16
D	0.725±0.004	18.41±0.1
E	0.400±0.004	10.16±0.1
E1	0.463±0.008	11.76±0.20
e	0.0315±0.004	0.80±0.10
L	0.0197±0.004	0.50±0.1
L1	0.0197±0.004	0.80±0.1
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

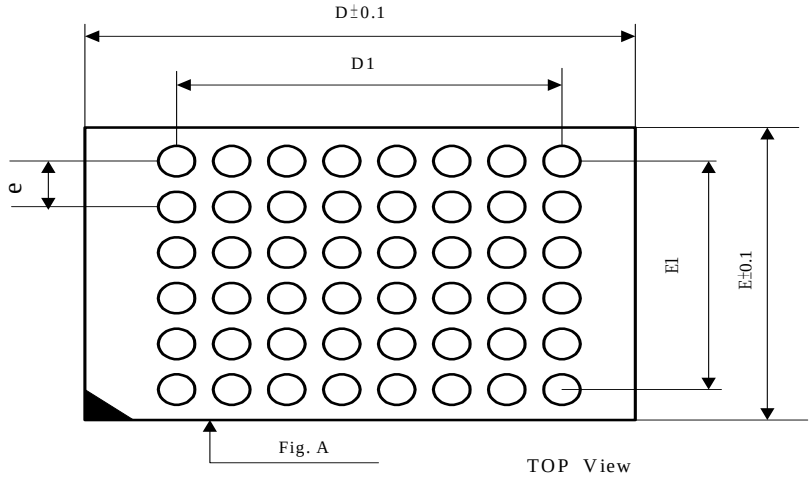




TSOPII - 44



Ball pitch e=0.75			
D	E	D1	E1
8.0	6.0	5.25	3.75



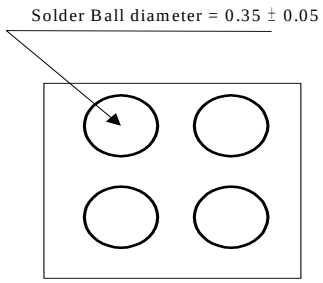


Fig. A

48 Mini-BGA 6*8mm