



UCA9306

CMOS IC

DUAL BIDIRECTIONAL I²C BUS AND SMBUS VOLTAGE-LEVEL TRANSLATOR

DESCRIPTION

The UTC **UCA9306** device is a dual bidirectional I²C and SMBus voltage-level translator with an enable(EN) input, and is operational from 1.2-V to 3.3-V V_{REF1} and 1.8-V to 5.5-V V_{REF2}.

The UTC **UCA9306** device allows bidirectional voltage translations between 1.2V and 5V, without the use of a direction pin. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In addition to voltage translation, the UTC **UCA9306** device can be used to isolate a 400-kHz bus from a 100-kHz bus by controlling the EN pin, and disconnecting the slower bus during fast-mode communication.

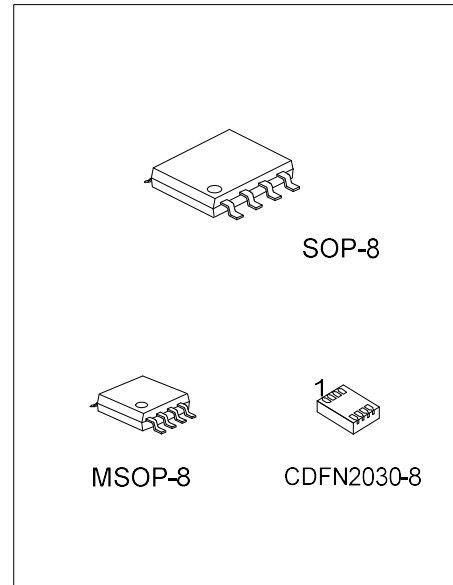
FEATURES

- * 2-Bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I²C Applications
- * I²C and SMBus Compatible
- * Less Than 1.5-ns Maximum Propagation Delay to Accommodate Standard-Mode and Fast-Mode I²C Devices and Multiple Masters
- * Allows Voltage-Level Translation Between
 - 1.2V V_{REF1} and 1.8-V, 2.5-V, 3.3-V, or 5-V V_{REF2}
 - 1.8V V_{REF1} and 2.5-V, 3.3-V, or 5-V V_{REF2}
 - 2.5V V_{REF1} and 3.3-V or 5-V V_{REF2}
 - 3.3V V_{REF1} and 5-V V_{REF2}
- * Provides Bidirectional Voltage Translation With No Direction Pin
- * Low 3.5-Ω ON-State Resistance Between Input And Output Ports Provides Less Signal Distortion
- * Open-Drain I²C I/O Ports (SCL1, SDA1, SCL2, and SDA2)
- * 5-V Tolerant I²C I/O Ports to Support Mixed-Mode Signal Operation
- * High-Impedance SCL1, SDA1, SCL2, and SDA2 Pins for EN=Low
- * Lockup-Free Operation for Isolation When EN=Low
- * Flow-Through Pinout for Ease of Printed-Circuit-Board Trace Routing

ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|----------------------|----------------------|------------|-----------|
| Lead Free | Halogen Free | | |
| UCA9306L-S08-R | UCA9306G-S08-R | SOP-8 | Tape Reel |
| UCA9306L-SM1-R | UCA9306G-SM1-R | MSOP-8 | Tape Reel |
| UCA9306L-CK08-2030-R | UCA9306G-CK08-2030-R | CDFN2030-8 | Tape Reel |

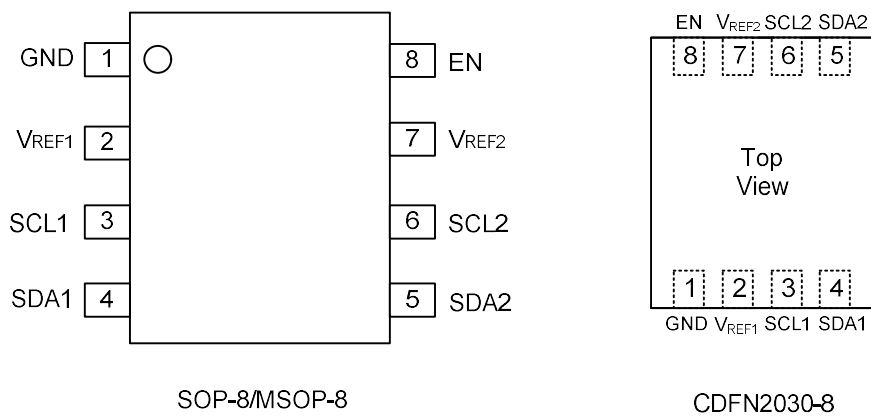
| | |
|--|---|
| <p>UCA9306G-S08-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p> | <p>(1) R: Tape Reel (2) S08: SOP-8, SM1: MSOP-8 CK08-2030: CDFN2030-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p> |
|--|---|



MARKING

| SOP-8 / MSOP-8 | CDFN2030-8 |
|--|---|
| <p>UTC □ □ □ □ → Date Code UCA9306 □ □ □ □ → L: Lead Free □ □ □ □ → G: Halogen Free □ □ □ □ → Lot Code</p> | <p>UCA 9306 • □ □ □ □ → Date Code</p> |

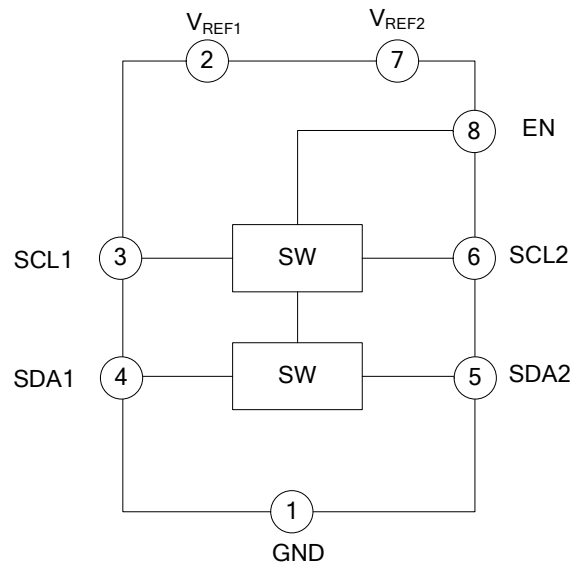
PIN CONFIGURATION



PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---------|----------|--|
| 1 | GND | Ground,0V |
| 3 | SCL1 | Serial clock , low-voltage side |
| 6 | SCL2 | Serial clock , high-voltage side |
| 4 | SDA1 | Serial data , low-voltage side |
| 5 | SDA2 | Serial data , high-voltage side |
| 2 | VREF1 | Low-voltage-side reference supply voltage for SCL1 and SDA1 |
| 7 | VREF2 | High-voltage-side reference supply voltage for SCL2 and SDA2 |
| 8 | EN | Switch enable input |

■ BLOCK DIAGRAM



■ FUNCTION TABLE

| INPUT EN | TRANSLATOR FUNCTION |
|----------|----------------------|
| H | SCL1=SCL2, SDA1=SDA2 |
| L | Disconnect |

■ ABSOLUTE MAXIMUM RATING (Note 2)

Over operating ambient temperature range (unless otherwise noted)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-------------------------------------|------------|------------|------|
| DC reference voltage range | V_{REF1} | -0.5 ~ 7.0 | V |
| DC reference bias voltage range | V_{REF2} | -0.5 ~ 7.0 | V |
| Input voltage range (Note 3) | V_I | -0.5 ~ 7.0 | V |
| Input/output voltage range (Note 3) | $V_{I/O}$ | -0.5 ~ 7.0 | V |
| Continuous channel current | | 128 | mA |
| Input clamp current ($V_I < 0$) | I_{IK} | -50 | mA |
| Maximum junction temperature | T_J | +125 | °C |
| Storage temperature range | T_{STG} | -65 ~ +150 | °C |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3. The input and input/output negative voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING RATINGS

| PARAMETER | SYMBOL | RATING | UNIT |
|-------------------------------|------------|------------|------|
| Input/output voltage | $V_{I/O}$ | 0 ~ 5.5 | V |
| Reference voltage (Note) | V_{REF1} | 0 ~ 5.5 | V |
| Reference voltage (Note) | V_{REF2} | 0 ~ 5.5 | V |
| Enable input voltage | EN | 0 ~ 5.5 | V |
| Pass switch current | I_{PASS} | 64 | mA |
| Operating ambient temperature | T_A | -40 ~ +125 | °C |

Note: To support translation, V_{REF1} supports 1.2V to V_{REF2} -0.6V. V_{REF2} must be between $V_{REF1}+0.6V$ to 5.5V. See Typical Application for more information.

■ ELECTRICAL CHARACTERISTICS

Over recommended operating ambient temperature range (unless otherwise specified)

| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP (Note 1) | MAX | UNIT | | |
|---------------------------------------|------------|----------------------|------------------------|---------------------------------------|-----------------|------|------|----|---|
| Input clamp voltage | | V_{IK} | $I_I = -18mA, EN=0V$ | | | -1.2 | V | | |
| Input leakage current | | I_{IH} | $V_I = 5V, EN=0V$ | | | 5 | µA | | |
| Input capacitance | | $C_{J(EN)}$ | $V_I = 3V$ or 0 | | 11 | | pF | | |
| Off Capacitance | SCLn, SDAn | $C_{JO(OFF)}$ | $V_O = 3V$ or 0, EN=0V | | 4 | 6 | pF | | |
| On Capacitance | SCLn, SDAn | $C_{JO(ON)}$ | $V_O = 3V$ or 0, EN=3V | | 10.5 | 12.5 | pF | | |
| On-state Resistance | SCLn, SDAn | R_{ON} (Note 2) | $V_I = 0, I_O = 64mA$ | EN=4.5V | 3.5 | 5.5 | Ω | | |
| | | | | EN=3V | 4.7 | 7.0 | Ω | | |
| | | | | EN=2.3V | 6.3 | 9.5 | Ω | | |
| | | | $V_I = 0, I_O = 15mA$ | EN=1.5V | 25.5 | 32 | Ω | | |
| | | | | $V_I = 2.4V$ (Note 3) $I_O = 15mA$ | EN=4.5V | 1 | 6 | 15 | Ω |
| | | | | EN=3V | 20 | 60 | 140 | Ω | |
| $V_I = 1.7V$ (Note 3) $I_O = 15mA$ | EN=2.3V | 20 | 60 | 140 | Ω | | | | |

Notes: 1. All typical values are at $T_A = 25^\circ C$.

2. Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch.

3. Measured in current sink configuration only.

■ AC PERFORMANCE (TRANSLATING DOWN)

Switching Characteristics

(Over recommended operating free-air temperature range, EN=3.3V, V_{IH} =3.3V, V_{IL} =0, and V_M =1.15V unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|-----------|-----------------------|-----|-----|-----|------|
| From SCL2 or SDA2 to SCL1 or SDA1 | t_{PLH} | $C_L = 15 \text{ pF}$ | 0 | | 0.3 | ns |
| | | $C_L = 30 \text{ pF}$ | 0 | | 0.6 | ns |
| | | $C_L = 50 \text{ pF}$ | 0 | | 0.8 | ns |
| | t_{PHL} | $C_L = 15 \text{ pF}$ | 0 | | 0.5 | ns |
| | | $C_L = 30 \text{ pF}$ | 0 | | 1.0 | ns |
| | | $C_L = 50 \text{ pF}$ | 0 | | 1.2 | ns |

Switching Characteristics

(Over recommended operating free-air temperature range, EN=2.5V, V_{IH} =2.5V, V_{IL} =0, and V_M =0.75V unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|-----------|-----------------------|-----|-----|-----|------|
| From SCL2 or SDA2 to SCL1 or SDA1 | t_{PLH} | $C_L = 15 \text{ pF}$ | 0 | | 0.4 | ns |
| | | $C_L = 30 \text{ pF}$ | 0 | | 0.7 | ns |
| | | $C_L = 50 \text{ pF}$ | 0 | | 1.0 | ns |
| | t_{PHL} | $C_L = 15 \text{ pF}$ | 0 | | 0.6 | ns |
| | | $C_L = 30 \text{ pF}$ | 0 | | 1.0 | ns |
| | | $C_L = 50 \text{ pF}$ | 0 | | 1.3 | ns |

■ AC PERFORMANCE (TRANSLATING UP)

Switching Characteristics

(Over recommended operating free-air temperature range, EN=3.3V, V_{IH} =2.3V, V_{IL} =0, V_T =3.3V, V_M =1.15V and R =300 Ω unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|-----------|-----------------------|-----|-----|-----|------|
| From SCL1 or SDA1 to SCL2 or SDA2 | t_{PLH} | $C_L = 15 \text{ pF}$ | 0 | | 0.4 | ns |
| | | $C_L = 30 \text{ pF}$ | 0 | | 0.6 | ns |
| | | $C_L = 50 \text{ pF}$ | 0 | | 0.9 | ns |
| | t_{PHL} | $C_L = 15 \text{ pF}$ | 0 | | 0.7 | ns |
| | | $C_L = 30 \text{ pF}$ | 0 | | 1.1 | ns |
| | | $C_L = 50 \text{ pF}$ | 0 | | 1.4 | ns |

Switching Characteristics

(Over recommended operating free-air temperature range, EN=2.5V, V_{IH} =2.3V, V_{IL} =0, V_T =3.3V, V_M =0.75V and R =300 Ω unless otherwise noted)

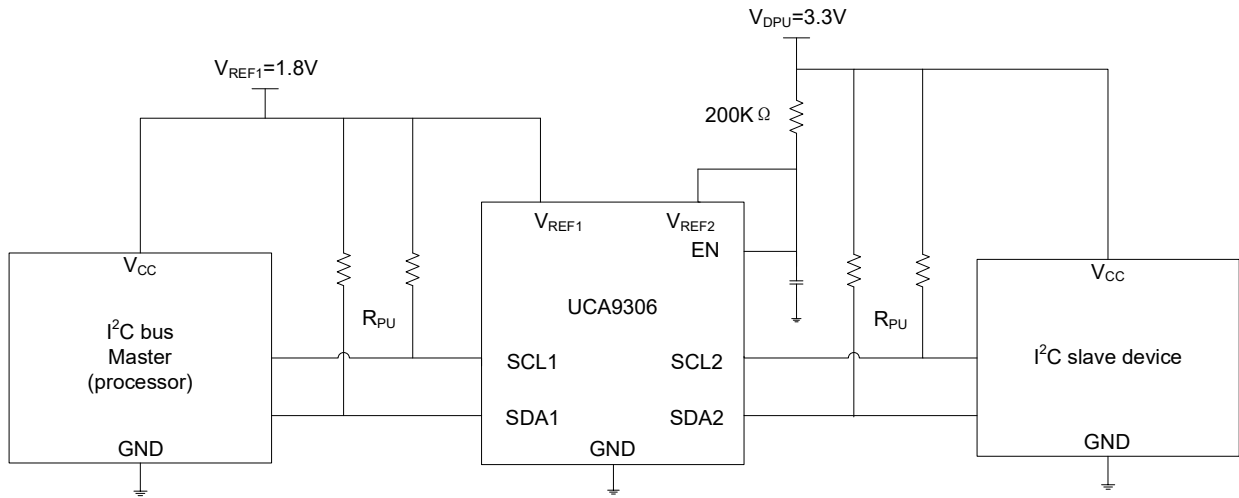
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------|-----------|-----------------------|-----|-----|-----|------|
| From SCL1 or SDA1 to SCL2 or SDA2 | t_{PLH} | $C_L = 15 \text{ pF}$ | 0 | | 0.4 | ns |
| | | $C_L = 30 \text{ pF}$ | 0 | | 0.6 | ns |
| | | $C_L = 50 \text{ pF}$ | 0 | | 1.0 | ns |
| | t_{PHL} | $C_L = 15 \text{ pF}$ | 0 | | 0.8 | ns |
| | | $C_L = 30 \text{ pF}$ | 0 | | 1.3 | ns |
| | | $C_L = 50 \text{ pF}$ | 0 | | 1.3 | ns |

■ APPLICATION INFORMATION

General Applications of I²C

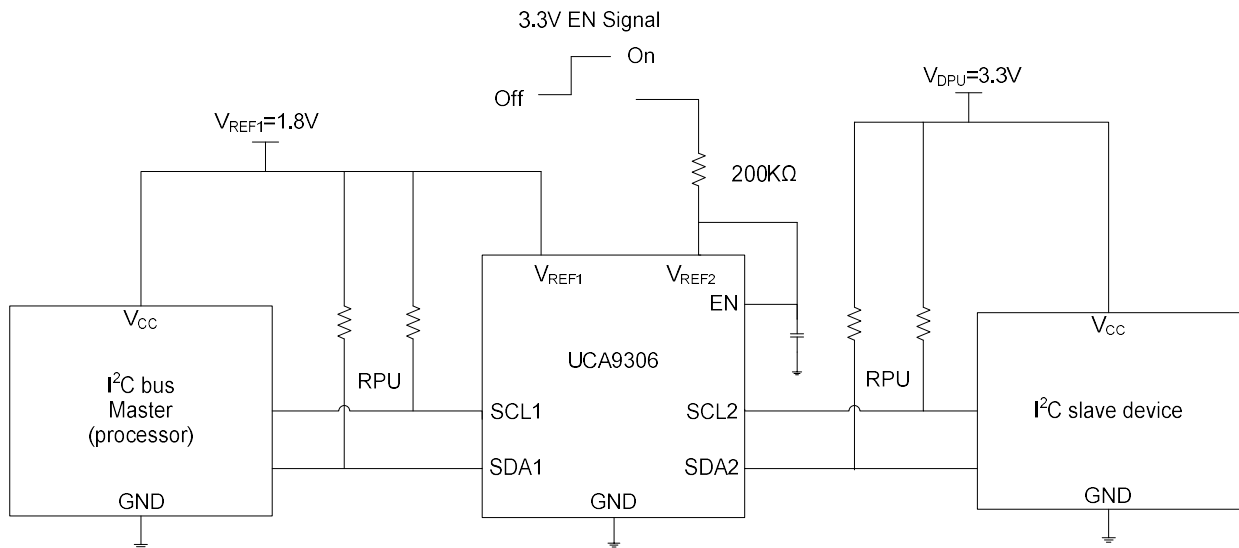
As with the standard I²C system, pull up resistors are required to provide the logic-high levels on the translator bus. The size of these pull up resistors depends on the system, but each side of the repeater must have a pull up resistor. The device is designed to work with standard-mode and fast-mode I²C devices, in addition to SMBus devices. Standard-mode I²C devices only specify 3 mA in a generic I²C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1} . When the SDA1 port is high, the SDA2 port is pulled to the pull up supply voltage of the drain (V_{DPU}) by the pull up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

■ TYPICAL APPLICATION CIRCUIT



Typical Application Circuit (Switch Always Enabled)

The applied voltages at V_{REF1} and V_{DPU} should be such that V_{REF2} is at least 1 V higher than V_{REF1} for best translator operation.



Typical Application Circuit (Switch Enable Control)

In the enabled mode, the applied enable voltage and the applied voltage at V_{REF1} should be such that V_{REF2} is at least 1 V higher than V_{REF1} for best translator operation.

■ DETAILED DESIGN PROCEDURE

Bidirectional Voltage Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200k Ω). This allows V_{REF2} to regulate the EN input. A100-Pf filter capacitor connected to V_{REF2} is recommended. The I²C bus master output can be push-pull or open-drain (pull up resistors may be required) and the I²C bus device output can be totem pole or open-drain (pull up resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage (V_{REF1}) is connected to the core power-supply voltage of the processor.

Design Requirements

| PARAMETER | SYMBOL | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------------------|------------|----------------|--------------------|-----|---------|
| Reference voltage | V_{REF2} | $V_{REF1}+0.6$ | 2.1 | 5 | V |
| Enable input voltage | EN | $V_{REF1}+0.6$ | 2.1 | 5 | V |
| Reference voltage | V_{REF1} | 1.2 | 1.5 | 4.4 | V |
| Pass switch current | I_{PASS} | | 6 | | mA |
| Reference-transistor current | I_{REF} | | 5 | | μ A |

Note: All typical values are at $T_A=25^\circ\text{C}$.

Sizing Pull up Resistor

The pull up resistor value needs to limit the current through the pass transistor, when it is in the on state, to about 15mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15mA, the pullup resistor value is calculated as:

$$R_{PU} = \frac{V_{DPU} - 0.35V}{0.015A}$$

The following table summarizes resistor values, reference voltages, and currents at 15mA, 10 mA, and 3mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350mV or less. The external driver must be able to sink the total current from the resistors on both sides of the UTC **UCA9306** device at 0.175V, although the 15 mA applies only to current flowing through the UTC **UCA9306** device.

Pullup Resistor Values

| V_{DPU} | PULLUP RESISTOR VALUE (Ω) | | | | | |
|-----------|------------------------------------|------|---------|------|---------|------|
| | 15mA | | 10mA | | 3mA | |
| | NOMINAL | +10% | NOMINAL | +10% | NOMINAL | +10% |
| 5V | 310 | 341 | 465 | 512 | 1550 | 1705 |
| 3.3V | 197 | 217 | 295 | 325 | 983 | 1082 |
| 2.5V | 143 | 158 | 215 | 237 | 717 | 788 |
| 1.8V | 97 | 106 | 145 | 160 | 483 | 532 |
| 1.5V | 77 | 85 | 115 | 127 | 383 | 422 |
| 1.2V | 57 | 83 | 85 | 94 | 283 | 312 |

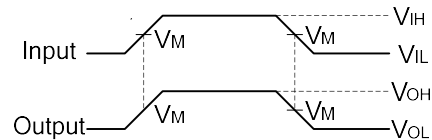
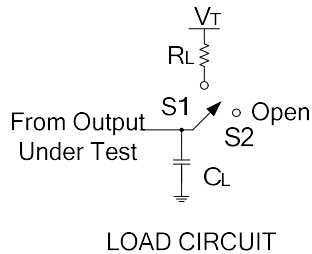
(1) Calculated for $V_{OL}=0.35V$

(2) Assumes output driver $V_{OL}=0.175V$ at stated current

(3) +10% to compensate for V_{DD} range and resistor tolerance

■ PARAMETER MEASUREMENT INFORMATION

| USAGE | SWITCH |
|------------------|--------|
| Translating up | S1 |
| Translating down | S2 |



- Notes:
1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_0 = 50\Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 3. The outputs are measured one at a time, with one transition per measurement.

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