UCB1400

Audio codec with touch screen controller and power management monitor

Rev. 02 — 21 June 2002 **Product data**

1. General description

The UCB1400 is a stereo audio codec equipped with touch screen and power management interfaces. It integrates an AC '97 Rev. 2.1 interface for communication to an AC link host controller such as the Intel Xscale™ processor. The stereo audio codec inputs connect directly to a microphone or line level sources such as a CD player. The stereo audio codec outputs at line level and can drive a headphone directly. The touch screen interface connects directly to a 4-wire resistive touch screen. A built-in 10-bit analog-to-digital converter provides readout of touch screen and power management parameters. Ten general-purpose I/O pins provide programmable inputs and/or outputs to the system.

2. Features

- 48-pin LQFP surface mount package and low external component count for minimal PCB space requirement
- Integrated AC '97 Rev. 2.1 interface
- 20-bit stereo audio codec supporting programmable sample rates, and input/output gain control
  - Stereo line input and mono microphone input
  - Stereo line/headphone output with bass/treble control
  - Headphone driver with short circuit protection and virtual ground for DC coupling
- 4-wire resistive touch screen interface circuit supporting position, pressure and plate resistance measurements
- 10-bit successive approximation ADC with internal track-and-hold circuit and analog multiplexer for touch screen readout and monitoring of four external high voltage (7.5 V) sources
- Ten general purpose input/output pins
- 3.3 V supply voltage and built-in power saving modes for portable and battery powered applications.

3. Applications

- Smart mobile phones
- Handheld PCs
- Palm-top PCs
- Personal Intelligent Communicators (PIC)
- Personal Digital Assistants (PDA).

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
UCB1400BE	LQFP48	Plastic low profile quad flat package, 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5. Block diagram

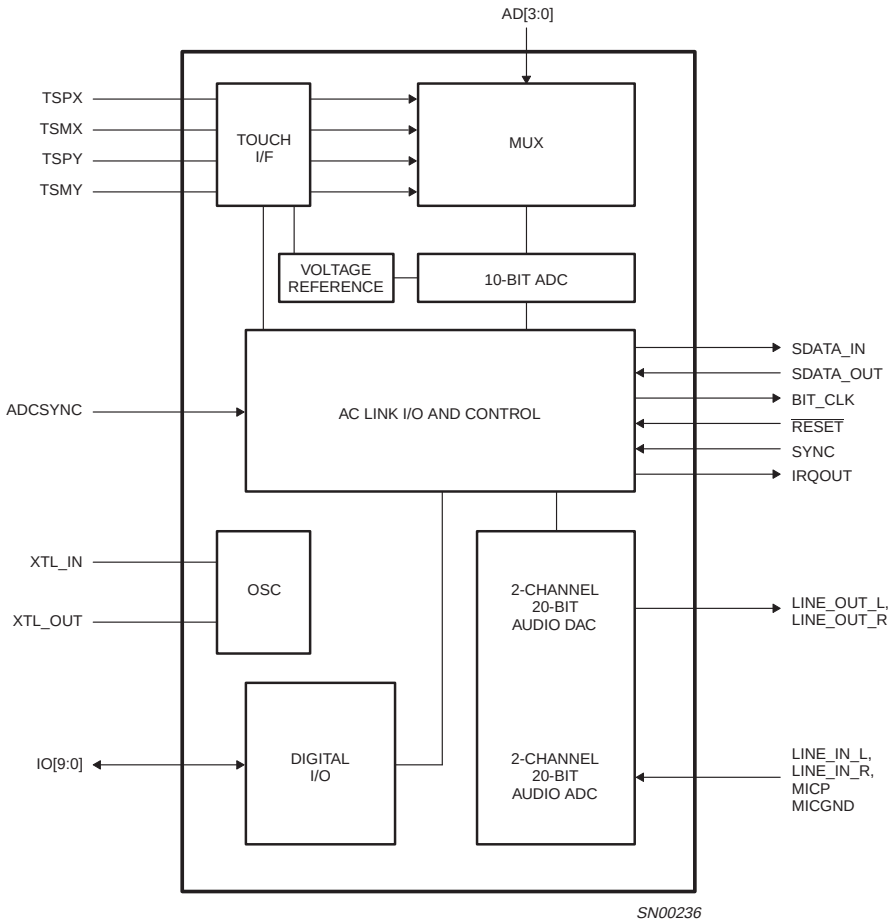


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

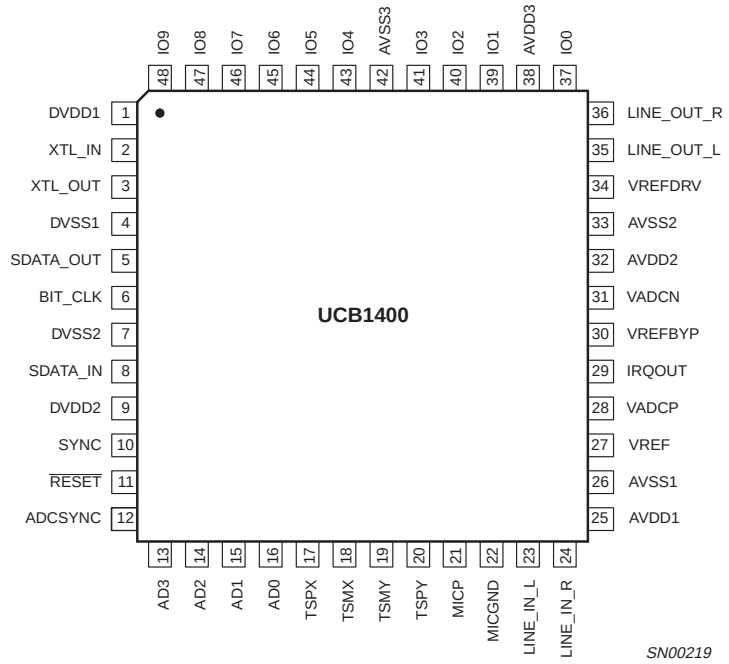


Fig 2. Pin configuration (LQFP48).

6.2 Pin description

Table 2: Pin description

Total pin count = 48

Symbol	Pin	Type	Default state	Description
AC-link, crystal and interrupt interface (pin count = 8)				
XTL_IN	2	I	–	24.576 MHz crystal / master clock input
XTL_OUT	3	O	–	24.576 MHz crystal
$\overline{\text{RESET}}$	11	I	–	AC-link master reset
SYNC	10	I	–	AC-link sample sync
BIT_CLK	6	O	0	AC-link 12.288 MHz serial data clock
SDATA_OUT	5	I	–	AC-link serial data output. UCB1400 input stream
SDATA_IN	8	O	0	AC-link serial data input. UCB1400 output stream
IRQOUT	29	O	0	Interrupt output

Table 2: Pin description...*continued*

Total pin count = 48

Symbol	Pin	Type	Default state	Description
Audio interface (pin count = 6)				
MICP	21	I	–	Microphone input
MICGND	22	I	closed	Microphone ground switch input
LINE_IN_L	23	I	–	Line in left channel
LINE_IN_R	24	I	–	Line in right channel
LINE_OUT_L	35	O	driver off	Line out left channel
LINE_OUT_R	36	O	driver off	Line out right channel
ADC and touch screen interface (pin count = 9)				
AD[3:0]	13, 14, 15, 16	I	–	Analog voltage input
TSPX	17	I/O	Hi-Z	Touch screen positive X-plate
TSMX	18	I/O	Hi-Z	Touch screen negative X-plate
TSMY	19	I/O	Hi-Z	Touch screen negative Y-plate
TSPY	20	I/O	Hi-Z	Touch screen positive Y-plate
ADCSYNC	12	I	–	ADC synchronization pulse
GPIO interface (pin count = 10)				
IO[9:0]	48, 47, 46, 45, 44, 43, 41, 40, 39, 37	I/O	Input	General purpose input/output
Power and miscellaneous (pin count = 15)				
DVDD2, DVDD1	9, 1	S	–	Digital supply
DVSS2, DVSS1	7, 4	S	–	Digital ground
AVDD3, AVDD2, AVDD1	38, 32, 25	S	–	Analog supply
AVSS3, AVSS2, AVSS1	42, 33, 26	S	–	Analog ground
VREFDRV	34	O	–	Reference voltage for headphone drivers
VREF	27	O	–	Reference voltage
VADCP	28	S	–	Audio ADC positive reference voltage
VADCN	31	S	–	Audio ADC negative reference voltage
VREFBYP	30	I/O	Hi-Z	Reference bypass output/ external reference voltage input

7. Functional description

7.1 Functional block diagram

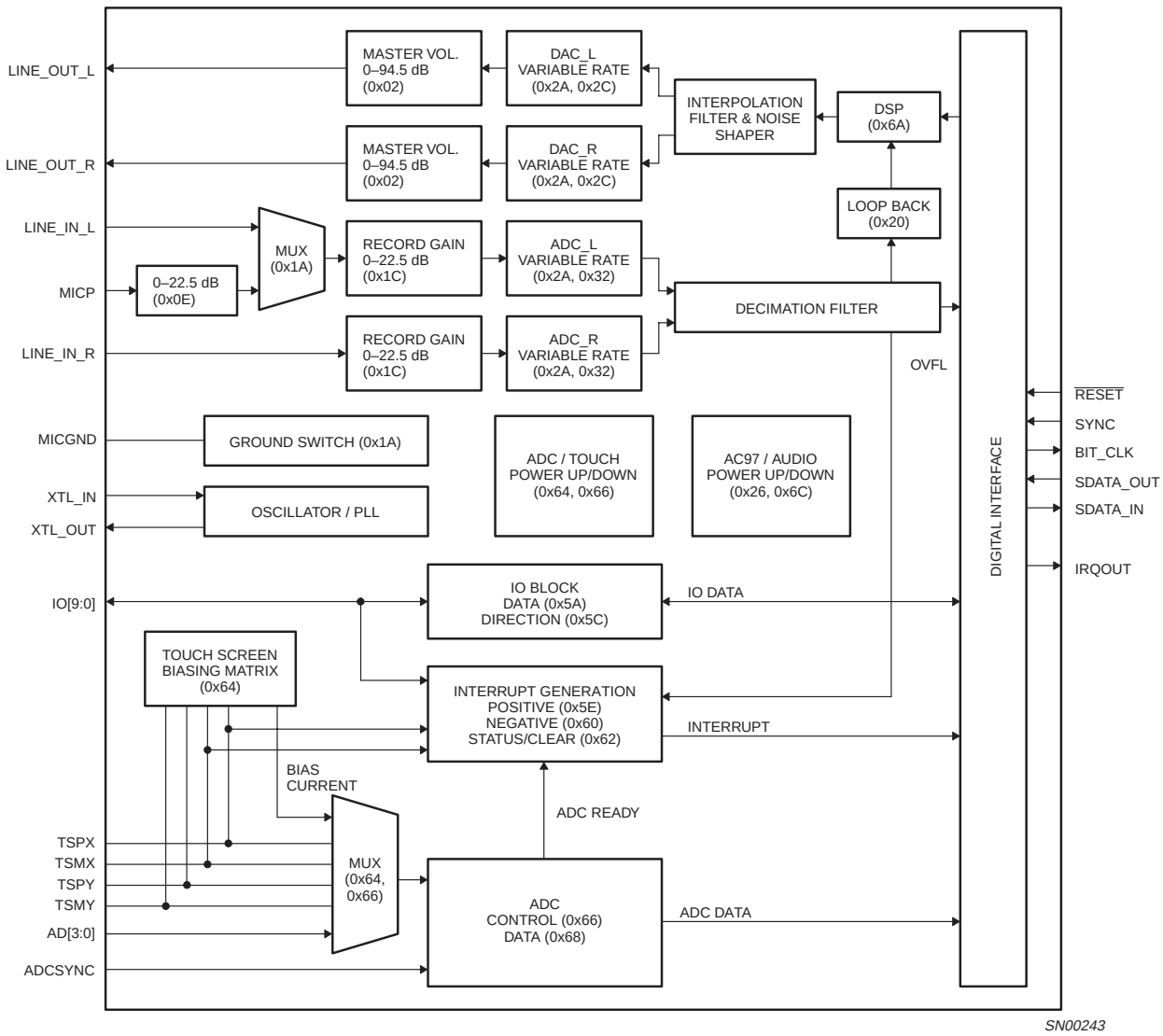


Fig 3. Functional block diagram.

8. AC ’97 interface

The UCB1400 implements an AC ’97 Revision 2.1 interface. Refer to the *Audio Codec ’97 Component Specification Revision 2.1* from Intel.

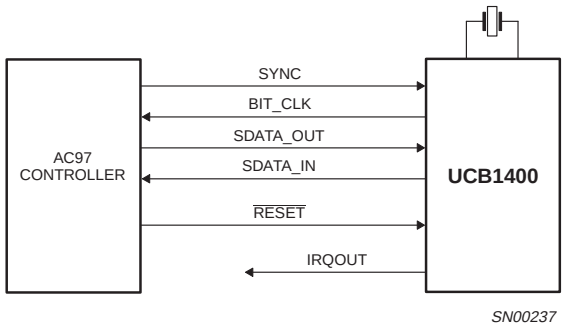


Fig 4. UCB1400 and AC ’97 controller connection diagram.

8.1 Clocking

The UCB1400 functions only as a primary codec. As such, it derives its clock internally from an externally attached 24.576 MHz crystal or clock oscillator, and drives a buffered and divided down (½) clock to its digital companion controller over AC-link under the signal name “BIT_CLK”.

The beginning of all audio sample packets, or Audio Frames, transferred over AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the AC ’97 Controller. The AC ’97 Controller takes BIT_CLK as an input and generates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48 kHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

8.2 Resetting UCB1400

The UCB1400 recognizes the following types of reset:

- Cold reset: where all UCB1400 logic (registers included) is initialized to its default state. Initiated by bringing $\overline{\text{RESET}}$ LOW for at least 1 μs.
- Warm reset: where the contents of the UCB1400 register set are left unaltered. Initiated by bringing SYNC HIGH for at least 1 μs without BIT_CLK.
- Register reset: which only initializes the UCB1400 registers to their default states. Initiated by a write to register 0x00.

After signaling a reset to UCB1400, the AC ’97 Controller should not attempt to play or capture audio data until it has sampled a “Codec Ready” indication from UCB1400.

8.3 Digital interface

8.3.1 AC-link digital serial interface protocol

The UCB1400 incorporates a 5-pin digital serial interface that links it to the AC '97 Controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input, and output audio and modem streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. The control and data slots defined by UCB1400 include:

- SDATA_OUT TAG (output slot 0)
- SDATA_IN TAG (input slot 0)
- Control (CMD ADDR & DATA) write port (output slots 1, 2)
- Status (STATUS ADDR & DATA) read port (input slots 1, 2)
- PCM L & R DAC playback (output slots 3, 4)
- PCM L & R ADC record (input slots 3, 4)
- GPIO interrupt status (input slot 12)

The AC-link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data.

SYNC remains HIGH for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is HIGH is defined as the Tag Phase. The remainder of the audio frame where SYNC is LOW is defined as the "Data Phase". Additionally, for power savings, all clock, sync, and data signals can be halted. UCB1400 is implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

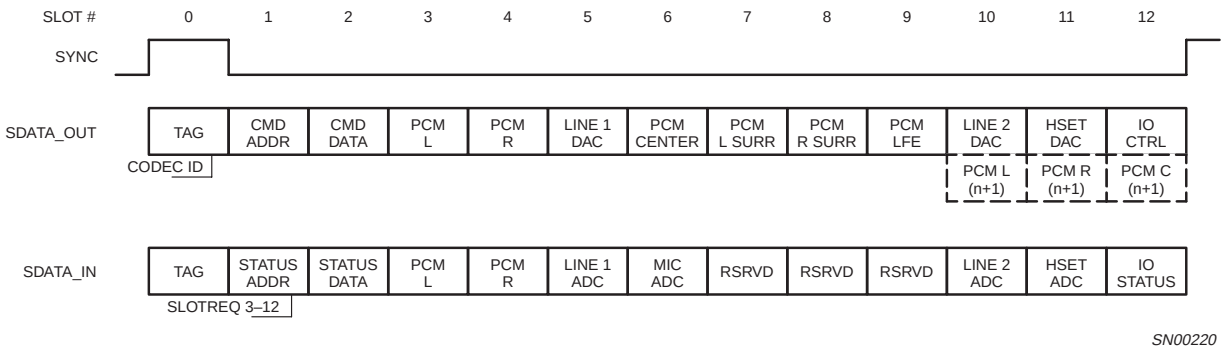


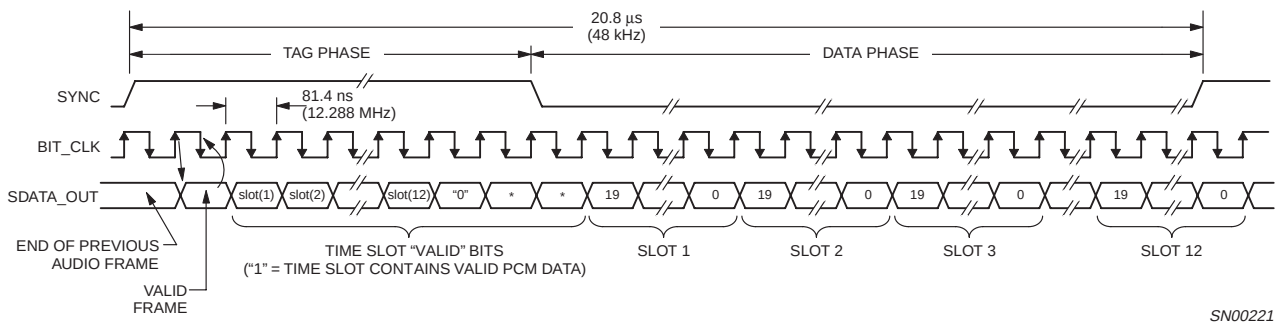
Fig 5. Standard bi-directional audio frame.

8.3.2 AC-link audio output frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting UCB1400's DAC inputs, and control registers. Each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Slot 0: TAG: Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the 'Valid Frame' bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by UCB1400 indicate which of the corresponding 12 time slots contain valid data. In this way, data streams of differing sample rates can be transmitted across AC-link at its fixed 48 kHz audio frame rate.

Figure 6 illustrates the time slot based AC-link protocol. (Note that Bits 1 and 0 of slot 0 tag phase are used for primary/secondary codec addressing as described in Section 8.4.



* See Table 4.

Fig 6. AC Link audio output frame.

A new audio output frame begins with a LOW-to-HIGH transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the UCB1400 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 Controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by UCB1400 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

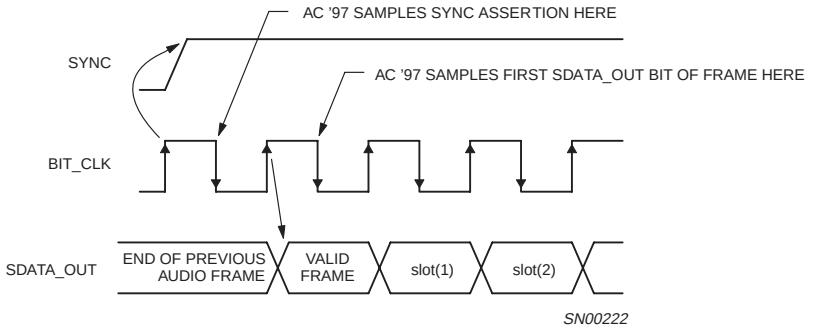


Fig 7. Start of an audio output frame.

SDAT_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0s by the AC '97 Controller. If there are less than 20 valid bits within an assigned and valid time slot, the AC '97 Controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0s.

Slot 1: Command address port: The command port is used to control features, and monitor status (see Section 8.3.3 "AC-link audio input frame (SDATA_IN)", Slots 1 and 2) for AC '97 functions including, but not limited to, sample rate, codec configuration, and power management.

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries, and reserves support for 64 odd addresses, as described in *AC '97 2.1 Component Specification Appendix D*. Only the even registers (00h, 02h, etc.) are currently defined, odd register (01h, 03h, etc.) accesses are reserved.

Note that shadowing of the control register file on the AC '97 Controller is an option left open to the implementation of the AC '97 Controller. UCB1400's control register file is readable as well as writable to provide more robust testability.

Audio output frame slot 1 communicates control register address, and write/read command information to the UCB1400.

Command Address Port bit assignments are:

- Bit(19) Read/write command (1 = read, 0 = write).
- Bit(18:12) Control register index (64 16-bit locations, addressed on even byte boundaries)
- Bit(11:0) Reserved (stuffed with 0s)

The first bit (MSB) sampled by UCB1400 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate with the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0s by the AC '97 Controller.

Slot 2: Command data port: The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19).

- Bit(19:4) Control Register Write Data (stuffed with 0s if current operation is a read).
- Bit(3:0) Reserved (stuffed with 0s)

If the current command port operation is a read, then the entire slot time must be stuffed with 0s by the AC ’97 Controller.

Slot 3: PCM playback left channel: Audio output frame slot 3 is the composite digital audio left playback stream. Typically, this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC ’97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20 bits is transferred, the AC ’97 Controller must stuff all trailing non-valid bit positions within this time slot with 0s.

Slot 4: PCM playback right channel: Audio output frame slot 4 is the composite digital audio right playback stream. Typically, this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC ’97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20 bits is transferred, the AC ’97 Controller must stuff all trailing non-valid bit positions within this time slot with 0s.

Slots 5 through 12: All other audio output frame slots are ignored by the UCB1400.

8.3.3 AC-link audio input frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC ’97 Controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits, which are used for AC-link protocol infrastructure.

Slot 0: TAG: Within slot 0, the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether UCB1400 is in the ‘Codec Ready’ state or not. If the ‘Codec Ready’ bit is a 0, this indicates that UCB1400 is not ready for normal operation. This condition is normal following the deassertion of power-on reset, for example, while UCB1400’s voltage references settle. When the AC-link ‘Codec Ready’ indicator bit is a logic 1, it indicates that the AC-link and UCB1400 control and status registers are in a fully operational state. The AC ’97 Controller must further probe the Power-down Control/Status Register (0x26) to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting UCB1400 into operation, the AC ’97 Controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that the UCB1400 has gone ‘Codec Ready’. Once the UCB1400 is sampled ‘Codec Ready’ then the next 12 bit positions sampled by the AC ’97 Controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 8 illustrates the time slot based AC-link protocol.

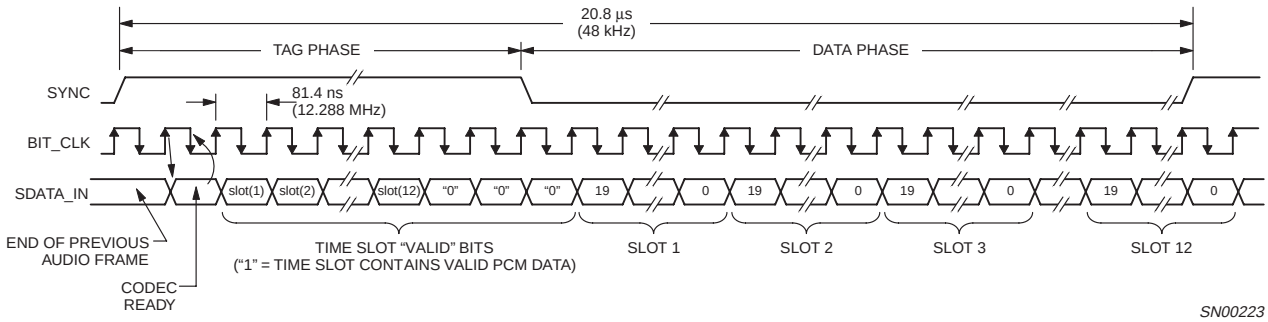


Fig 8. AC-link audio input frame.

A new audio input frame begins with a LOW-to-HIGH transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, UCB1400 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, UCB1400 transitions SDATA_IN into the first bit position of slot 0 (‘Codec Ready’ bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC ’97 Controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

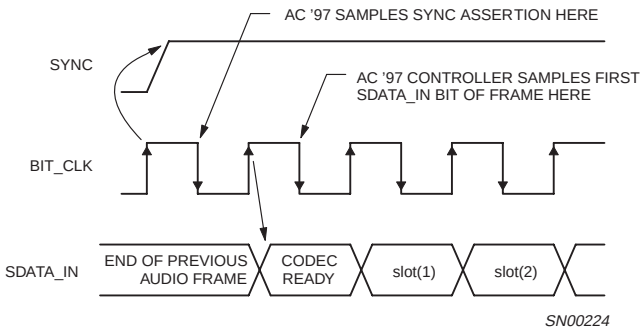


Fig 9. Start of an audio input frame.

SDATA_IN’s composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0s by the UCB1400. SDATA_IN data is sampled on the falling edges of BIT_CLK.

Slot 1: Status address port: The status port is used to monitor status for UCB1400 functions including, but not limited to, codec settings and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged 'valid' by UCB1400 during slot 0.)

Status address port bit assignments are:

- Bit(19) Reserved (stuffed with 0s)
- Bit(18:12) Control register index (echo of register index for which data is being returned)
- Bit(11:2) SLOTREQ bits: Only bits 11 and 10 (PCM L & R) shall be used by UCB1400. All unused bits shall be stuffed with 0s.
- Bit(1, 0) Reserved (stuffed with 0s)

The first bit (MSB) generated by UCB1400 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, the next 10 bits are the SLOTREQ bits, two of which (bits 11 and 10) are used by UCB1400 to request data using the variable sample rate signaling protocol as defined in the *AC '97 Component Specification*. The trailing 2 bit positions are stuffed with 0s by UCB1400.

Slot 2: Status data port: The status data port delivers 16-bit control register read data.

- Bit(19:4) Control register read data (stuffed with 0s if tagged 'invalid' by UCB1400)
- Bit(3:0) Reserved (stuffed with 0s)

If slot 2 is tagged invalid by UCB1400, then the entire slot will be stuffed with 0s by UCB1400.

Slot 3: PCM record left channel: Audio input frame slot 3 is the left channel output of UCB1400's input MUX, post-ADC. The UCB1400's ADCs are implemented to support 20-bit resolution. UCB1400 ships out its ADC output data (MSB first) to fill out its 20-bit time slot.

Slot 4: PCM record right channel: Audio input frame slot 4 is the right channel output of UCB1400's input MUX, post-ADC. The UCB1400's ADCs are implemented to support 20-bit resolution. UCB1400 ships out its ADC output data (MSB first) to fill out its 20-bit time slot.

Slot 12: GPIO status: Audio output frame slot 12 is used to carry modem GPIO input data. Table 3 shows the definition by *AC '97 Component Specification*. The UCB1400 does not make use of slot 12 to report its IO pin status. It only uses the GPIO_INT as an optional means (when the GIEN bit is set in the Feature CSR1 register) to signify an interrupt event (in addition to pin IRQOUT).

Table 3: Slot 12 definition

Bit	GPIO	Name	Sense	Description
19-4	GPIO[15:0]		in/out	Modem GPIO as defined by the *Intel AC '97 Component Specification*.
3-1		Vendor rsrvd		Vendor optional.
0		GPIO_INT	in	GPIO_INT (uses same logic as wake-up event)

Slots 5 through 11: All other audio input frame slots shall be stuffed with 0s by the UCB1400.

8.3.4 AC-link low power mode

The AC-link signals can be placed in a low power mode. When the UCB1400's PR4 bit is set to '1' in the Power-down status and control register (0x26), both BIT_CLK and SDATA_IN will be brought to, and held at, a logic LOW voltage level.

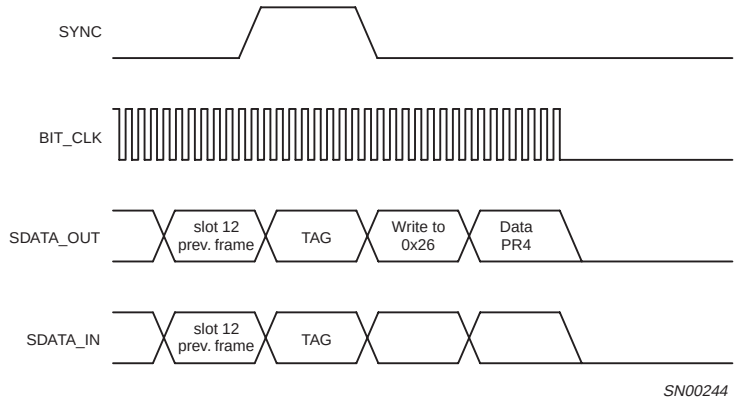


Fig 10. AC-link power-down timing.

BIT_CLK and SDATA_IN are transitioned low immediately following the decode of the write to Register 0x26 with PR4. When the AC '97 Controller driver is at the point where it is ready to program the AC-link into its low power mode, slots (1 and 2) **are assumed to be** the only valid stream in the audio output frame.

The AC '97 Controller should also drive SYNC and SDATA_OUT LOW after programming UCB1400 AC '97 to this low power, halted mode. The AC '97 Controller is required to drive and keep SYNC and SDATA_OUT LOW in this low power, halted mode.

Once the UCB1400 has been instructed to halt BIT_CLK, a special 'wake-up' protocol must be used to bring the AC-link to the active mode since normal audio output and input frames cannot be communicated in the absence of BIT_CLK.

Waking up the AC-link: There are two methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC '97 Controller that performs the wake-up task.

AC-link protocol provides for a 'Cold AC '97 Reset', and a 'Warm AC '97 Reset'. The current power-down state would ultimately dictate which form of AC '97 reset is appropriate. Unless a 'cold' or 'register' reset (a write to the Reset register) is performed, wherein the UCB1400 registers are initialized to their default values, registers are required to keep state during all power-down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the power-down was triggered. When AC-link powers-up, it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold AC '97 reset: A cold reset is achieved by asserting $\overline{\text{RESET}}$ for the minimum specified time. By driving $\overline{\text{RESET}}$ LOW, all UCB1400 control registers will be initialized to their default power-on reset values. BIT_CLK and SDATA_OUT will be activated, or re-activated as the case may be. $\overline{\text{RESET}}$ is an asynchronous input to the UCB1400.

Warm AC '97 reset: A warm AC '97 reset will re-activate the AC-link without altering the current AC '97 register values. A warm reset is signaled, in the absence of BIT_CLK, by driving SYNC HIGH for a minimum of 1 µs.

Within normal audio frames, SYNC is a synchronous input to the UCB1400. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the UCB1400.

The UCB1400 **must not** respond with the activation of BIT_CLK until SYNC has been sampled LOW again by the UCB1400. This will preclude the false detection of a new audio frame.

8.4 Accessing the UCB1400

The UCB1400 supports only primary codec configuration. Typically, the UCB1400 expects a 24.576 MHz crystal across the XTL_IN and XTL_OUT pins. Alternatively, an external 24.576 MHz clock can be applied to XTL_IN.

Table 4: AC-link audio output frame slot 0 bit allocation

Bit	Description
15	Frame valid
14	Slot 1 valid command address bit (primary codec only)
13	Slot 2 valid command data bit (primary codec only)
12-3	Slot 3-12 valid bits as defined by *AC '97 Component Specification*
2	Reserved (set to 0)
1-0	2-bit codec ID field 00 reserved for primary 01, 10, 11 indicate secondary

In order for the AC ’97 Digital Controller to access the UCB1400, the 2-bit Codec ID field (chip select) (LSBs of Output Slot 0) must be set to ‘0’ (see Table 4). The UCB1400 shall monitor the Frame Valid, Slot 1 Valid Command Address, Slot 2 Valid Command Data and Codec ID bits, and respond only if properly accessed by the AC ’97 Digital Controller, as illustrated in Table 5. Note that although SLOTREQ bits reside in slot 1, they have validity independent of the tag bit for Valid Slot 1 Address. The UCB1400 shall only set SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to ‘1’ when returning valid data from a previous register read, regardless of the validity of SLOTREQ bits (see also Section 8.5).

Table 5: UCB1400 response to AC ’97 digital controller access

Function	Slot 0, bit 15 (Valid frame)	Slot 0, bit 14 (Valid Slot 1 address)	Slot 0, bit 13 (Valid Slot 2 data)	Slot 0, bits 1-0 (codec ID)	Action
AC ’97 digital controller primary read frame N, SDATA_OUT	1	1	0	00	AC ’97 controller reads UCB1400 register
UCB1400 status frame N+1, in response to AC ’97 digital controller primary read frame N, SDATA_IN	1	1	1	00	UCB1400 returns register status
AC ’97 digital controller primary write frame N, SDATA_OUT	1	1	1	00	AC ’97 controller writes UCB1400 register
UCB1400 status frame N+1, in response to AC ’97 digital controller primary write frame N, SDATA_IN	1	0	0	00	UCB1400 writes register internally and returns nothing
AC ’97 digital controller secondary read or write frame N, SDATA_OUT	1	0	0	01, 10 or 11	AC ’97 controller reads or writes secondary codec
UCB1400 status frame N+1, in response to AC ’97 digital controller secondary read or write frame N, SDATA_IN	1	0	0	00	UCB1400 ignores commands and returns nothing

8.5 Variable sample rate signaling protocol

The AC-link is defined for a fixed transfer rate of 48 kHz. To support the diverse sample rates, UCB1400 implements the Variable Sample Rate Signaling Protocol of the *AC '97 Component Specification*:

- To control the AC '97 Controller to input a rate other than 48 kHz, the UCB1400 uses the tag bit for slot 3 and 4 (PCM L & R) to indicate whether valid data is present or not.
- To control the AC '97 Controller to output a rate other than 48 kHz, the UCB1400 uses the active-low SLOTREQ bit for slot 3 and slot 4 (PCM L & R) to indicate whether it needs data from the AC '97 Controller.

8.5.1 SLOTREQ protocol

To control the AC '97 Controller to output a rate other than 48 kHz, the UCB1400 examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (LOW). SLOTREQ bits asserted during the current audio input frame signal which active output slots require data from the AC '97 Digital Controller in the next audio output frame. An active output slot is defined as any slot supported by UCB1400 that is not in a power-down state.

In case of UCB1400, the only SLOTREQ bits used are that for slot 3 and slot 4 request (bits 11 and 10 of input slot 1). SLOTREQ bits for all other slots shall be stuffed with 0s by UCB1400. Note that although SLOTREQ bits reside in slot 1, their validity does not depend on the tag bit for Valid Slot 1 Address (see also Section 8.4).

8.6 Wake-up support

Pressing the touch screen is an example of events that might need to wake-up the host CPU that has suspended into a low power state. Figure 11 shows the AC Link power-down/power-up sequence. The UCB1400 powers down the AC Link subsequent to its PR4 bit being programmed to 1. When enabled to wake on, e.g., a touch screen event, a wake event causes the UCB1400 to transition IRQOUT from LOW to HIGH. The system controller can use this information as a signal to wake up. Subsequently, the first thing that the device driver must do to reestablish communications with the UCB1400 is to command the AC '97 Digital Controller to execute a warm reset to the AC Link. Alternatively, if the GIEN bit in the Feature CSR1 register (0x6A) is set, a wake event will cause the UCB1400 to transition its SDATA_IN from LOW to HIGH. The UCB1400 shall keep SDATA_IN HIGH until it has sampled SYNC having gone HIGH, and then LOW.

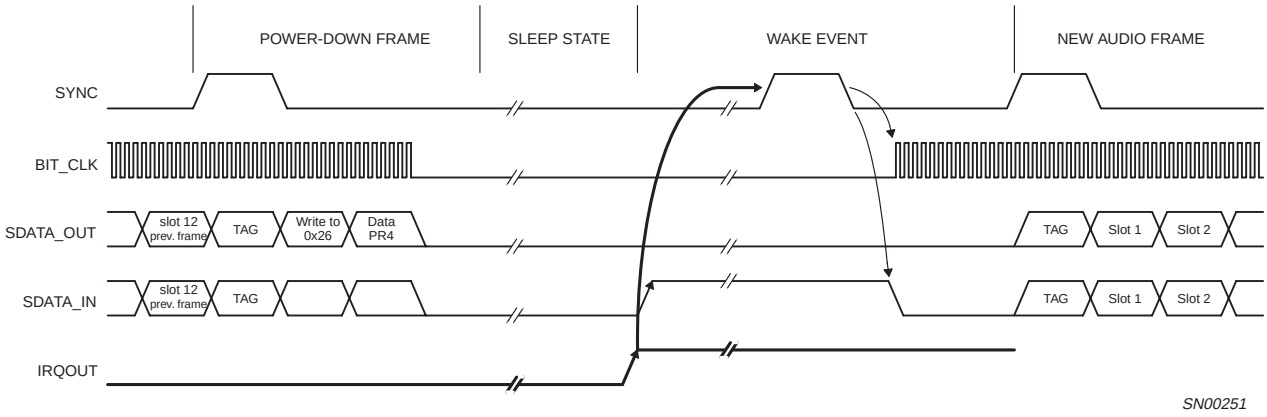


Fig 11. AC Link power-down/power-up sequence.

Before enabling wake-up via IRQOUT or GIEN bit, the UCB1400 must be enabled for interrupt by setting the appropriate bits in the Positive INT Enable register (0x5E) and Negative INT Enable register (0x60). The INT Clear/Status register (0x62) should then be cleared of any previous interrupts before going to low-power mode.

8.7 Test modes

AC '97 Component Specification defines two test modes. One is for ATE in-circuit test, and the other if for vendor-specific tests. The UCB1400 enters the ATE in-circuit test mode if SDATA_OUT is sampled HIGH at the trailing edge of $\overline{\text{RESET}}$. The UCB1400 enters the vendor-specific test mode when coming out of reset if SYNC is HIGH. These cases will never occur during standard operating conditions. Regardless of the test mode, the AC '97 Controller must issue a cold reset to resume normal operation of the UCB1400.

8.7.1 ATE in-circuit test mode

When the UCB1400 is placed in the ATE test mode, its digital AC-link outputs (i.e., BIT_CLK and SDATA_IN) shall be driven to a high impedance state. This allows ATE in-circuit testing of the AC '97 Controller.

8.7.2 Vendor-specific test mode

When the UCB1400 is placed in the vendor-specific test mode, the Test Control register (Index 0x6E) determines the kind of tests to be performed.
Refer to Section 12 "Register definition" for details.

8.8 General purpose IOs

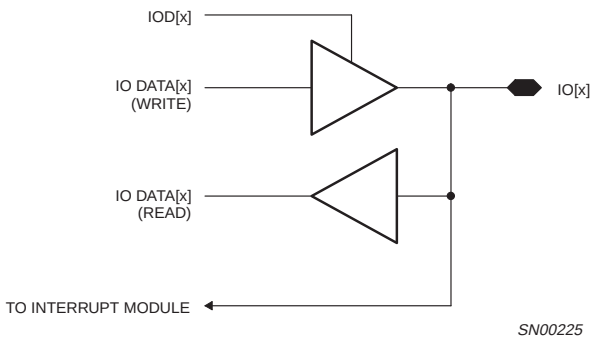


Fig 12. Block diagram of IO pin circuitry.

The UCB1400 has 10 programmable digital input/output (I/O) pins. These pins can be independently programmed as input or output using the IOD[9:0] bits in the IO Direction Register (0x5C). The output data is determined by the content of the IO[9:0] bits in the IO Data Register (0x5A), while the actual status of these pins can be read from the same register bits.

The data on the IO[9:0] pins are fed into the interrupt control block, where they can generate an interrupt on the rising and/or falling edge of these signals.

8.9 Interrupt generation

The UCB1400 contains a programmable interrupt control block, which can generate an interrupt for a 0-to-1 and/or 1-to-0 transition on one or more of the IO[9:0] pins, the audio overload detection, the ADC Ready signal, and the TSPX and TSMX signals.

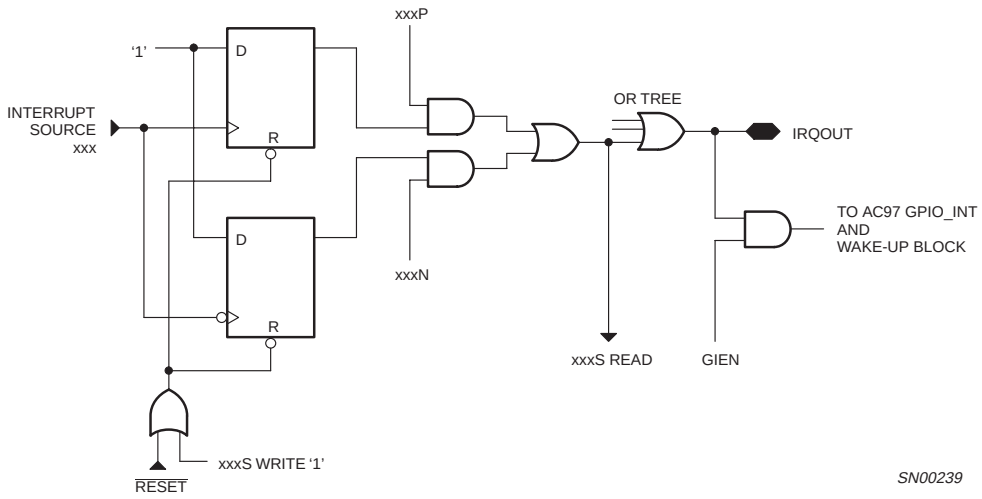


Fig 13. Block diagram of the interrupt controller.

The interrupt generation mode is set by the Positive INT Enable Register (0x5E) and Negative INT Enable Register (0x60). The actual interrupt status of each signal can be read from the INT Clear/Status Register (0x62). The interrupt status is cleared whenever a ‘1’ is written in the INT Clear/Status Register (0x62) for the corresponding bit.

The interrupt controller is implemented asynchronously. This provides the possibility to generate interrupts when the BIT_CLK is stopped, e.g., an interrupt can be generated in power-down mode when the touch screen is pressed or when the state of one of the IO pins changes.

The IRQOUT pin presents the ‘OR’ function of all interrupt status bits and can be used to give an interrupt to the system controller.

When the GIEN bit of the Feature Control/Status Register 1 (0x6A) is set, the IRQOUT signal is communicated to the AC Link by means of:

- GPIO_INT bit of input slot 12 when BIT_CLK is on.
- Rising SDATA_IN when BIT_CLK is off.

9. Audio codec

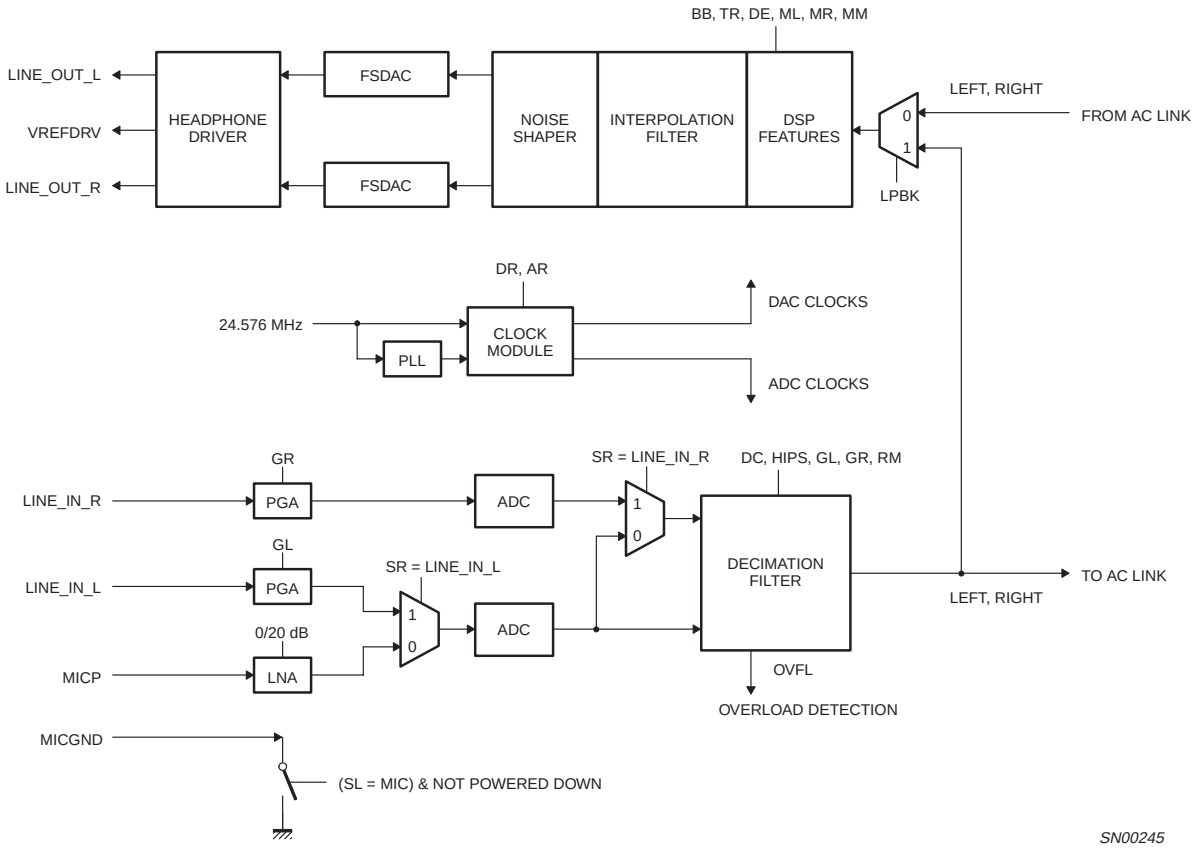


Fig 14. Audio codec block diagram.

9.1 ADC analog front-end

The analog front-end of the UCB1400 consists of one stereo ADC with a selector in front of it. Using this selector, one can either select the microphone input with a dedicated Low Noise Amplifier (LNA), or the line input with a Programmable Gain Amplifier (PGA). Via appropriate AC '97 register settings, the following modes can be supported:

- Standby mode: all PGAs, LNA and ADCs are powered down.
- Stereo line in mode: the PGAs are used, and the LNA is powered down.
- Microphone mode: the PGAs and right channel ADC are powered down, and MICGND switch is on. The mono microphone signal can be sent to both left and right input of the decimation filter via a MUX in front of the decimation input.
- One line-in and one microphone mode: the left PGA is powered down.

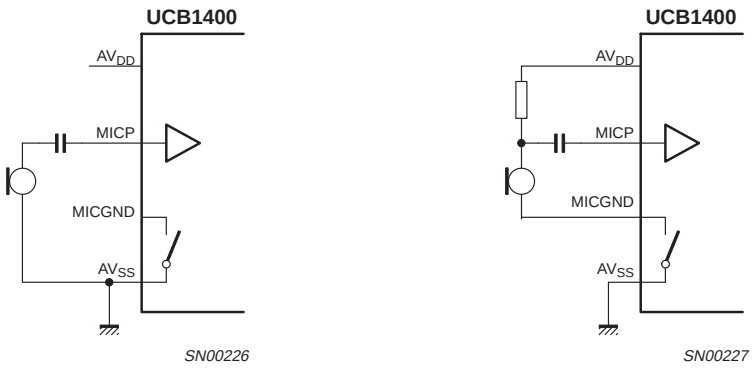
9.1.1 Line inputs

The analog front-end of the UCB1400 consists of two stereo ADCs with a programmable gain stage. The full scale input voltage of the line input path is programmable in 1.5 dB steps independently for the left and right channels by setting the GL[3:0] and GR[3:0] bits in the Record Gain Register (0x1C).

9.1.2 Microphone input

The UCB1400 audio codec input path accepts microphone signals via a DC blocking capacitor. The 'ground' side of the microphone is either connected to the analog ground (AV_{SS}) or to the MICGND pin of the UCB1400. The latter will decrease the current consumption of active microphones, since the MICGND pin is made Hi-Z when the microphone input is not selected (SL = LINE_IN_L in Record Select register (0x1A)).

The LNA gain can be set to 0 or 20 dB via the 20 dB bit in the MIC Volume register (0x0E). Additional gain in 1.5 dB steps is possible via the GL[3:0] in the Record Gain register (0x1C).



a. 'Passive' microphone.

b. 'Active' microphone.

Fig 15. Possible microphone connections.

9.1.3 Decimation filter

The decimation from 128 fs is performed in two stages. The first stage realizes sin(x)/x characteristics with decimation factor of 16. The second stage consists of 3 half-band filters, each decimating by a factor of 2. The filter characteristics are shown in Table 6.

Table 6: Decimation filter characteristics

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.45 fs	±0.015
Stop band	> 0.55 fs	−60
Dynamic range	0 to 0.45 fs	> 135

Two bits in the Feature Control/Status Register 1 (0x6A) provide control over DC filtering:

- DC bit: controls the DC filter before the decimator used to compensate the DC offset is added in the ADC to remove idle tones from the audio band.
- HIPS bit: controls the DC filter at the output of the decimation filter.

9.1.4 Overload detection

An overload detection circuit will inform the user whenever the input voltage exceeds the maximum input voltage, which will lead to a high distortion. In that case, the OVFL bit in the Feature Control/Status Register 1 (0x6A) is set. In addition, an interrupt is generated on the IRQOUT pin of the UCB1400 whenever the **OVLP bit** or the **OVLN bit** is set in the Positive and/or Negative INT Enable Registers.

9.2 Interpolation filter (DAC)

The digital interpolation filter interpolates from 1 fs to 128 fs by means of a cascade of FIR filters. The filter characteristics are shown in Table 7.

Table 7: Interpolation filter characteristics

Item	Condition	Value (dB)
Pass-band ripple	0 to 0.45 fs	±0.025
Stop band	> 0.55 fs	−65
Dynamic range	0 to 0.45 fs	> 135

9.2.1 DSP features

The UCB1400 supports the following DSP (Digital Sound Processing) features through the Feature Control/Status register 1 (0x6A):

- Tone control: Bass Boost (BB[3:0]) and Treble Boost (TR[1:0])
- Flat/Minimum/Maximum setting for bass and treble boost (M[1:0])
- De-emphasis control (DE bit)

In addition, the UCB1400 supports volume control and soft muting via the Master Volume register (0x02):

- Master volume control: The output level can be attenuated in 1.5 dB steps down to −94.5 dB independently for the left and right channels via the Master Volume Register (0x02).
- Mute: The output is muted when the MM bit in the Master Volume Register is set. Muting the DAC will result in a cosine roll-off soft mute, using 128 samples in the normal mode: this results in 3 ms at fs = 44.1 kHz.

9.2.2 Noise shaper

The 3rd-order noise shaper operates at 128 fs. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream Digital-to-Analog Converter (FSDAC).

9.2.3 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way, very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output. The output voltage of the FSDAC scales proportionally with the power supply voltage.

9.2.4 Headphone driver

The headphone driver a reference output that acts as the virtual ground. This allows direct connection to a stereo headphone without the use of external DC blocking capacitors. The headphone driver is enabled when HPEN is set to ‘1’ in the Feature Control/Status Register 1 (0x6A).

The headphone driver is equipped with a short circuit protection on each of the LINE_OUT_L, LINE_OUT_R and VREFDRV output. When HPEN = 1, the short circuit protection circuit will inform the user in case the limiter is activated, e.g., in case of short circuit, by setting the corresponding bit (CLPL, CLPR or CLPG) in the Extra Interrupt register (0x70). In addition, an interrupt is generated on the IRQOUT pin of UCB1400 whenever the CLPP or CLPN bit is set in the Positive and/or Negative INT Enable Registers. In that case, the CPLS bit will be set in the INT Clear/Status register (index 0x62). The user can subsequently examine the Extra Interrupt register (0x70) to determine the source of the short circuit.

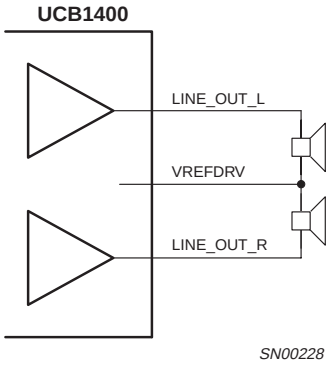


Fig 16. Headphone connections.

9.3 Loopback mode

The audio codec incorporates a loopback mode, in which codec input path and output path are connected in series. It is activated when the LPBK bit in the General Purpose register (0x20) set. The loopback internally connects the digital output from the decimator of the ADC to the digital input of the Interpolator of the DAC, allowing for codec testing without the use of the AC Link.

9.4 PLL and sample rates

The audio sample rate is derived from the 24.576 MHz crystal clock for 8, 12, 16, 24, 32, and 48 kHz sample rates, and from the built-in PLL for 11.025, 22.05 and 44.1 kHz sample rates. The ADC and DAC can run at independent sample rates and are controlled by the ADC and DAC Sample Rate registers (0x32 and 0x2C).

9.5 Power-down modes

The audio input and output paths can be powered down independently; the input path is powered down when the PR0 bit in the Power-down Control/Status register (0x26) is set. The output path is disabled when the PR1 bit of the same register is set. This provides the user the means to reduce the current consumption of UCB1400 if one part of the audio codec is not used in the application. When both the input and output paths are disabled, the PR3 bit of the same register can also be set to turn off the audio reference to further reduce power consumption.

If the Smart Low Power bits (SLP0 and SLP1) are set in the Feature Control/Status Register 2 (0x6C), the UCB1400 will power down unused blocks in the audio ADC analog front end and the PLL in a smart way, ensuring the lowest power consumption in each audio operating mode.

10. Touch screen interface

10.1 Universal touch screen matrix

The UCB1400 contains a universal touch screen interface for 4-wire resistive touch screen, capable of performing position, pressure and plate resistance measurements. In addition, the touch screen can be programmed to generate interrupts when the touch screen is pressed. The last mode is also active when the UCB1400 is set in the stand-by mode.

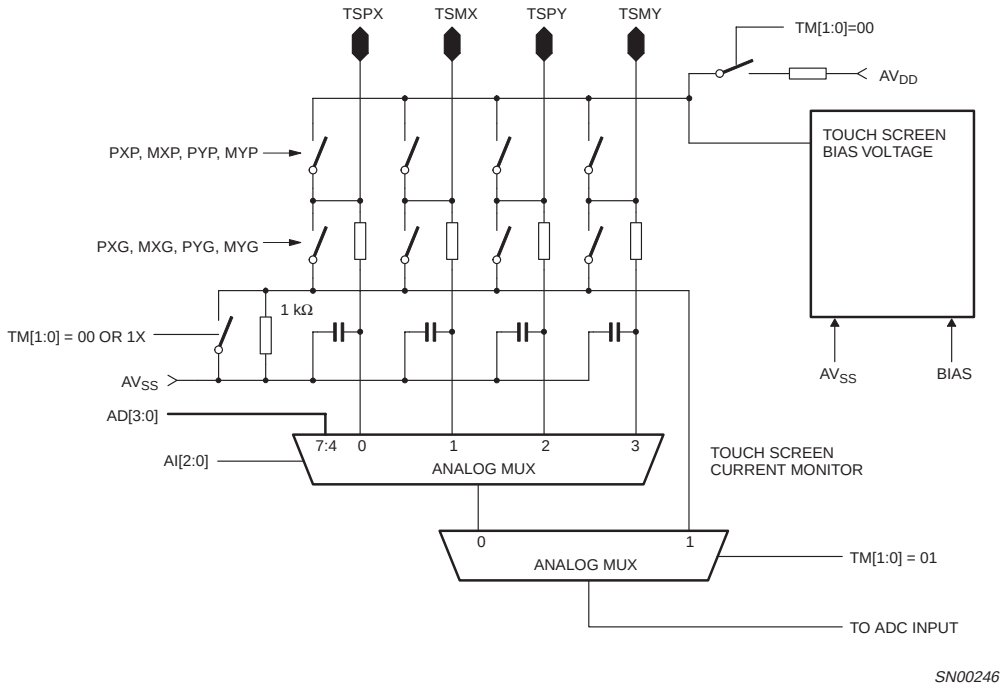


Fig 17. Block diagram of the touch screen interface.

The touch screen interface connects to the touch screen by four wires: TSPX, TSMX, TSPY and TSMY. Each of these pins can be programmed to be floating, powered or grounded in the touch screen switch matrix. The setting of each touch screen pin is programmable by the PXP, MXP, PYP, MYP and PXG, MYG, PYG, MYG bits in the touch screen control register. Possible conflicting settings (grounding and powering of a touch screen pin at the same time) are detected by the UCB1400. In that case, the UCB1400 will ground the touch screen pin.

Each of the four touch screen signals can be selected as input for the built-in 10-bit ADC, which is used to determine the voltage on the selected touch screen pin in position measurement mode. In addition, the UCB1400 can monitor touch screen current via an internal 1 kΩ resistor that can act as the input to the 10-bit ADC in pressure or plate resistance measurement mode. The flexible switch matrix and the multi-functional touch screen bias circuit enable the user of the UCB1400 to set each desired touch screen configuration.

The UCB1400's internal voltage reference (V_{ref}) acts as the reference voltage for the touch screen bias circuitry. This makes the touch screen biasing independent of supply voltage and temperature variations. Four low pass filters, one on each touch screen terminal, are built in to minimize the noise coupled from the LCD into the touch screen signals. An LCD typically generates large noise glitches on the touch screen, since they are closely coupled.

The setting of the touch screen bias circuitry and the ADC multiplexer is determined by the setting of TM[1:0] in the touch screen control register according to Table 8.

Table 8: Touch screen mode selection

TM[1:0]	Selected mode	Touch screen bias source	ADC multiplexer setting
00	Interrupt	Resistor to AV_{DD}	Defined by AI[2:0]
01	Pressure	Touch screen bias circuit	Touch screen current monitor
10	Position	Touch screen bias circuit	Defined by AI[2:0]
11	Position	Touch screen bias circuit	Defined by AI[2:0]

10.2 Operational modes

The UCB1400 supports three modes of touch screen measurements: position, pressure, and plate resistances. Additionally, an interrupt mode is provided for detection of touch events.

10.2.1 Position measurement

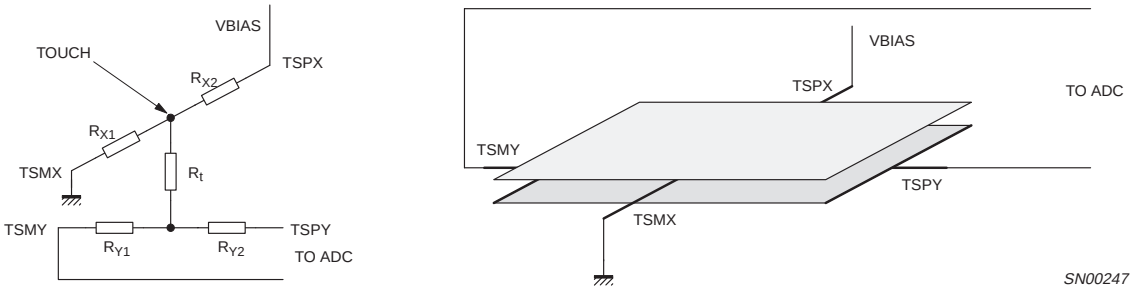


Fig 18. Touch screen setup for X position measurement.

Two position (X, Y) measurements are needed to determine the location of the pressed spot. The X plate is biased during the X position measurement and the voltage on one or both Y terminals (TSPY, TSMY) is measured. The circuit can be represented by a potentiometer, with the TSPY and/or TSMY electrode being the 'wiper'. The measured voltage on the TSPY/TSMY terminal is proportional to the X position of the pressed spot of the touch screen.

In the Y position mode, the X plate and Y plate terminals are interchanged, thus the Y plate is biased and the voltage on the TSPX and/or TSMX terminal is measured.

10.2.2 Pressure measurement

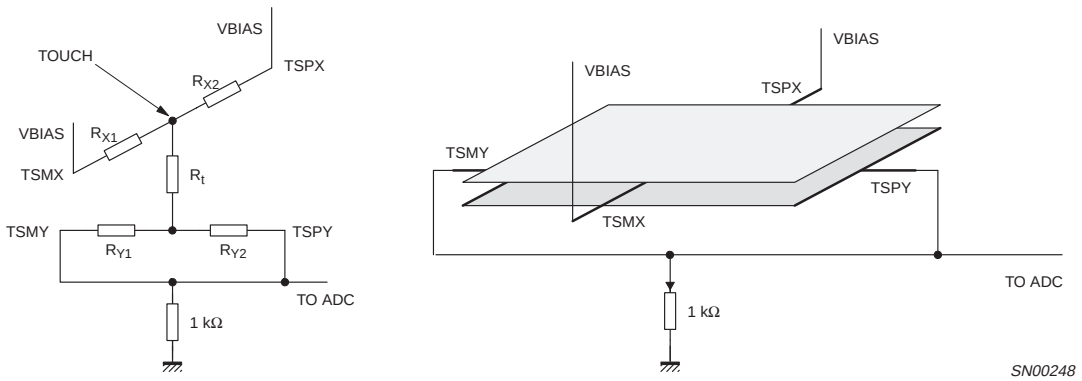


Fig 19. Touch screen setup for pressure-1 measurement (see Table 9).

The pressure applied to the touch screen can be determined. In fact, the contact resistance between the X and Y plates is measured, which is a good indication of the size of the pressed spot and the applied pressure. A soft stylus, e.g., a finger, leads to a rather large contact area between the two plates when a large pressure is applied. A hard stylus, e.g., a pen, leads to less variation in measured contact resistance since the contact area is rather small.

One plate is biased at one or both terminals during this pressure measurement, whereas the other plate is grounded, again on one or both terminals. The current flowing through the touch screen is a direct indication for the resistance between both plates. A compensation for the series resistance, formed by the touch screen plates and the internal 1 kΩ resistance of the UCB1400 will improve the accuracy of this measurement.

10.2.3 Plate resistance measurement

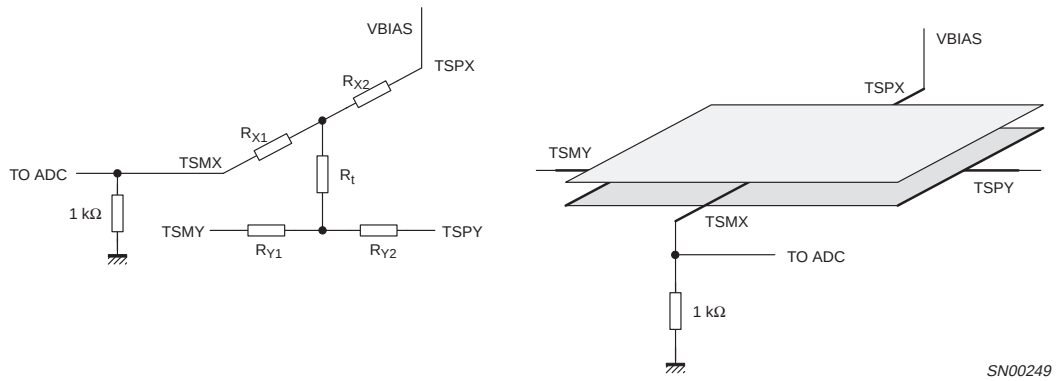


Fig 20. Touch screen setup for X plate resistance measurement.

The plate resistance of a touch screen varies a lot due to processing spreads. Knowing the actual plate resistance makes it possible to compensate for the plate resistance effects in the pressure resistance measurements. Secondly, the plate resistance decreases when two or more spots on the touch screen are pressed. In that case, a part of one plate, e.g., the X plate, is shorted by the other plate, which decreases the actual plate resistance.

The plate resistance measurement is executed in the same way as the pressure resistance measurement. In this case, only one of the two plates is biased, and the other plate is kept floating. The current through the connected plate is again a direct indication of the connected resistance.

10.2.4 Interrupt mode

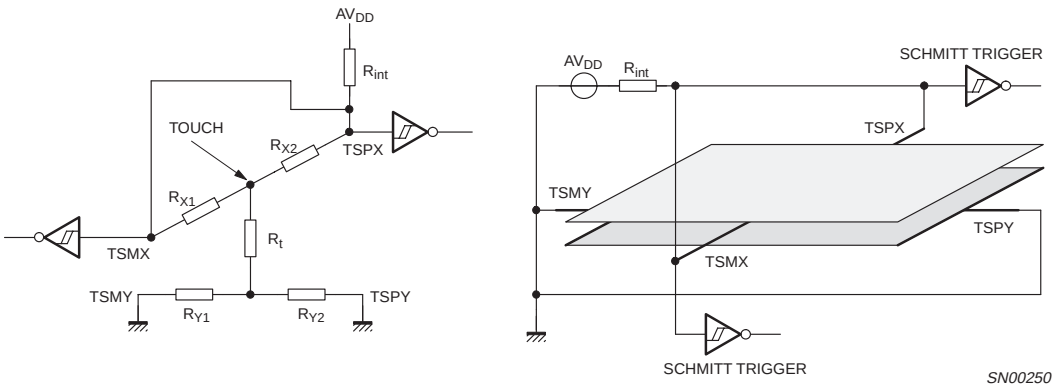


Fig 21. Touch screen setup for interrupt detection.

In addition to the measurements made above, the touch screen can also act as an interrupt source. In this mode, the X plate of the touch screen has to be powered, and the Y plate has to be grounded. In this case, the touch screen is not biased by the active touch screen bias circuit, but by a resistor to AV_{DD}. This configuration simply biases the touch screen and the UCB1400 does not consume power unless the touch screen is touched. The voltage on the X plate terminals drops if the screen is pressed. This voltage drop is detected by Schmitt trigger circuits, of which the outputs are connected to the interrupt control block. A touch screen interrupt is generated either when the touch screen is pressed (falling edge enabled) or when the touch screen is released (rising edge enabled), which can be used to activate the system around the UCB1400 to start a touch screen readout sequence. The internal Schmitt trigger circuits are connected to the TSPX and TSMX signals after the built-in low-pass filters. This reduces the number of spurious interrupts, due to the coupling between the LCD screen and the touch screen sensors.

10.2.5 Mode summary

Table 9: Measurement mode summary

Touch screen measurement	PXP	PXG	MXP	MXG	PYP	PYG	MYP	MYG	BIAS	TM	AI
X position[1]	1	0	0	1	0	0	0	0	1	2	2 or 3
Y position[1]	0	0	0	0	1	0	0	1	1	2	0 or 1
Pressure - 1[2]	1	0	1	0	0	1	0	1	1	1	Any
Pressure - 2[2]	1	0	0	0	0	1	0	0	1	1	Any
Pressure - 3[2]	0	0	0	1	1	0	0	0	1	1	Any
Pressure - 4[2]	0	0	1	0	0	0	0	1	1	1	Any
Pressure - 5[2]	0	1	0	0	0	0	1	0	1	1	Any
X plate resistance	1	0	0	1	0	0	0	0	1	1	Any
Y plate resistance	0	0	0	0	1	0	0	1	1	1	Any
Interrupt	1	0	1	0	0	1	0	1	0	0	Any

[1] For X and Y position measurements, (PXP, PXG, PYP, PYG) can be swapped with (MXP, MXG, MYP, MYG) to get readings reversed in direction.

[2] For pressure measurements, (PXP, PXG, PYP, PYG) can be swapped with (MXP, MXG, MYP, MYG) to get the same readings with current flowing in the opposite direction.

11. 10-bit ADC

The UCB1400 includes a 10-bit successive approximation analog-to-digital converter (ADC) with built-in track-and-hold circuitry, and an analog multiplexer to select one of the four analog inputs (AD0-3), the four touch screen inputs (TSPX, TSMX, TSPY, TSMY) or the current of the touch screen bias circuit. The analog multiplexer contains four resistive dividers to attenuate the high voltages on the AD0-3 inputs to the ADC input range.

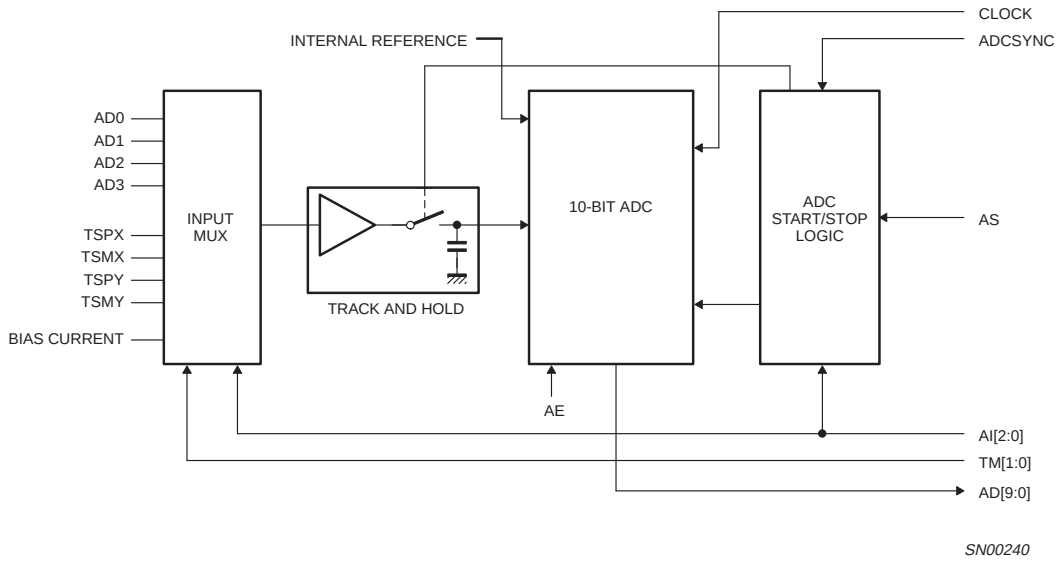


Fig 22. Block diagram of the 10-bit ADC circuit.

The ADC is controlled through the AC '97 interface, but the UCB1400 contains internal logic to ease the control of the ADC and to minimize the number of AC '97 frame read/write actions.

The ADC is activated by the AE bit in the ADC Control register (0x66). The ADC circuitry, including the track and hold circuitry does not consume any power as long as this bit is reset. The analog input multiplexer is controlled by the AI[2:0] bits and the ADC is actually started with the AS bit in the ADC Control register (0x66).

A complete ADC control sequence consists of several phases. First the ADC has to be enabled; secondly, the input selector must be set to the proper input; thirdly, the ADC conversion has to be started; and finally, the ADC result has to be read from the ADC Data register (0x68).

The UCB1400 has two different modes to start the ADC conversion, which are selected by the ASE bit in the ADC Control register (0x66). When ASE is '0', the ADC conversion is started directly by writing a '1' in the AS bit. If the AVE bit in the Feature/Control Status Register 2 (0x6C) is set to '1', additional filtering is applied to the ADC data, making it more immune to high frequency fluctuations in a noisy environment.

When ASE is ‘1’, the ADC is started at a rising edge of the signal applied to the ADCSYNC pin. In this mode, writing ‘1’ to the AS bit will arm the ADC, such that it will start in the first detected rising edge of the ADCSYNC signal. A rising edge of the signal connected to the ADCSYNC pin occurring during the tracking time is ignored; the ADC conversion is started on the first rising edge detected after this delay time. This mode is particularly useful when the internal ADC has to be synchronized to the external system. Note that the AVE bit should not be set to ‘1’ when ASE is ‘1’.

The result of the conversion is stored in the ADC Data register (0x68), after the completion of the conversion. An interrupt may be generated whenever a conversion is completed (ADCP and/or ADCN bits in the Positive and Negative INT Enable registers) to ease the synchronization between the UCB1400 and the system controller. The ADV bit in the ADC Data register 0x68 indicates the status of the ADC data; it equals ‘0’ when an ADC sequence is started, which implies that the ADC result is not valid, and it equals ‘1’ when the ADC conversion is completed and the result is stored in the ADC Data register (0x68).

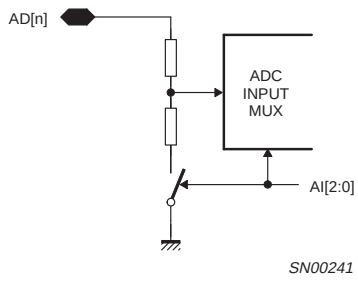


Fig 23. AD0-AD3 resistive dividers block diagram.

The applied voltage on the four analog inputs of the UCB1400 (AD0-AD3) is attenuated before it is applied to the ADC input multiplexer using on-chip resistive dividers. These high voltage inputs are optimized to handle voltages larger than the used supply voltage. The built-in resistive voltage dividers are only activated if the corresponding analog input is selected. The resistive dividers are made floating when the input is not selected by the ADC input multiplexer, such that the input leakage of these high voltage analog pins is minimized. This makes these analog inputs very suitable to monitor battery voltages.

11.1 On-chip reference circuit

The UCB1400 contains an on-chip reference voltage source, which generates the reference voltage for the 10-bit ADC and touch screen bias. The internal bandgap circuit is activated if the 10-bit ADC or touch screen function is activated. This reduces the current consumption of the UCB1400 in standby mode.

The internal reference voltage is connected to the VREFBYP pin, where an external capacitor can be connected to filter this reference voltage, if the VREFB bit (register 0x66) is set to ‘1’.

12. Register definition

The following tables describe the register definition for the UCB1400. The UCB1400 shall follow the *AC '97 2.1 Interoperability Requirements and Recommendations* as follows:

- Non-implemented or reserved register bits: All reserved or non-implemented register bits (marked 'X' in the tables) are required to return '0' when read.
- Non-implemented Addresses: Read access to non-implemented registers are required to echo a 'valid' 7-bit register address in Input Slot 1 and return 'valid' 0x0000 data in Input Slot 2 on the next AC-link frame.
- Odd Register Addresses: Read (and write) access to odd register addresses are required to be treated the same as non-implemented addresses, instead of aliasing them to the next lower even-numbered register.
- Codec register read data need to be returned in the next AC-link frame following the frame in which the read request occurs.
- Codec-Ready and audio DAC/ADC status bits shall only change from 'ready' to 'not ready' in response to a PR state change issued by the Controller to the Power-down Control/Status registers 0x26. This guarantees that once data is actively flowing on a slot, the Controller does not have to continuously read the Power-down Control/Status register to detect any unexpected Codec PR status change.

Table 10: Register definitions

Shaded registers are read-only.

Reg (HEX)	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
00	Reset	X	X	X	X	X	X	ID9	X	ID7	X	ID5	X	X	X	X	X	02A0
02	Master Volume	MM	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000
04-0C	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0E	MIC Volume	X	X	X	X	X	X	X	X	X	20dB	X	X	X	X	X	X	0000
10-18	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1A	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000
1C	Record Gain	RM	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000
1E	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
20	General Purpose	X	X	X	X	X	X	X	X	LPBK	X	X	X	X	X	X	X	0000
1E-24	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
26	Power-down Control/Status	X	X	PR5	PR4	PR3	X	PR1	PR0	X	X	X	X	REF	X	DAC	ADC	000X
28	Ext'd Audio ID	ID1	ID0	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0001
2A	Ext'd Audio Status/Control	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000
2C	Audio DAC rate	DR15	DR14	DR13	DR12	DR11	DR10	DR9	DR8	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	BB80
2E-30	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
32	Audio ADC rate	AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0	BB80
34-58	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
5A	IO data	X	X	X	X	X	X	IO9	IO8	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	0000
5C	IO direction	X	X	X	X	X	X	IOD9	IOD8	IOD7	IOD6	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0	0000
5E	Positive INT enable	OVLP	CLPP	TMXP	TPXP	ADCP	X	IOP9	IOP8	IOP7	IOP6	IOP5	IOP4	IOP3	IOP2	IOP1	IOP0	0000

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Table 10: Register definitions...*continued*

Shaded registers are read-only.

Reg (HEX)	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)
60	Negative INT enable	OVLN	CLPN	TMXN	TPXN	ADCN	X	ION9	ION8	ION7	ION6	ION5	ION4	ION3	ION2	ION1	ION0	0000
62	INT clear/status	OVLS	CLPS	TMXS	TPXS	ADCS	X	IOS9	IOS8	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0	0000
64	Touch Screen control	X	X	MX	PX	BIAS	HYSD	TM1	TM0	PYG	MYG	PXG	MXG	PYP	MYP	PXP	MXP	0000
66	ADC control	AE	X	X	X	X	X	X	X	AS	X	EXVEN	AI2	AI1	AI0	VREFB	ASE	0000
68	ADC data	ADV	X	X	X	X	X	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0000
6A	Feature CSR1	X	BB3	BB2	BB1	BB0	TR1	TR0	M1	M0	HPEN	DE	DC	HIPS	GIEN	X	OVFL	0000
6C	Feature CSR2	SMT	SUEV 1	SUEV 0	AVE	AVEN 1	AVEN 0	X	X	X	X	SLP1	SLP0	X	EV2	EV1	EV0	0000
6E	Test Control	X	X	X	X	X	X	X	X	X	TM6	TM5	TM4	TM3	TM2	TM1	TM0	XXXX
70	Extra Interrupt	CLPL	CLPR	CLPG	X	X	X	X	X	X	X	X	X	X	X	X	X	0000
7A	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7C	Vendor ID1	0	1	0	1	0	0	0	0	0	1	0	1	0	0	1	1	5053
7E	Vendor ID2	0	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0	4304

12.1 Reset register (index 0x00)

Table 11: Reset register

Register address: 0x00; default: 02A0

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	X	X	X	X	ID9	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	ID7	X	ID5	X	X	X	X	X

Table 12: Description of Reset register bits

Bit	Symbol	Type	Description
D15 - D10	X	R	Reserved.
D9	ID9	R	Always ‘1’ (20-bit ADC resolution supported).
D8	X	R	Reserved.
D7	ID7	R	Always ‘1’ (20-bit DAC resolution supported).
D6	X	R	Reserved.
D5	ID5	R	Always ‘1’ (Loudness (bass boost) supported).
D4 - D0	X	R	Reserved.

Writing any value to this register performs a register reset, which causes all registers to revert to their default values.

12.2 Master Volume register (index 0x02)

Table 13: Master Volume register

Register address: 0x02; default: 8000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	MM	X	ML5	ML4	ML3	ML2	ML1	ML0
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	X	MR5	MR4	MR3	MR2	MR1	MR0

Table 14: Description of Master Volume register bits

Bit	Symbol	Type	Description
D15	MM	RW	Master mute.
D14	X	R	Reserved.
D13 - D8	ML5 - ML0	RW	Left channel attenuation in 1.5 dB step (000000 = 0 dB; 111111 = –94.5 dB).
D7 - D6	X	R	Reserved.
D5 - D0	MR5 - MR0	RW	Right channel attenuation in 1.5 dB step (000000 = 0 dB; 111111 = –94.5 dB).

12.3 MIC Volume register (index 0x0E)

Table 15: MIC Volume register

Register address: 0x0E; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	X	X	X	X	X	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	20dB	X	X	X	X	X	X

Table 16: Description of MIC Volume register bits

Bit	Symbol	Type	Description
D15 - D7	X	R	Reserved.
D6	20dB	RW	20 dB boost.
D5 - D0	X	R	Reserved.

12.4 Record Select register (index 0x1A)

Table 17: Record Select register

Register address: 0x1A; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	X	X	X	SL2	SL1	SL0
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	X	X	X	X	SR2	SR1	SR0

Table 18: Description of Record Select register bits

Bit	Symbol	Type	Description
D15 - D11	X	R	Reserved.
D10 - D8	SL2 - SL0	RW	Left record source (000 = MIC; 100 = Line In L; other values reserved).
D7 - D3	X	R	Reserved.
D2 - D0	SR2 - SR0	RW	Right record source (000 = Copy Left; 100 = Line In R; other values reserved). When SR = 000, the right record channel copies data from left record channel to create mono data and gain and sample rate control can only be made via the left channel. This mode is primarily intended when the mono MIC input is selected at the left channel (SL = 000).

12.5 Record Gain register (index 0x1C)

Table 19: Record Gain register

Register address: 0x1C; default: 8000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	RM	X	X	X	GL3	GL2	GL1	GL0
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	X	X	X	GR3	GR2	GR1	GR0

Table 20: Description of Master Volume register bits

Bit	Symbol	Type	Description
D15	RM	RW	Master Record mute.
D14 - D12	X	R	Reserved.
D11 - D8	GL3 - GL0	RW	Left channel record gain in steps of 1.5 dB (0000 = 0 dB; 1111 = 22.5 dB).
D7 - D4	X	R	Reserved.
D3 - D0	GR3 - GR0	RW	Right channel record gain in steps of 1.5 dB (0000 = 0 dB; 1111 = 22.5 dB).

12.6 General Purpose register (index 0x20)

Table 21: General Purpose register

Register address: 0x20; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	X	X	X	X	X	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	LPBK	X	X	X	X	X	X	X

Table 22: Description of General Purpose register bits

Bit	Symbol	Type	Description
D15 - D8	X	R	Reserved.
D7	LPBK	RW	ADC/DAC loopback mode (ADC output to DAC input).
D6 - D0	X	R	Reserved.

The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements.

12.7 Power-down Control/Status register (index 0x26)

Table 23: Power-down Control/Status register

Register address: 0x26; default: 000X

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	PR5	PR4	PR3	X	PR1	PR0
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	X	X	X	REF	X	DAC	ADC

Table 24: Description of Power-down Control/Status register bits

Bit	Symbol	Type	Description
D15 - D14	X	R	Reserved.
D13	PR5	RW	Internal clock disable.
D12	PR4	RW	Digital interface (AC-link) power-down (external clock off).
D11	PR3	RW	Audio V_{REF} power-down.
D10	X	R	Reserved.
D9	PR1	RW	Audio DAC and output path power-down.
D8	PR0	RW	Audio ADC and input path power-down.
D7 - D4	X	R	Reserved.
D3	REF	R	Audio V_{REF} up to nominal level.
D2	X	R	Reserved.
D1	DAC	R	Audio DAC section ready to accept data.
D0	ADC	R	Audio ADC section ready to transmit data.

This read/write register is used to program power-down states and monitor subsystem readiness. The lower half of this register is read only status, a ‘1’ indicating that the subsection is ‘ready’. ‘Ready’ is defined as the subsection able to perform in its nominal state. When this register is written, the bit values that come in on AC-link will have no effect on read-only bits 0 - 7.

When the ‘Codec Ready’ indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the UCB1400 control and status registers are in a fully operational state. The AC ’97 Controller must further probe this Power-down Control/Status register to determine exactly which subsections, if any, are ready.

12.8 Extended Audio ID register (index 0x28)

Table 25: Extended Audio ID register

Register address: 0x28; default: 0001

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	ID1	ID0	X	X	X	X	X	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	X	X	X	X	X	X	VRA

Table 26: Description of Extended Audio ID register bits

Bit	Symbol	Type	Description
D15 - D14	ID1 - ID0	R	Always ‘0’ (UCB1400 is a primary codec).
D13 - D1	X	R	Reserved.
D0	VRA	R	Always ‘1’ (Variable Rate PCM Audio supported).

The Extended Audio ID is a read-only register that identifies which extended audio features are supported (in addition to the original AC ’97 features identified by reading the Reset register at Index 0x00).

12.9 Extended Audio Status and Control register (index 0x2A)

Table 27: Extended Audio Status and Control register

Register address: 0x2A; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	X	X	X	X	X	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	X	X	X	X	X	X	VRA

Table 28: Description of Extended Audio Status and Control register bits

Bit	Symbol	Type	Description
D15 - D1	X	R	Reserved.
D0	VRA	RW	1 enables Variable Rate Audio mode (sample rate control registers and SLOTREQ signalling).

12.10 Audio Sample Rate Control register (index 0x2C and 0x32)

Table 29: Audio DAC Sample Rate Control register

Register address: 0x2C; default: BB80

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	DR15	DR14	DR13	DR12	DR11	DR10	DR9	DR8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

Table 30: Audio ADC Sample Rate Control register

Register address: 0x32; default: BB80

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

The sample rate control registers contain 16-bit unsigned values between 0 and 65535, representing the rate of operation in Hz. Table 31 shows the sample rates supported by UCB1400.

In VRA mode (VRA = 1 in register 0x2A), if the value written to the register is supported, that value will be echoed back when read, otherwise the closest (higher in case of a tie) sample rate supported is returned. The UCB1400's DAC and ADC are capable of operating at independent rates.

In non-VRA mode (VRA = 0 in register 0x2A), the only supported sample rate is 48 kHz.

Table 31: Supported sample rates

Sample rate (MHz)	D15 - D0
8000	1F40
11025	2B11
12000	2EE0
16000	3E80
22050	5622
24000	5DC0
32000	7D00
44100	AC44
48000	BB80

12.11 IO Data register (index 0x5A)

Table 32: IO Data register

Register address: 0x5A; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	X	X	X	X	IO9	IO8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

Table 33: Description of IO Data register bits

Bit	Symbol	Type	Description
D15 - D10	X	R	Reserved.
D9 - D0	IO9 - IO0	RW	When read, this register returns the actual state of all IO pins. When written, each register bit will be transferred to the corresponding IO pin programmed as output.

12.12 IO Direction register (index 0x5C)

Table 34: IO Direction register

Register address: 0x5C; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	X	X	X	X	IOD9	IOD8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	IOD7	IOD6	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0

Table 35: Description of IO Direction register bits

Bit	Symbol	Type	Description
D15 - D10	X	R	Reserved.
D9 - D0	IOD9 - IOD0	RW	If a bit is ‘1’, the associated IO pin is defined as output. If a bit is ‘0’, the associated IO pin is defined as input.

12.13 Positive INT Enable register (index 0x5E)

Table 36: Positive INT Enable register

Register address: 0x5E; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	OVLP	CLPP	TMXP	TPXP	ADCP	X	IOP9	IOP8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	IOP7	IOP6	IOP5	IOP4	IOP3	IOP2	IOP1	IOP0

Table 37: Description of Positive INT Enable register bits

Bit	Symbol	Type	Description
D15	OVLP	RW	If ‘1’, the rising edge interrupt of the OVFL signal is enabled.
D14	CLPP	RW	If ‘1’, the rising edge interrupt of the CLIP signal is enabled.
D13	TMXP	RW	If ‘1’, the rising edge interrupt of the TSMX signal is enabled.
D12	TPXP	RW	If ‘1’, the rising edge interrupt of the TSPX signal is enabled.
D11	ADCP	RW	If ‘1’, the rising edge interrupt of ADC Ready is enabled.
D10	X	R	Reserved.
D9 - D0	IOP9 - IOP0	RW	If a bit is ‘1’, the rising edge interrupt of the associated IO pin is enabled.

12.14 Negative INT Enable register (index 0x60)

Table 38: Negative INT Enable register

Register address: 0x60; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	OVLN	CLPN	TMXN	TPXN	ADCN	X	ION9	ION8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	ION7	ION6	ION5	ION4	ION3	ION2	ION1	ION0

Table 39: Description of Negative INT Enable register bits

Bit	Symbol	Type	Description
D15	OVLN	RW	If ‘1’, the falling edge interrupt of the OVFL signal is enabled.
D14	CLPN	RW	If ‘1’, the falling edge interrupt of the CLIP signal is enabled.
D13	TMXN	RW	If ‘1’, the falling edge interrupt of the TSMX signal is enabled.
D12	TPXN	RW	If ‘1’, the falling edge interrupt of the TSPX signal is enabled.
D11	ADCN	RW	If ‘1’, the falling edge interrupt of ADC Ready is enabled.
D10	X	R	Reserved.
D9 - D0	ION9 - ION0	RW	If a bit is ‘1’, the falling edge interrupt of the associated IO pin is enabled.

12.15 INT Clear/Status register (index 0x62)

Table 40: INT Clear/Status register

Register address: 0x62; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	OVLS	CLPS	TMXS	TPXS	ADCS	X	IOS9	IOS8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0

Table 41: Description of INT Clear/Status register bits

Bit	Symbol	Type	Description
D15	OVLS	RW	When read, returns the OVFL interrupt status. Cleared by writing ‘1’ to this bit.
D14	CLPS	RW	When read, returns the CLIP interrupt status. Cleared by writing ‘1’ to this bit.
D13	TMXS	RW	When read, returns the TSMX interrupt status. Cleared by writing ‘1’ to this bit.
D12	TPXS	RW	When read, returns the TSPX interrupt status. Cleared by writing ‘1’ to this bit.
D11	ADCS	RW	When read, returns the ADC Ready interrupt status. Cleared by writing ‘1’ to this bit.
D10	X	R	Reserved.
D9 - D0	IOS9 - IOS0	RW	When read, returns all IO pin interrupt status. The interrupt status of a pin is cleared by writing ‘1’ to the corresponding bit.

12.16 Touch Screen Control register (index 0x64)

Table 42: Touch Screen Control register

Register address: 0x64; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	MX	PX	BIAS	HYSD	TM1	TM0
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	PYG	MYG	PXG	MXG	PYP	MYP	PXP	MXP

Table 43: Description of Touch Screen Control register bits

Bit	Symbol	Type	Description
D15 - D14	X	R	Reserved.
D13	MX	R	State of the TSMX pin. 0 = low voltage (pen down) 1 = high voltage (pen up)
D12	PX	R	State of the TSPX pin. 0 = low voltage (pen down) 1 = high voltage (pen up)
D11	BIAS	RW	If ‘1’, the touch screen bias circuitry is activated. If ‘0’, the touch screen bias is disabled to minimize power consumption.

Table 43: Description of Touch Screen Control register bits…*continued*

Bit	Symbol	Type	Description
D10	HYSD	RW	If ‘1’, hysteresis is deactivated on the Schmitt triggers.
D9 - D8	TM1 - TM0	RW	Touch screen operation mode 00 = interrupt mode 01 = pressure measurement mode 1x = position measurement mode
D7	PYG	RW	If ‘1’, the TSPY pin is grounded.
D6	MYG	RW	If ‘1’, the TSMY pin is grounded.
D5	PXG	RW	If ‘1’, the TSPX pin is grounded.
D4	MXG	RW	If ‘1’, the TSMX pin is grounded.
D3	PYP	RW	If ‘1’, the TSPY pin is powered.
D2	MYP	RW	If ‘1’, the TSMY pin is powered.
D1	PXP	RW	If ‘1’, the TSPX pin is powered.
D0	MXP	RW	If ‘1’, the TSMX pin is powered.

12.17 ADC Control register (index 0x66)

Table 44: ADC Control register

Register address: 0x66; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	AE	X	X	X	X	X	X	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	AS	X	EXVEN	AI2	AI1	AI0	VREFB	ASE

Table 45: Description of ADC Control register bits

Bit	Symbol	Type	Description
D15	AE	RW	If ‘1’, ADC is activated. If ‘0’, ADC is powered-down.
D14 - D8	X	R	Reserved.
D7	AS	RW	Writing ‘1’ starts the ADC conversion sequence. This bit self-clears.
D6	X	R	Reserved.
D5	EXVEN	R/W	Must be set to ‘0’ (other values reserved for testing purposes only).
D4 - D2	AI2 - AI0	RW	ADC input selection: 000 = TSPX 001 = TSMX 010 = TSPY 011 = TSMY 100 = AD0 101 = AD1 110 = AD2 111 = AD3

Table 45: Description of ADC Control register bits...*continued*

Bit	Symbol	Type	Description
D1	VREFB	R/W	VREF bypass. If '1', the internal reference voltage is connected to VREFBYP pin.
D0	ASE	RW	If '1', ADC is armed by the AS bit and started by a rising edge on the ADCSYNC pin. If '0', ADC is started by the AS bit.

12.18 ADC Data register (index 0x68)

Table 46: ADC Data register

Register address: 0x68; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	ADV	X	X	X	X	X	AD9	AD8
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 47: Description of ADC Data register bits

Bit	Symbol	Type	Description
D15	ADV	R	'0' if ADC conversion is in progress. '1' if the ADC conversion is completed and the ADC data is stored in AD9 - AD0.
D14 - D10	X	R	Reserved.
D9 - D0	AD9 - AD0	R	ADC data.

12.19 Feature Control/Status Register 1 (index 0x6A)

Table 48: Feature Control/Status Register 1

Register address: 0x6A; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	BB3	BB2	BB1	BB0	TR1	TR0	M1
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	M0	X	DE	DC	HIPS	GIEN	X	OVFL

Table 49: Description of Feature Control/Status Register 1 bits

Bit	Symbol	Type	Description
D15	X	R	Reserved.
D14 - D11	BB3 - BB0	RW	Bass boost

BB	M = Flat (dB)	M = Min. (dB)	M = Max. (dB)
0-9	0	2*BB	2*BB
10-12	0	18	2*BB
13-15	0	18	24

D10 - D9	TR1 - TR0	RW	Treble boost

TR	M = Flat (dB)	M = Min. (dB)	M = Max. (dB)
0-3	0	2*TR	2*TR

D8 - D7	M1 - M0	RW	Mode 00 = flat 01 = minimum 10 = minimum 11 = maximum
D6	HPEN	RW	If ‘1’, headphone driver is enabled.
D5	DE	RW	If ‘1’, de-emphasis is enabled when the sample rate is 48, 44.1 or 32 kHz.
D4	DC	RW	If ‘1’, DC filter is enabled.
D3	HIPS	R	If ‘1’, activate high-pass filter in the decimator.
D2	GIEN	RW	If ‘1’, the following interrupt/wake-up signalling is enabled: • Interrupt signalling via GPIO_INT (input slot 12) when BIT_CLK is on. • Wake-up signalling via SDATA_IN when BIT_CLK is off.
D1	X	R	Reserved.
D0	OVFL	RW	When read, returns ADC overflow status (set status is sticky until cleared). When written, clears ADC overflow status.

12.20 Feature Control/Status Register 2 (index 0x6C)

Table 50: Feature Control/Status Register 2

Register address: 0x6C; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	SMT	SUEV1	SUEV0	AVE	AVEN1	AVEN0	X	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	X	SLP1	SLP0	X	EV2	EV1	EV0

Table 51: Description of Feature Control/Status Register 2 bits

Bit	Symbol	Type	Description
D15	SMT	RW	Must be set to ‘0’ (other values reserved for testing purposes only).
D14 - D13	SUEV1 - SUEV0	RW	Must be set to ‘0’ (other values reserved for testing purposes only).
D12	AVE	RW	If ‘1’, ADC Filter is enabled.
D11 - D10	AVEN1 - AVEN0	RW	Must be set to ‘0’ (other values reserved for testing purposes only).
D5 - D4	SLP1 - SLP0	RW	• 0: no Smart Low Power Mode. On normal mode operation, all Codec input blocks and PLL are ON. • 1: Smart Low Power Mode on the Codec **only**. On normal mode operation, only used input stage(s) is/are ON. PLL remains ON all the time. • 2: Smart Low Power Mode on the PLL **only**. On normal mode operation, PLL is ON **only** when a sample rate equal to 11.025, 22.05, or 44.1 kHz is selected and the corresponding audio ADC or DAC is not in power-down mode. Codec input blocks are always ON. • 3: Smart Low Power Mode on both Codec and PLL.
D2 - D0	EV2 - EV0	RW	Must be set to ‘0’ (other values reserved for testing purposes only).

12.21 Test Control register (index 0x6E)

Table 52: Test Control register

Register address: 0x6E; default: XXXX

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	X	X	X	X	X	X	X	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	TM6	TM5	TM4	TM3	TM2	TM1	TM0

Table 53: Description of Test Control register bits

Bit	Symbol	Type	Description
D15 - D7	X	R	Reserved.
D6 - D0	TM6 - TM0	RW	Test mode. Reserved for testing purposes only.

This register cannot be reset and is not scan testable. It has no effect until the UCB1400 is put in Vendor-Specific Test Mode (refer to Section 8.7.2).

12.22 Extra Interrupt register (index 0x70)

Table 54: Extra Interrupt register

Register address: 0x70; default: 0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	CLPL	CLPR	CLPG	X	X	X	X	X
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	X	X	X	X	X	X	X	X

Table 55: Description of ADC Data register bits

Bit	Symbol	Type	Description
D15	CLPL	RW	Status of the CLIPL (LINE_OUT_L short circuit) signal; write ‘1’ to clear.
D14	CLPR	RW	Status of the CLIPR (LINE_OUT_R short circuit) signal; write ‘1’ to clear.
D13	CLPG	RW	Status of the CLIPGND (VREFDRV short circuit) signal; write ‘1’ to clear.
D12 - D0	X	R	Reserved.

12.23 Vendor ID1 and ID2 registers (index 0x7C and 0x7E)

Table 56: Vendor ID1 register

Register address: 0x7C; default: 5053

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	0	1	0	1	0	0	0	0
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	0	1	0	1	0	0	1	1

Table 57: Vendor ID2 register

Register address: 0x7E; default: 4304

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Symbol	0	1	0	0	0	0	1	1
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Symbol	0	0	0	0	0	1	0	0

13. Limiting values

Table 58: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4	V
T_{stg}	Storage temperature		–65	+125	°C
T_{amb}	Operating ambient temperature		–40	+85	°C
V_{es}	Electrostatic handling voltage	Equivalent to discharging a 100 pF capacitor via 1.5 kΩ series resistor	–1500	+1500	V

14. Static characteristics

Table 59: Static characteristics

$DV_{DD} = AV_{DD} = V_{ADCP} = 3.3$ V; $T_{amb} = 25$ °C; all voltage measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
AV_{DD}	Analog supply voltage		3.0	3.3	3.6	V
DV_{DD}	Digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	Digital supply current	Full audio, Line-in selected	–	18	–	mA
		Audio ADC only, Line-in selected	–	12	–	mA
		Audio DAC and headphone driver only	–	13	–	mA
		AC-link only	–	7	–	mA
		Standby	–	1	–	µA
I_{DDA}	Analog supply current	Full audio, Line-in selected	–	12	–	mA
		Audio ADC only, Line-in selected	–	8	–	mA
		Audio DAC and headphone driver only	–	4.5	–	mA
		Touch screen bias only	–	0.9	–	mA
		10-bit ADC only	–	1.8	–	mA
		Standby	–	3	–	µA
Digital input pins (5 V tolerant, TTL compatible)						
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
V_{IL}	LOW-level input voltage		–0.5	–	0.8	V
$\|I_{IL}\|$	Input leakage current		–	–	1	µA
C_i	Input capacitance		–	–	10	pF
Digital output pins						
V_{OH}	HIGH-level output voltage	$I_{OH} = –2$ mA	0.85 DV_{DD}	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V

15. Dynamic characteristics

Table 60: Dynamic characteristics

DV_{DD} = AV_{DD} = V_{ADCP} = 3.3 V; T_{amb} = 25 °C; all voltage measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Audio ADC						
V_{ADCP}	Positive reference voltage		–	AV_{DD}	–	V
V_{ADCN}	Negative reference voltage		–	0.0	–	V
R_{IL}	Line input resistance		–	10	–	kΩ
C_{IL}	Line input capacitance		–	24	–	pF
R_{IM}	MIC input resistance		–	10	–	kΩ
C_{IM}	MIC input capacitance		–	24	–	pF
Z_{MICGND}	Impedance MICGND - V_{SSA}		–	–	200	Ω
$V_{i(rms)}$	FS input voltage (rms value)	Record Gain = 0 dB				
	Line inputs		–	1.0	–	V
	MIC input	20 dB = 0	–	1.0	–	V
		20 dB = 1	–	0.1	–	V
ΔV_i	Unbalance between channels		–	0.1	–	dB
$\frac{(THD+N)}{S}$	Total harmonic distortion plus noise-to-signal ratio; f_s = 48 kHz, Line-in selected	At –3 dB input	–	–87	–	dB
		At –60 dB input; A-weighted	–	–37	–	dB
S/N	Signal-to-noise ratio; f_s = 48 kHz, Line-in selected	At zero input; A-weighted	–	97	–	dB
α_{CS}	Channel separation; f_s = 48 kHz, Line-in selected	At 0 dB input	–	95	–	dB
PSRR	Power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 30 $mV_{(p-p)}$	–	30	–	dB
Audio DAC + headphone driver						
R_L	Load resistance		16	32	–	Ω
C_L	Load capacitance		–	–	30	pF
$V_{VREFDRV}$	VREFDRV voltage		–	$AV_{DD}/2$	–	V
$V_{o(rms)}$	Output voltage (rms value)	At 0 dB (FS) digital input R_L = 10 kΩ	–	1.0	–	V
P_o	Output power	At 0 dB (FS) digital input R_L = 32 Ω	–	25	–	mW
ΔV_o	Unbalance between channels	At 0 dB (FS) digital input R_L = 10 kΩ	–	<0.1	–	dB
$\frac{(THD+N)}{S}$	Total harmonic distortion plus noise-to-signal ratio; f_s = 48 kHz	At 0 dB digital input, R_L = 32 Ω	–	–40	–	dB
		At 0 dB digital input, R_L = 10 kΩ	–	–80	–	dB
		At –60 dB digital input; A-weighted	–	–32	–	dB
S/N	Signal-to-noise ratio	Code = 0; A-weighted	–	91	–	dB
α_{CS}	Channel separation	R_L = 32 Ω	–	54	–	dB
PSRR	Power supply rejection ratio	R_L = 10 kΩ; f_{ripple} = 1 kHz; V_{ripple} = 30 $mV_{(p-p)}$	–	58	–	dB

Table 60: Dynamic characteristics *…continued*

DV_{DD} = AV_{DD} = V_{ADCP} = 3.3 V; T_{amb} = 25 °C; all voltage measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Touch screen						
$V_{i(bias)}$	Bias voltage	Position mode selected; no loading	–	1.89	–	V
I	Max. touch screen current	Position mode selected	10	–	–	mA
R_i	Max. touch screen resistance to generate an interrupt	Interrupt mode selected	–	–	2500	Ω
R_{gs}	Ground switch on resistance		–	–	50	Ω
R_{ps}	Power switch on resistance		–	–	50	Ω
Voltage monitor ADC						
RES	Resolution		–	10	–	Bits
$V_{i(AD0-AD3)}$	Full scale AD0-AD3 inputs		-	7.5	-	V
Z_i	Input impedance		-	77	-	kΩ
I_{LI}	Input leakage current	V_{AD0} = V_{AD1} = V_{AD2} = V_{AD3} = 7.5 V	–	–	10	µA
LE_d	Differential linearity error		–	±1	–	LSB
LE_i	Integral linearity error		–	±2	–	LSB
t_{en}	ADC enable time					
$t_{d(s)}$	Sampling delay	Non-synchronization mode (AS = 0, AVE = 0)	21 T_{clk_period}	–	–	
		Synchronization mode; rising edge ADCSYNC to sample moment (AS = 1, AVE = 0)	1 T_{clk_period}	–	3 T_{clk_period}	
t_{conv}	Total conversion time	AS = AVE = 0	–	10	–	µs
t_{track}	Tracking time		–	2	–	µs
$t_{adcsync}$	HIGH time ADSYNC signal		81.4			ns
Oscillator						
f_{osc}	Oscillator frequency		–	24.576	–	MHz

16. AC Link characteristics

Table 61: Characteristics

DV_{DD} = AV_{DD} = V_{ADCP} = 3.3 V; T_{amb} = 25 °C; all voltage measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Cold/warm reset						
T_{rst_low}	$\overline{RESET}$ active-LOW pulse width (AC Link controller)		1.0	-	-	µs
$T_{rst2clk}$	$\overline{RESET}$ inactive to BIT_CLK start-up delay		162.8			ns
T_{sync_high}	SYNC active-HIGH pulse width (AC Link controller)		1.0	-	-	µs
$T_{sync2clk}$	SYNC inactive to BIT_CLK start-up delay		162.8	-	-	ns
AC-link clocks						
	BIT_CLK frequency		-	12.288	-	MHz
T_{clk_period}	BIT_CLK period		-	81.4	-	ns
	BIT_CLK output jitter		-	-	750	ps
T_{clk_high}	BIT_CLK HIGH pulse width		36	40.7	45	ns
T_{clk_low}	BIT_CLK LOW pulse width		36	40.7	45	ns
	SYNC frequency		-	48.0	-	kHz
T_{sync_period}	SYNC period		-	20.8	-	µs
T_{sync_high}	SYNC HIGH pulse width		-	1.3	-	µs
T_{sync_low}	SYNC LOW pulse width		-	19.5	-	µs
Data setup and hold						
t_{co}	Output delay from rising edge of BIT_CLK		-	-	15	ns
T_{setup}	Input setup to falling edge of BIT_CLK		10	-	-	ns
T_{hold}	Input hold from falling edge of BIT_CLK		10	-	-	ns
$Trise_{clk}$	BIT_CLK rise time		-	-	10	ns
$Tfall_{clk}$	BIT_CLK fall time		-	-	10	ns
$Trise_{sync}$	SYNC rise time		-	-	6	ns
$Tfall_{sync}$	SYNC fall time		-	-	6	ns
$Trise_{din}$	SDATA_IN rise time		-	-	10	ns
$Tfall_{din}$	SDATA_IN fall time		-	-	10	ns
$Trise_{dout}$	SDATA_OUT rise time		-	-	6	ns
$Tfall_{dout}$	SDATA_OUT fall time		-	-	6	ns
AC-link low power mode						
T_{s2_pdown}	End of Slot 2 to BIT_CLK, SDATA_IN LOW		-	0.65	-	µs
ATE test mode						
$T_{setup2rst}$	Setup to trailing edge of $\overline{RESET}$ (AC Link controller)		15	-	-	ns
T_{off}	Rising edge of $\overline{RESET}$ to Hi-Z delay		-	-	25	ns

17. Timing diagrams

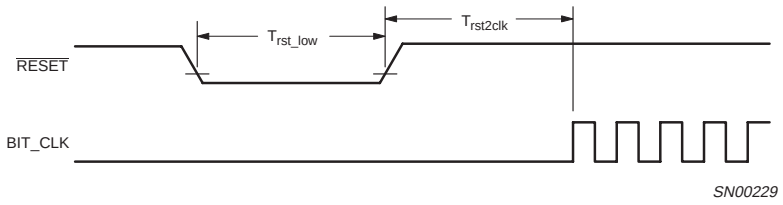


Fig 24. Cold reset timing.

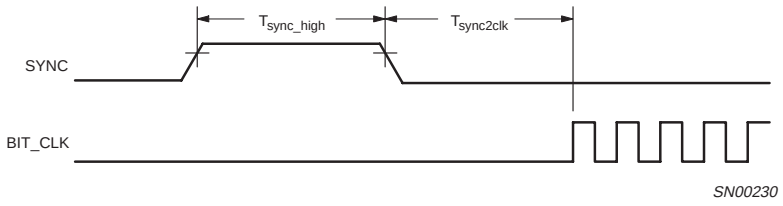


Fig 25. Warm reset timing.

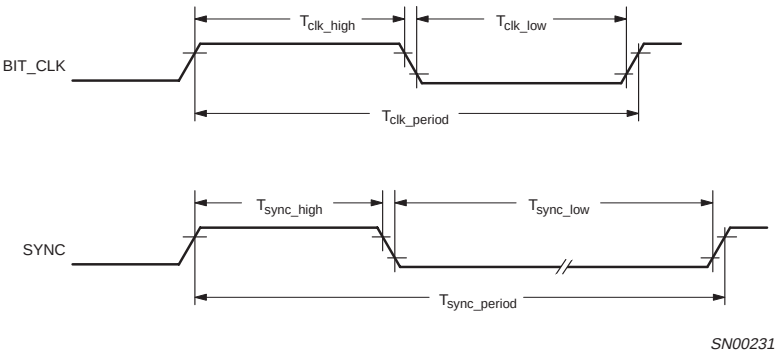


Fig 26. BIT_CLK and SYNC timing.

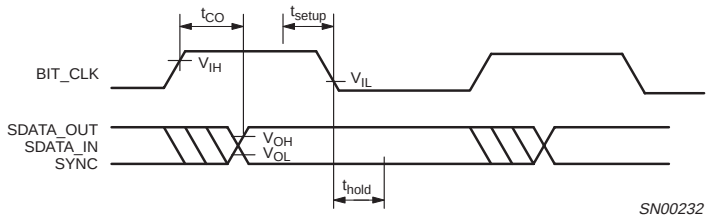


Fig 27. Data output and input timing.

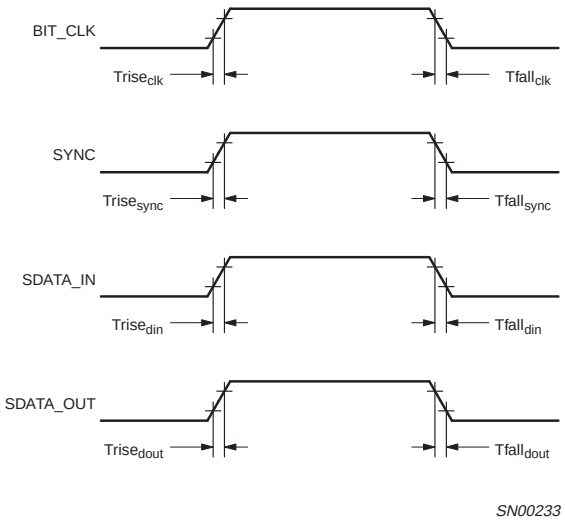
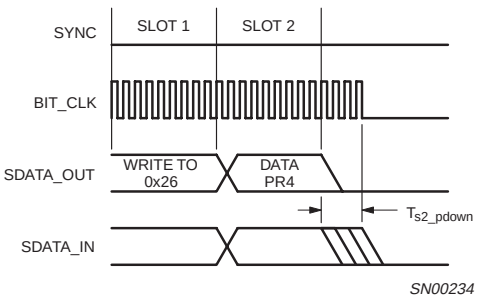


Fig 28. Data rise and fall timing.



BIT_CLK not to scale.

Fig 29. AC Link low power timing.

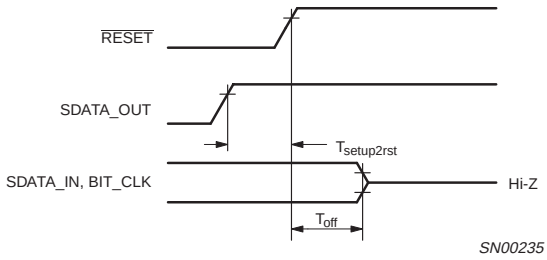


Fig 30. ATE test mode timing.

18. Application information

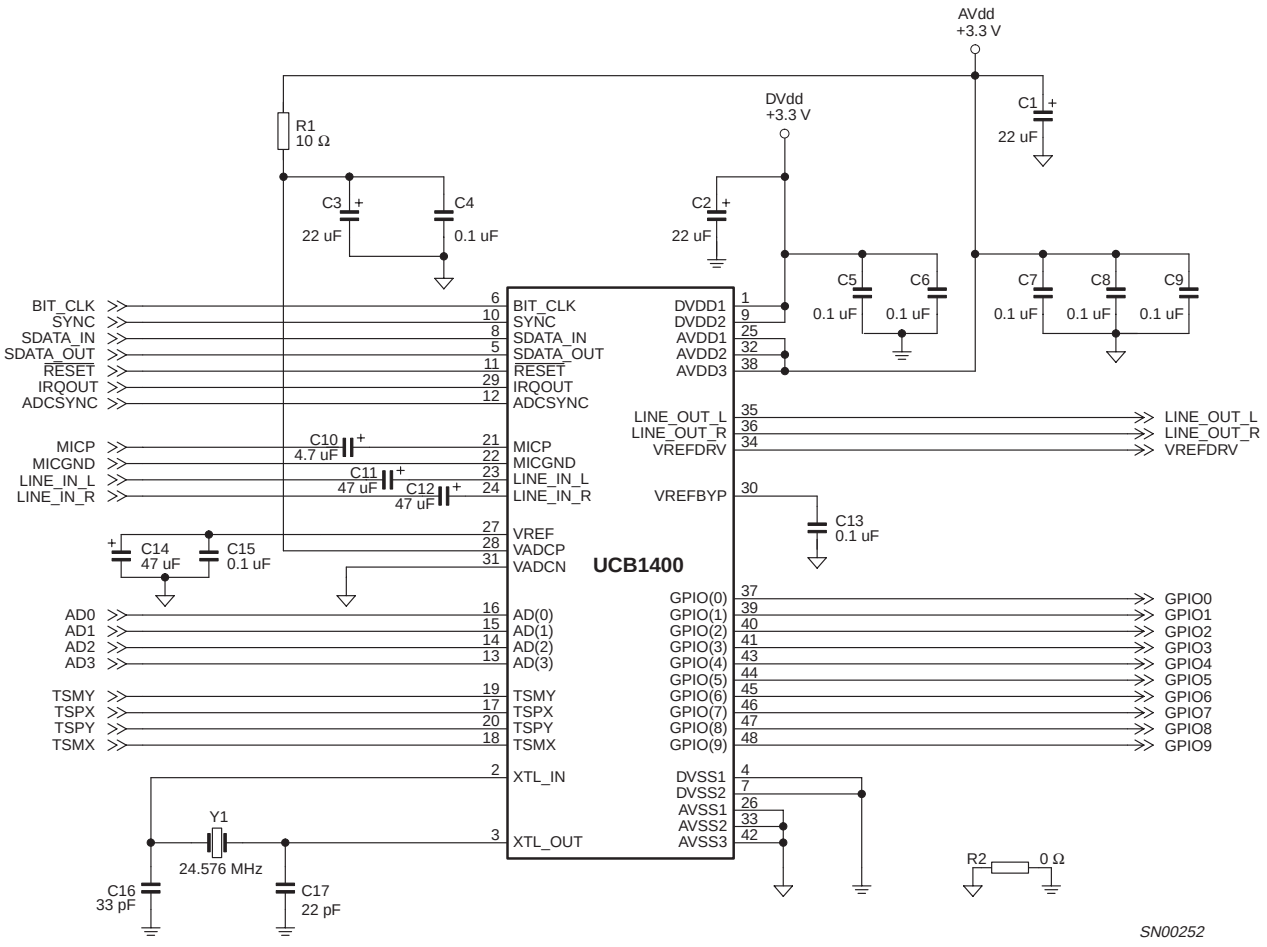


Fig 31. Typical application circuit.

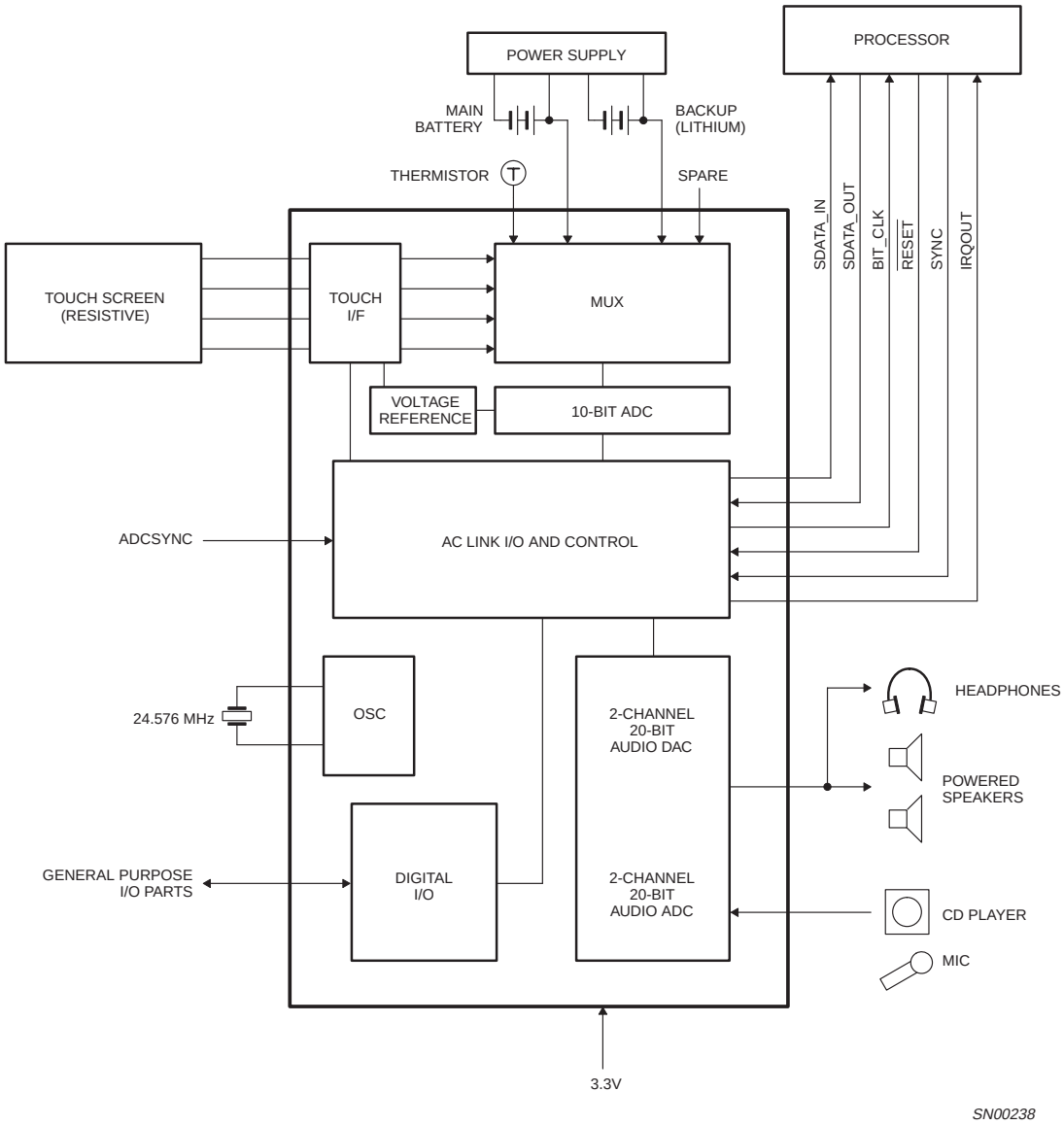
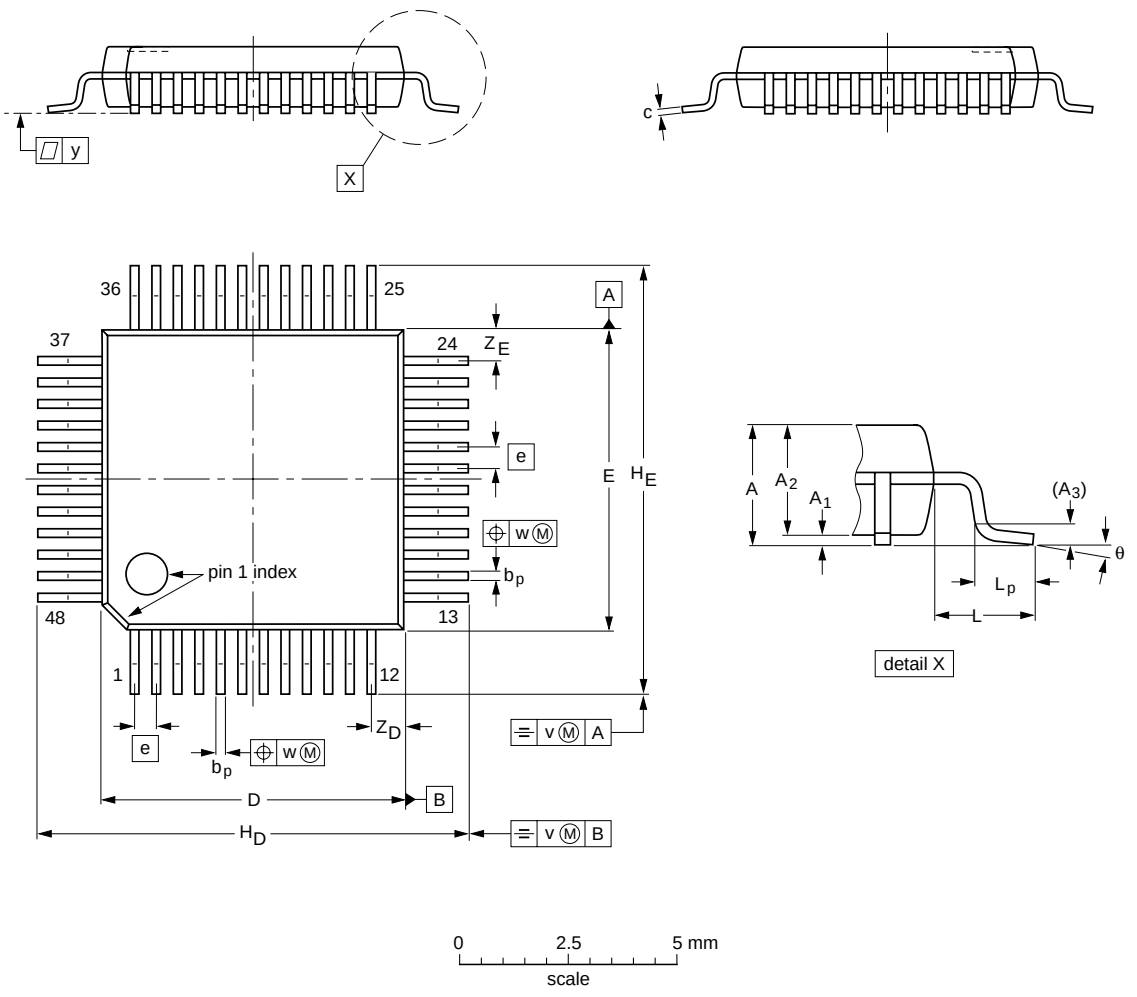


Fig 32. Application block diagram.

19. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

Fig 33. LQFP48 (SOT313-2).

20. Soldering

20.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

20.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

20.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

20.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

20.5 Package related soldering information

Table 62: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

21. Revision history

Table 63: Revision history

Rev	Date	CPCN	Description
02	20020621	-	**Product data; second version; Engineering Change Notice 853-2358 28518; supersedes initial version UCB1400-01 of 03 Jan 2002 (9397 750 09242). Modifications:** • Section 2 “Features” modified. • Section 9.2.4 “Headphone driver” modified. • Section 9.5 “Power-down modes” modified. • Section 13 “Limiting values” modified: added V_{es} parameter. • Section 14 “Static characteristics” modified. • Section 15 “Dynamic characteristics” modified. • Section 16 “AC Link characteristics” modified.
01	20020103	-	**Objective data; initial version.**

22. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

23. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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