INTERLEAVED DUAL PWM CONTROLLER WITH PROGRAMMABLE MAXIMUM DUTY CYCLE

FEATURES

- **Qualified for Automotive Applications**
- **2-MHz High-Frequency Oscillator With 1-MHz Operation Per Channel**
- **Matched Internal Slope Compensation Circuits**
- **Programmable Maximum Duty Cycle Clamp 60% to 90% Per Channel**
- **Peak Current Mode Control With Cycle-by-Cycle Current Limit**
- **Current Sense Discharge Transistor for Improved Noise Immunity**
- **Accurate Line Undervoltage and Overvoltage Sense With Programmable Hysteresis**
- **Opto-Coupler Interface**
- **Operates From 12-V Supply**
- **Programmable Soft-Start**

APPLICATIONS

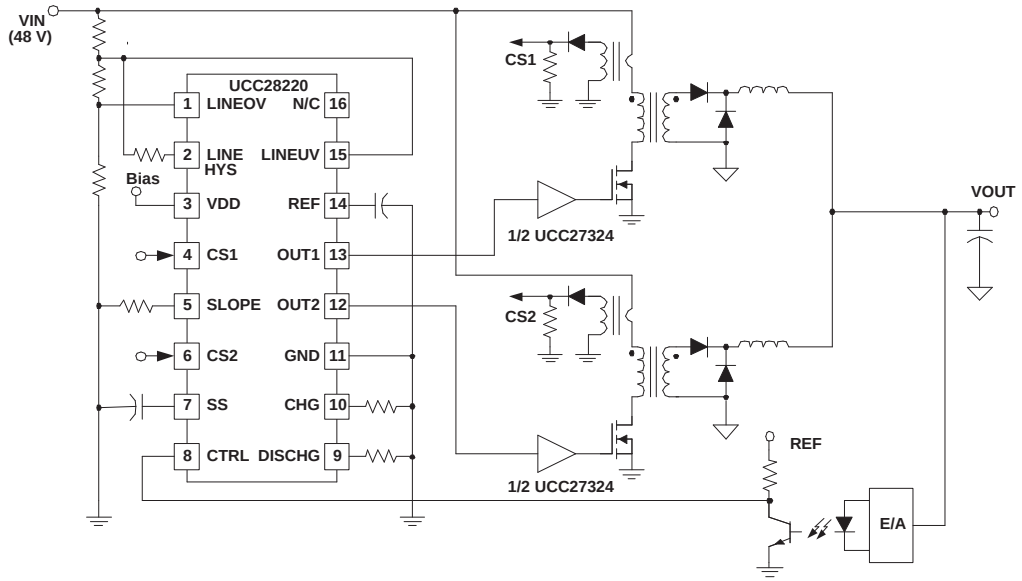
- **High Output Current (50 A to 100 A) Converters**
- **Maximum Power Density Designs**
- **High-Efficiency 48-V Input with Low-Output Ripple Converters**
- **High-Power Offline, Telecom, and Datacom Power Supplies**

DESCRIPTION

The UCC28220 is a BiCMOS interleaved dual-channel PWM controller. Peak current mode control is used to ensure current sharing between the two channels. A precise maximum duty cycle clamp can be set to any value between 60% and 90% duty cycle per channel. UCC28220 has an UVLO turn-on threshold of 10 V for use in 12-V supplies. It has 8-V turn-off threshold.

Additional features include a programmable internal slope compensation with a special circuit that ensures exactly the same slope is added to each channel. The UCC28220 is available in a 16-pin low-profile TSSOP package.

TYPICAL APPLICATION



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ORDERING INFORMATION(1)

$T_A = T_J$	UVLO THRESHOLDS	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	10 V On / 8 V Off	TSSOP-16 – PW	Reel of 2000	UCC28220QPWRQ1	U28220Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature (unless otherwise noted)

V_{DD}	Supply voltage		15 V
$I_{OUT(dc)}$	Output current, dc	OUT1, OUT2	±10 mA
	OUT1/ OUT2 capacitive load		200 pF
I_{REF}	REF output current		10 mA
	Current sense inputs	CS1, CS2	–1 V to 2 V
	Analog inputs	CHG, DISCHG, SLOPE, REF, CNTRL	–0.3 V to 3.6 V
		SS, LINEOV, LINEUV, LINEHYS	–0.3 V to 7 V
P_D	Power dissipation at T_A = 25°C		400 mW
T_J	Virtual-junction operating temperature range		–55°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
T_{lead}	Lead temperature (soldering, 10 seconds)		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	High-voltage start-up input voltage	36	76	V
V_{DD}	Supply voltage	8	14.5	V

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, 0.1-µF capacitor from VDD to GND, 0.1-µF capacitor from REF to GND, f_{OSC} = 1 MHz, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall					
Operating VDD		8.5		14	V
Quiescent current	SS = 0 V, No switching, f_{osc} = 1 MHz	1.5	3	4	mA
Operating current	Outputs switching, f_{osc} = 1 MHz	1.6	3.5	6	
Startup Section					
Startup current	VDD < (UVLO – 0.8)			200	µA
UVLO start threshold		9.5	10	10.5	V
UVLO stop threshold		7.6	8	8.4	V
UVLO hysteresis		1.8	2	2.2	V
Reference					
Output voltage	8.5 V < VDD < 14 V, I_{LOAD} = 0 mA to –10 mA	3.15	3.3	3.45	V
Output current	Outputs not switching, CNTRL = 0 V	10			mA
Output short-circuit current	V_{REF} = 0 V	–40	–20	–10	mA
V_{REF} UVLO		2.55	3	3.25	V
Soft Start (SS)					
SS charge current	R_{CHG} = 10.2 kΩ, SS = 0 V	–60	–100	–130	µA
SS discharge current	R_{CHG} = 10.2 kΩ, SS = 2 V	60	100	130	µA
SS initial voltage	LINEOV = 2 V, LINEUV = 0 V	0.5	1	1.5	V
SS voltage at 0% dc	Point at which output starts switching	0.5	1.2	1.8	
SS voltage ratio		75	90	100	%
SS maximum voltage	LINEOV = 0 V, LINEUV = 2 V	3	3.5	4	V
Oscillator and PWM					
Output frequency	R_{CHG} = 10.2 kΩ, R_{DISCHG} = 10.2 kΩ	400	500	550	kHz
Oscillator frequency	R_{CHG} = 10.2 kΩ, R_{DISCHG} = 10.2 kΩ	900	1000	1100	kHz
Output maximum duty cycle	R_{CHG} = 10.2 kΩ, R_{DISCHG} = 10.2 kΩ, Measured at OUT1 and OUT2	73	75	77	%
CHG voltage		1.5	2.5	3	V
DISCHG voltage		1.5	2.5	3	
Slope Compensation					
Slope	R_{SLOPE} = 75 kΩ, R_{CHG} = 66 kΩ, R_{DISCHG} = 44 kΩ, CSx = 0 V to 0.5 V	140	200	260	mV/µs
Channel matching	R_{SLOPE} = 75 kΩ, CSx = 0 V		0	10	%
Current Sense					
CS1, CS2 bias current	CS1 = 0, CS2 = 0	–500	0	500	nA
Prop delay CSx to OUTx	CSx input 0 V to 1.5 V step		40	85	ns
CS1, CS2 sink current	CSx = 2 V	2.3	4.5	7	mA
CNTRL Section					
Resistor ratio(1)			0.6		
CTRL input current	CTRL = 0 V and 3.3 V	–100	0	100	nA
CTRL voltage at 0% dc	CSx = 0 V, Point at which output starts switching (checks resistor ratio)	0.5	1.2	1.8	V

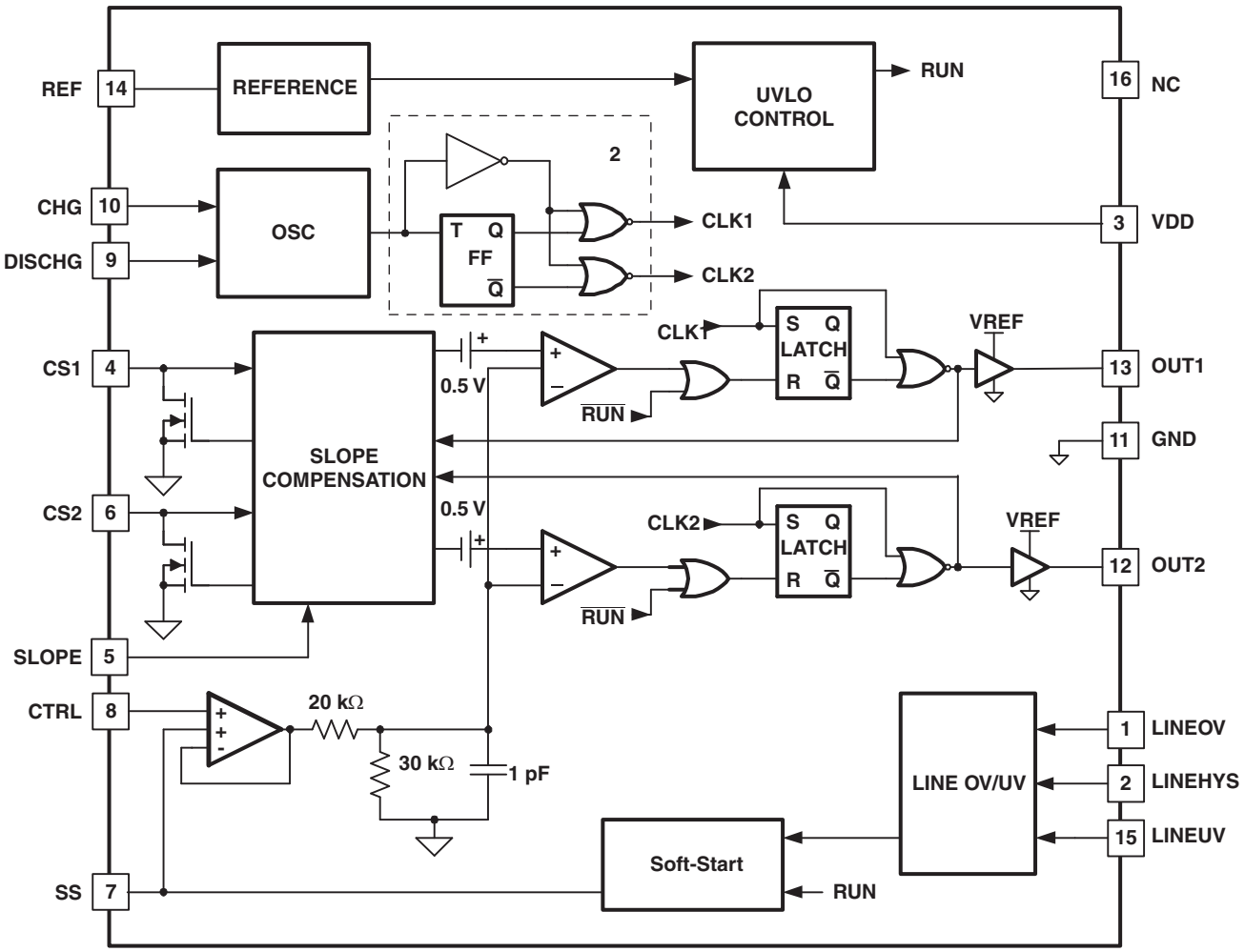
(1) Specified by design

ELECTRICAL CHARACTERISTICS (continued)

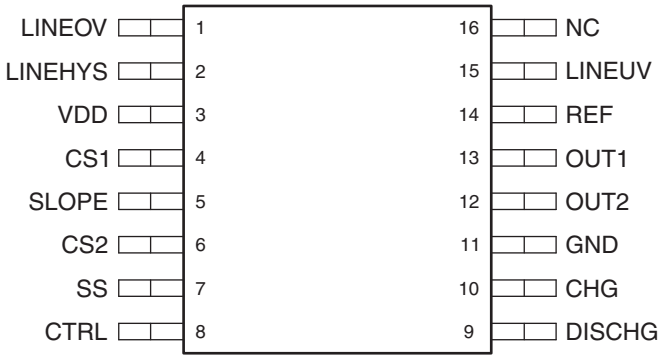
V_{DD} = 12 V, 0.1-µF capacitor from VDD to GND, 0.1-µF capacitor from REF to GND, f_{OSC} = 1 MHz, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Section (OUT1, OUT2)					
Low level	I_{OUT} = 10 mA		0.4	1	V
High level	I_{OUT} = –10 mA, V_{REF} – V_{OUT}		0.4	1	V
Rise time	C_{LOAD} = 50 pF		10	20	ns
Fall time	C_{LOAD} = 50 pF		10	20	ns
Line-Sense Section					
LINEOV threshold	T_A = 25°C	1.24	1.26	1.28	V
	T_A = –40°C to 125°C	1.23	1.26	1.29	
LINEUV threshold	T_A = 25°C	1.24	1.26	1.28	V
	T_A = –40°C to 125°C	1.23	1.26	1.29	
LINEHYST pull up voltage	LINEOV = 2 V, LINEUV = 2 V	3.1	3.25	3.4	V
LINEHYST off leakage	LINEOV = 0 V, LINEUV = 2 V	–500	0	500	nA
LINEHYS pullup resistance	I = –20 µA		100	500	Ω
LINEHYS pulldown resistance	I = 20 µA		100	500	Ω
LINEOV bias current	LINEOV = 1.25 V	–900		900	nA
LINEUV bias current	LINEUV = 1.25 V	–500		500	nA

FUNCTIONAL BLOCK DIAGRAM



PW PACKAGE
(TOP VIEW)



NC – No internal connection

TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
NO.	NAME		
1	LINEOV	I	Input for line overvoltage comparator
2	LINEHYS	I	Sets line comparator hysteresis
3	VDD	I	Device supply input
4	CS1	I	Channel 1 current sense input
5	SLOPE	I	Sets slope compensation
6	CS2	I	Channel 2 current sense input
7	SS	I	Soft-start input
8	CTRL	I	Feedback control input
9	DISCHG	I	Sets oscillator discharge current
10	CHG	I	Sets oscillator charge current
11	GND		Device ground
12	OUT2	O	PWM output from channel 2
13	OUT1	O	PWM output from channel 1
14	REF	O	Reference voltage output
15	LINEUV	I	Input for line undervoltage comparator
16	NC		No connection

TERMINAL DESCRIPTIONS

VDD: VDD supplies power to the device and is monitored by the UVLO circuit, which ensures glitch-free startup. Until VDD reaches its UVLO threshold, the device remains in low-power mode, drawing approximately 150 μA of current and forcing pins SS, CS1, CS2, OUT1, and OUT2 to logic 0 states. If VDD falls below 8 V after reaching the turn-on threshold, the device returns to the low-power state. The UVLO turn-on threshold is 10 V, and the turn-off threshold is 8 V.

CS1 and CS2: These two pins are the current-sense inputs to the device. The signals are internally level shifted by 0.5 V before the signal reaches the PWM comparator. Internally, the slope compensation ramp is added to this signal. The linear operating range on this input is 0 to 1.5 V. Also, this pin is pulled to ground each time its respective output goes low (i.e., OUT1 or OUT2).

SLOPE: This pin sets up a current used for the slope compensation ramp. A resistor to ground sets up a current, which is internally divided by 25 and applied to an internal 10-pF capacitor. Under normal operation, the dc voltage on this pin is 2.5 V.

SS: A capacitor to ground sets up the soft-start time for the open-loop soft-start function. The source and sink current from this pin is equal to 3/7 of the oscillator charge current set by the resistor on the CHG pin. The soft-start capacitor is held low during UVLO and during a line overvoltage or undervoltage condition. Once an overvoltage or undervoltage fault occurs, the soft-start capacitor is discharged by a current equal to its charging current. The capacitor does not quickly discharge during faults. In this way, the controller has the ability to recover quickly from very short line transients. This pin can also be used as an enable/disable function.

CHG: A resistor from this pin to GND sets up the charging current of the internal C_T capacitor used in the oscillator. This resistor, in conjunction with the resistor on the DISCHG pin, sets the operating frequency and maximum duty cycle. Under normal operation, the dc voltage on this pin is 2.5 V.

DISCHG: A resistor from this pin to GND sets the discharge current of the internal C_T capacitor used in the oscillator. This resistor, in conjunction with the resistor on the CHG pin, sets the operating frequency and maximum duty cycle. Under normal operation, the dc voltage on this pin is 2.5 V.

OUT1 and OUT2: These output buffers are intended to interface with high-current MOSFET drivers. The output drive capability is approximately 33 mA and has an output impedance of 100 Ω. The outputs swing between GND and REF.

LINEOV: This pin is connected to a comparator and used to monitor the line voltage for an overvoltage condition. The typical threshold is 1.26 V.

LINEUV: This pin is connected to a comparator and used to monitor the line voltage for an undervoltage condition. The typical threshold is 1.26 V.

LINEHYST: This pin is controlled by both the LINEOV and LINEUV pins. It controls the hysteresis values for both the overvoltage and undervoltage line detectors.

REF: REF is a 3.3-V output used primarily as a source for the output buffers and other internal circuits. It is protected from accidental shorts to ground. For improved noise immunity, it is recommended that the reference pin be bypassed with a minimum of 0.1-μF of capacitance to GND.

APPLICATION INFORMATION

General

The device is composed of several housekeeping blocks, as well as two slope-compensated PWM channels that are interleaved. The circuit is intended to run from an external VDD supply voltage between 8 V and 14 V. Other functions contained in the device are supply UVLO, 3.3-V reference, accurate line overvoltage and undervoltage functions, a high speed programmable oscillator for both frequency and duty cycle, programmable slope compensation, and programmable soft-start functions.

The UCC28220 is a primary-side controller for a two-channel interleaved power converter. The device is compatible with forward or flyback converters, as long as a duty cycle clamp between 60% and 90% is required. Therefore, the active clamp forward and flyback converters, as well as the RCD and resonant reset forward converters, are compatible with this device. To ensure the two channels share the total converter output current, current-mode control with internal slope compensation is used. Slope compensation is user programmable via a dedicated pin and can be set over a 50:1 range, ensuring good small-signal stability over a wide range of applications.

Line Overvoltage and Undervoltage

Three pins are provided to turn off the output drivers and reset the soft-start capacitor when the converter input voltage is outside a prescribed range. The undervoltage set point and undervoltage hysteresis are accurately set via external resistors. The overvoltage set point is also accurately set via a resistor ratio, but the hysteresis is fixed by the same resistor that sets the undervoltage hysteresis.

Figure 1 and Figure 2 show a detailed functional diagram and operation of the undervoltage lockout (UVLO) and overvoltage lockout (OVLO) features. The equations for setting the thresholds defined in Figure 2 are:

$$V1 = 1.26 \times \frac{R1}{(R2 + R3)} + 1.26 \quad (1)$$

$$V2 = 1.26 \times \frac{(R1 + Rx)}{Rx}, \text{ where } Rx = R4 \parallel (R2 + R3) \quad (2)$$

$$V4 = 1.26 \times \frac{(R1 + R2 + R3)}{R3} \quad (3)$$

$$V3 = V4 - 1.26 \times \left(\frac{R1}{R4}\right) \quad (4)$$

The UVLO hysteresis and the OVLO hysteresis can then be calculated as V2 – V1 and V4 – V3, respectively. By examining the design equations it becomes apparent that the value of R4 sets the amount of hysteresis at both thresholds. By realizing this fact, the designer can then set the value of R4 based on the most critical hysteresis specification either at high line or at low line. In most designs, the value of R4 is determined by the desired amount of hysteresis around the UVLO threshold. As an example, consider a telecom power supply with the following input UVLO and OVLO design specifications:

- V1 = 32.0 V
- V2 = 34.0 V
- V3 = 83.0 V
- V4 = 84.7 V

then

- R1 = 976 kΩ
- R2 = 24.9 kΩ
- R3 = 15.0 kΩ

and

- R4 = 604 kΩ

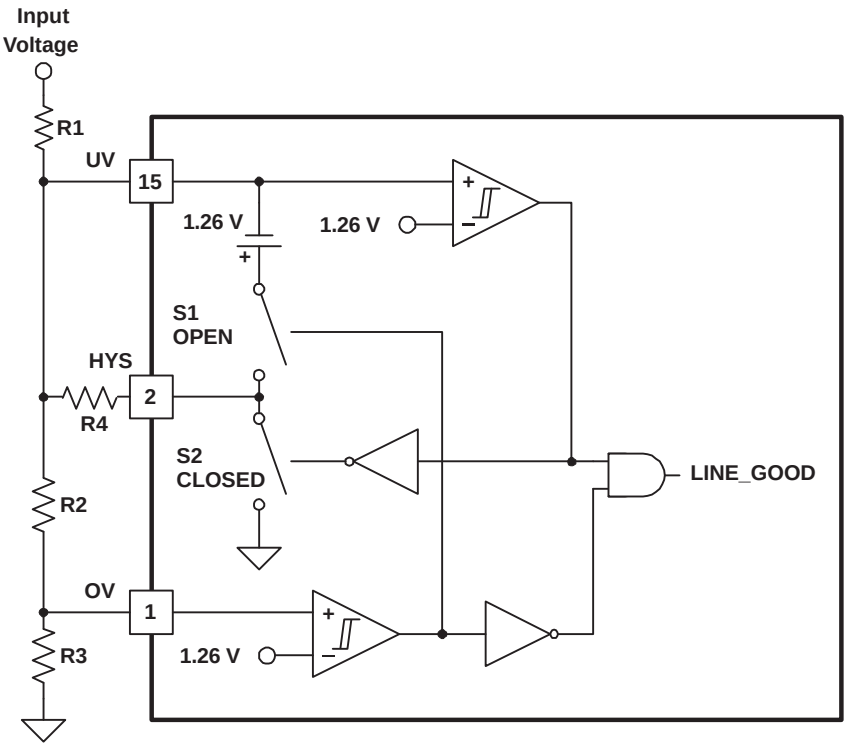


Figure 1. Line UVLO and OVLO Functional Diagram

Figure 2. Line UVLO and OVLO Operation

VDD

Because the driver output impedance is high, the energy storage requirements on the VDD capacitor is low. For improved noise immunity, it is recommended that the VDD pin be bypassed with a minimum of 0.1 μF of capacitance to GND. In most typical applications, the bias voltage for the MOSFET drivers is also used as the VDD supply voltage for the chip. In the aforementioned applications, it is beneficial to add a low-value resistor between the bulk-storage capacitor of the driver and the VDD capacitor for the UCC28220. By adding a resistor in series with the bias supply, any noise that is present on the bias supply is filtered out before getting to the VDD pin of the controller.

Reference

For improved noise immunity, it is recommended that the reference pin (REF) be bypassed with a minimum of 0.1 μF of capacitance to GND.

Oscillator Operation and Maximum Duty Cycle Setpoint

The oscillator uses an internal capacitor to generate the time base for both PWM channels. The oscillator is programmable over a 200-kHz to 2-MHz frequency range with 20% to 80% maximum duty cycle range. Both the dead time and the frequency of the oscillator are divided by two to generate the PWM clock and off-time information for each of the outputs. In this way, a 20% oscillator duty cycle corresponds to a 60% maximum duty cycle at each output, where an 80% oscillator duty cycle yields a 90% duty cycle clamp at each output.

The design equations for the oscillator and maximum duty cycle set point are given by:

$$F_{OSC} = 2 \times F_{OUT} \tag{5}$$

$$D_{MAX(osc)} = 1 - 2 \times \left(1 - D_{MAX(out)}\right) \tag{6}$$

$$R_{CHG} = K_{OSC} \times \frac{D_{MAX(osc)}}{F_{OSC}} \tag{7}$$

$$R_{DISCHG} = K_{OSC} \times \frac{\left(1 - D_{MAX(osc)}\right)}{F_{OSC}} \tag{8}$$

Where

$K_{OSC} = 2.04 \times 10^{10}$ [Ω/s]

F_{OUT} = Switching frequency at the outputs of the chip (Hz)

$D_{MAX(out)}$ = Maximum duty cycle limit at the outputs of the chip

$D_{MAX(osc)}$ = Maximum duty cycle of the Oscillator for the desired maximum duty cycle at the outputs

F_{OSC} = Oscillator frequency for desired output frequency (Hz)

R_{CHG} = External oscillator resistor which sets the charge current (Ω)

R_{DISCHG} = External oscillator resistor which sets the discharge current (Ω)

Soft Start

A current is forced out of the SS pin, equal to 3/7 of the current set by R_{CHG}, to provide a controlled ramp voltage. The current set by the R_{CHG} resistor is equal to 2.5 V divided by R_{CHG}. This ramp voltage overrides the duty cycle on the CTRL pin, allowing a controlled startup. Assuming the UCC28220 is biased on the primary side, the soft start should be quite quick to allow the secondary bias to be generated, and the secondary side control can then take over. Once the soft-start time interval is complete, a closed-loop soft-start on the secondary side can be executed.

$$ISS = \frac{3}{7} \times \frac{2.5}{R_{CHG}} \tag{9}$$

Where

ISS = current which is sourced out of the SS pin during the soft-start time (A)

Current Sense

The current sense signals CS1 and CS2 are level shifted by 0.5 V and have the slope compensation ramps added to them before being compared to the control voltage at the input of the PMW comparators. The amplitude of the current sense signal at full load should be selected such that it is very close to the maximum control voltage, in order to limit the peak output current during short-circuit operation.

Output Drivers

The UCC28220 is intended to interface with the UCC27323/4/5 family of MOSFET drivers. As such, the output drive capability is low (effectively 100 Ω), and the driver outputs swing between GND and REF.

Slope Compensation

The slope compensation circuit in the UCC28220 operates on a cycle-by-cycle basis. The two channels have separate slope compensation circuits. These are fabricated in precisely the same way so as current sharing is unaffected by the slope compensation circuit. For each channel, an internal capacitor is reset whenever that channel's output is off. At the beginning of the PWM cycle, a current is mirrored off the SLOPE pin into the capacitor, developing an independent ramp. Since the two channel's ramps start when the channel's output changes from a low to high state, the ramps are thus interleaved. These internal ramps are added to the voltages on the current sense pins (CS1 and CS2) and the result forms an input to the PWM comparators.

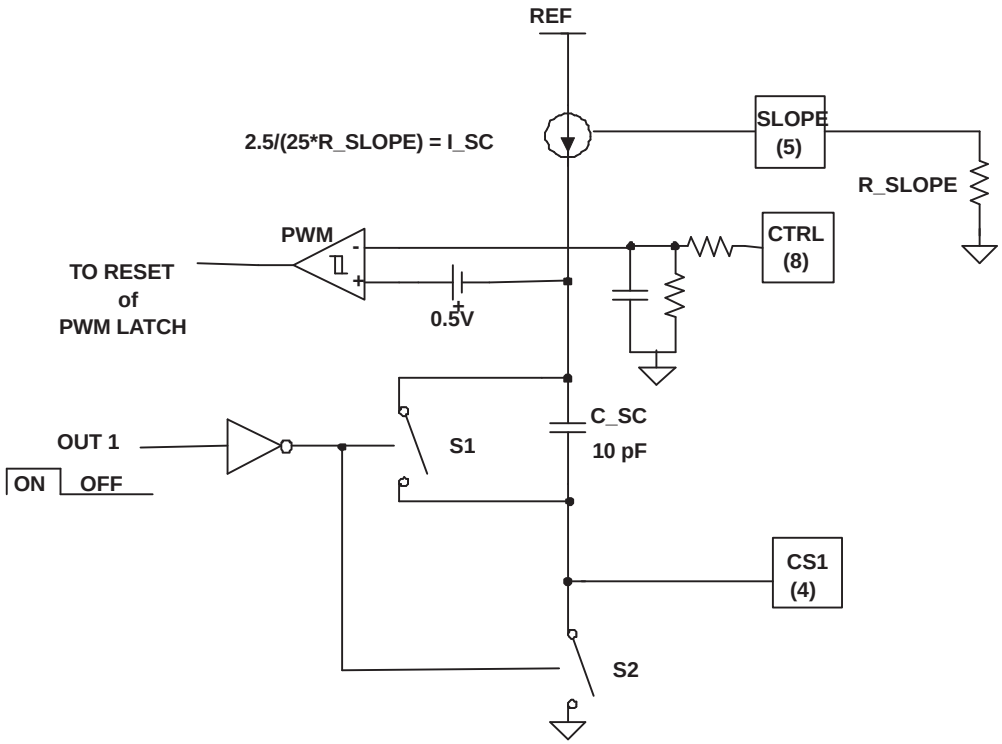


Figure 3. Slope Compensation Detail for Channel 1 (Duplicate Matched Circuitry for Channel 2)

To ensure stability, the slope compensation circuit must add between 1/5 and 1 times the inductor downslope to each of the current sense signals prior to being applied to the PWM comparator's input.

Determining the value for the slope compensation resistor:

Design Example

$N_{CT(p)}$ = 1	V_{OUT} = 12	Np = 7	R_{SENSE} = 5.23	$F_{S(out)}$ = 500000
$N_{CT(s)}$ = 50	L_{OUT} = 3.2 x 10^{-6}	Ns = 5	$V_{EA(cl)}$ = 1.98	

Where

$N_{CT(p)}$ = Number of primary turns on the Current Transformer (Turns)
$N_{CT(s)}$ = Number of Secondary turns on the current transformer (Turns)
V_{OUT} = Nominal output voltage of the converter (V)
L_{OUT} = Inductance value of each output inductor (H)
N_P = Number of primary turns on the main transformer (Turns)
N_S = Number of secondary turns on the main transformer (Turns)
R_{SENSE} = Value of current sense resistor on secondary of current sense transformer (Ω)
$V_{EA(cl)}$ = Maximum value of the E/A output voltage (V)
$F_{S(out)}$ = Switching frequency of each output (Hz)

Determine the correct value for the slope resistor, R_{SLOPE}, to provide the desired amount of slope compensation.

$$N_{CT} = \frac{N_{CT(p)}}{N_{CT(s)}}, \text{ Current Transformer Turns Ratio} \tag{10}$$

1. Transform the secondary inductor downslope to the primary

$$S_{L(prime)} = \frac{V_{OUT}}{L_{OUT}} \times \frac{N_s}{N_p}, \quad S_{L(prime)} = 2.679 \text{ A/µs} \tag{11}$$

2. Calculate the transformed slope voltage at sense resistor

$$VS_{L(prime)} = S_{L(prime)} \times N_{CT} \times R_{SENSE}, \quad VS_{L(prime)} = 2.281 \text{ V/µs} \tag{12}$$

3. Calculate the R_{SLOPE} value to give a compensating ramp equal to the transformed slope voltage given in Equation 12

$$M = 1.0 \tag{13}$$

The desired ratio between the compensating ramp and the output inductor downslope ramp, transformed to the primary sense resistor, is shown in Equation 14.

$$R_{SLOPE} = \frac{10^4}{\left(M \times VS_{L(prime)} \times 10^{-6}\right)}, \quad R_{SLOPE} = 35.556 \text{ k}\Omega \tag{14}$$

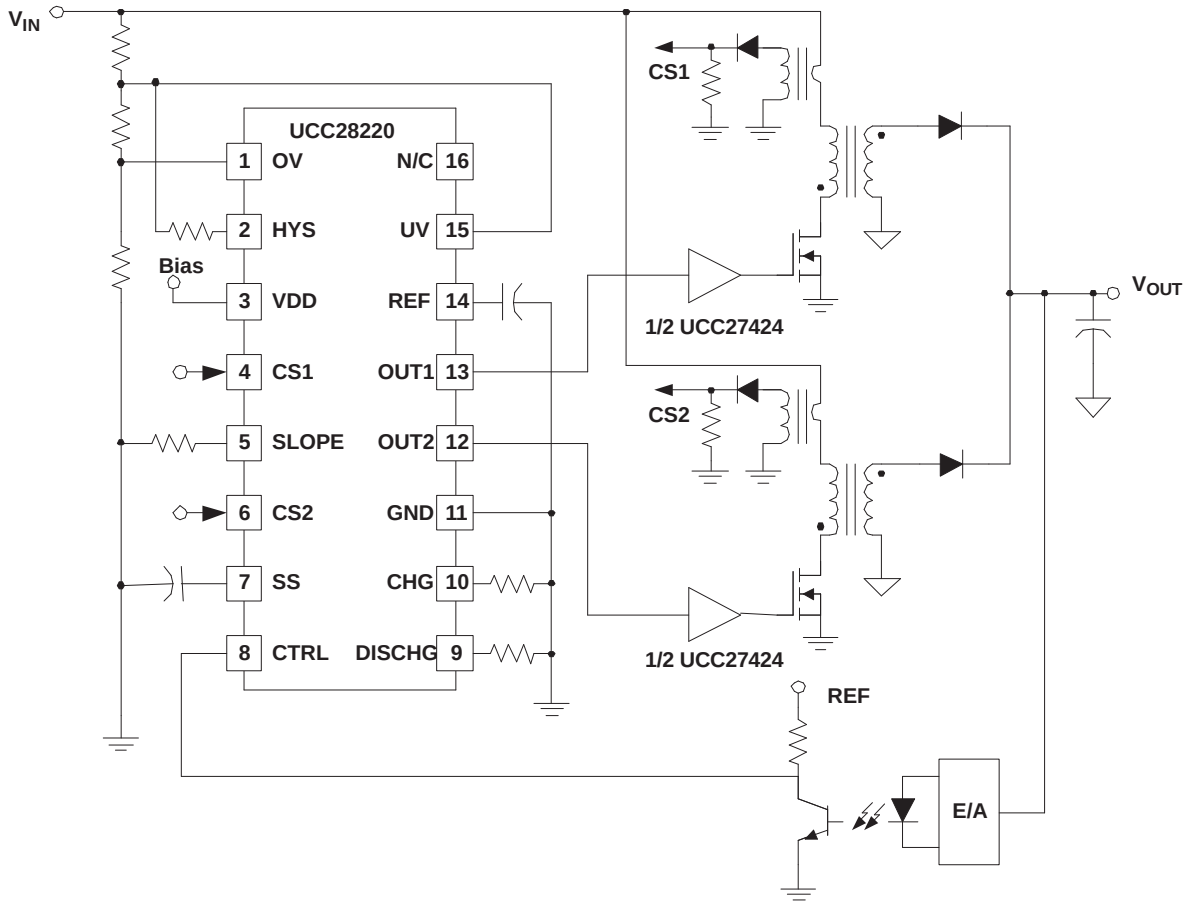


Figure 4. Interleaved Flyback Application Circuit

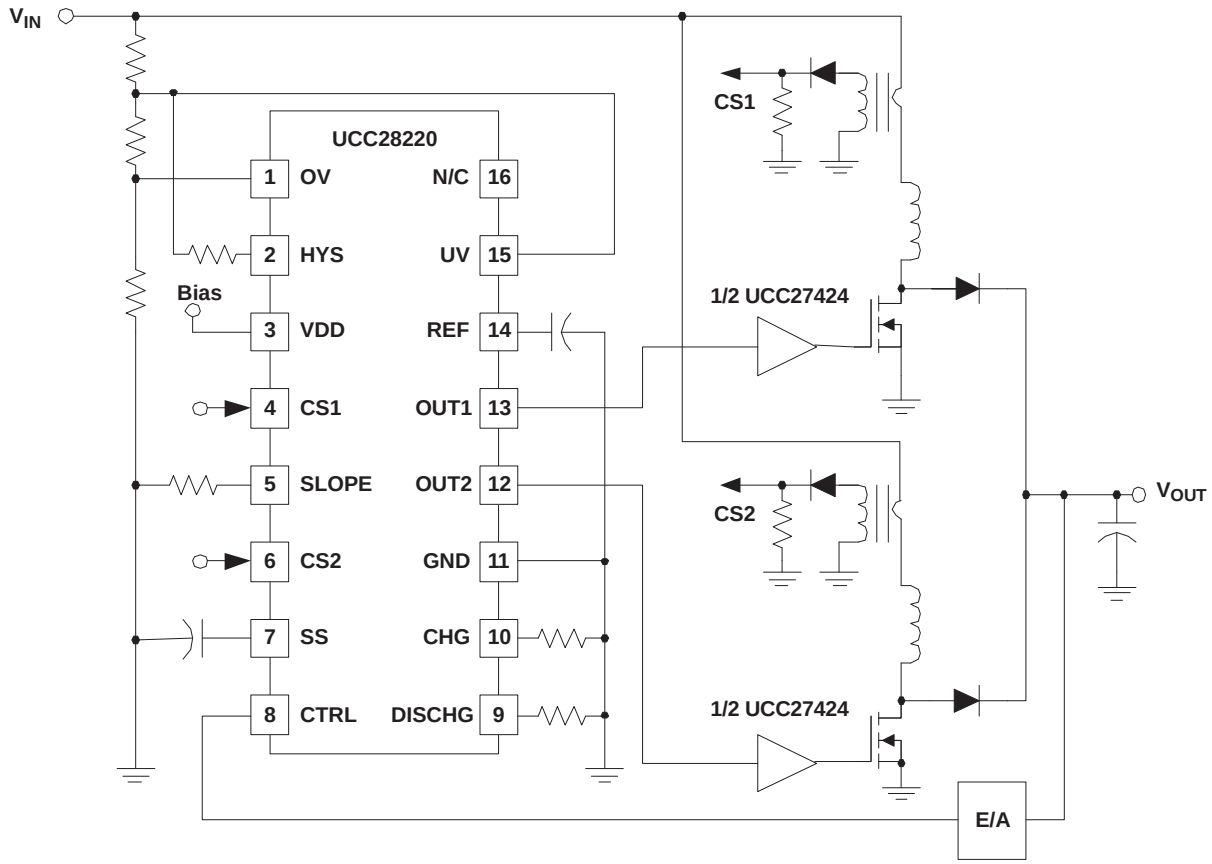


Figure 5. Interleaved Boost Application Circuit

TYPICAL CHARACTERISTICS

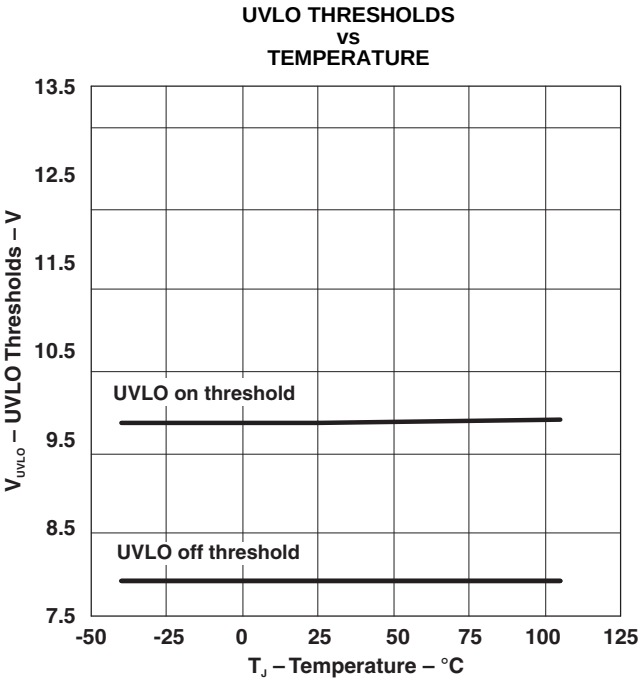


Figure 6.

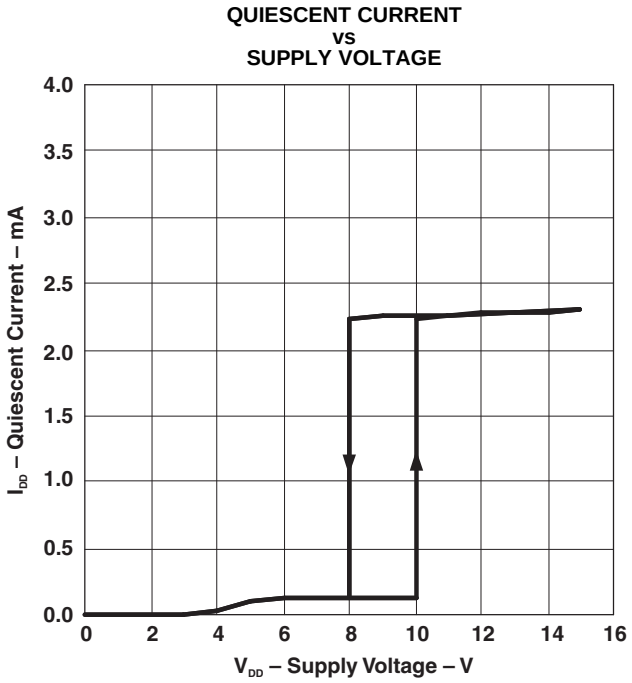


Figure 7.

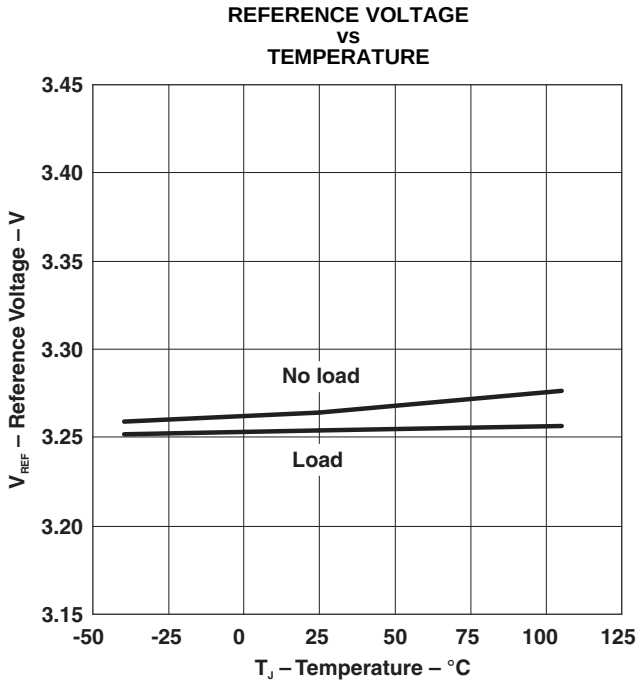


Figure 8.

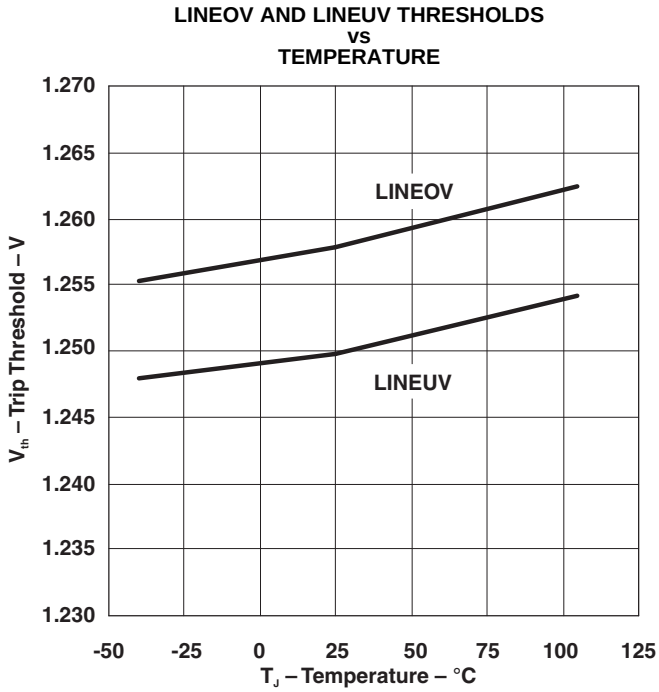


Figure 9.

TYPICAL CHARACTERISTICS (continued)

SLOPE COMPENSATION
vs
TEMPERATURE

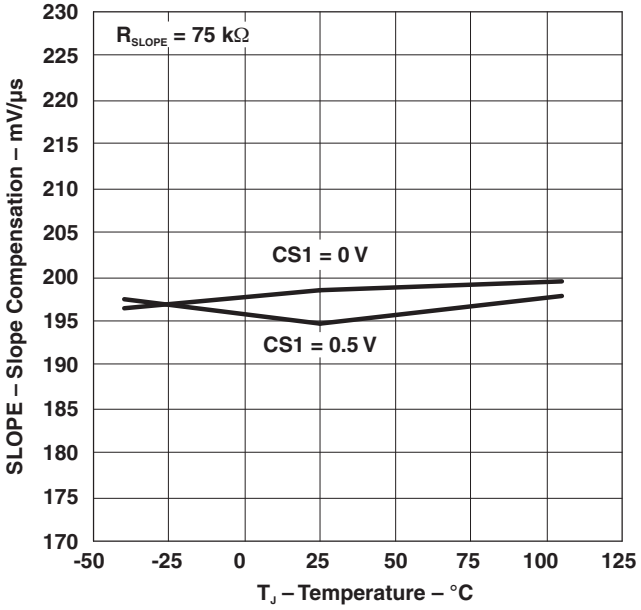


Figure 10.

PROGRAMMING RESISTOR
vs
SLOPE COMPENSATION

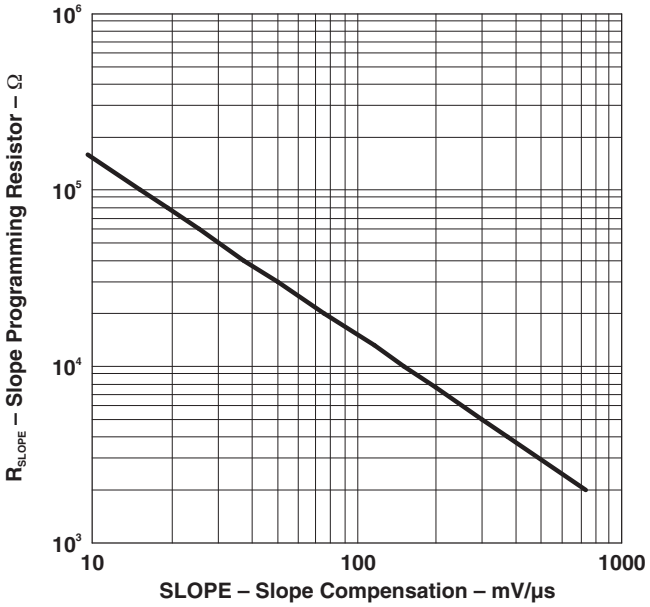


Figure 11.

CHANNEL 1 AND CHANNEL 2 SLOPE MATCHING
vs
TEMPERATURE

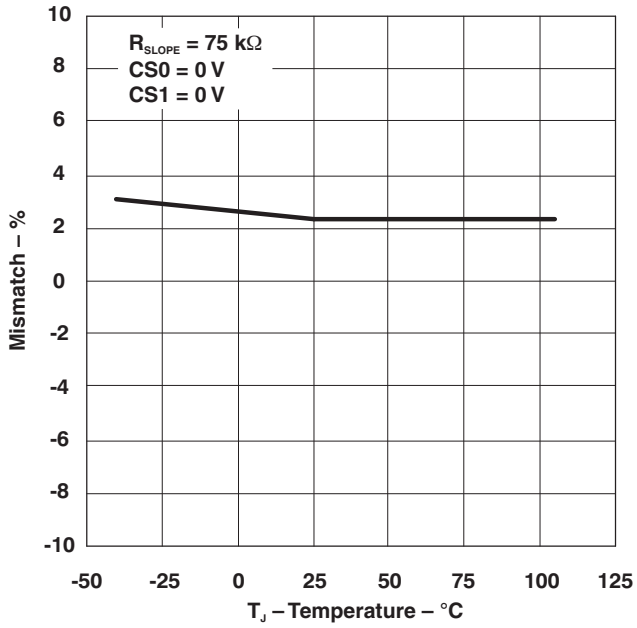


Figure 12.

RISE AND FALL TIME
vs
TEMPERATURE (C_L = 50 pF

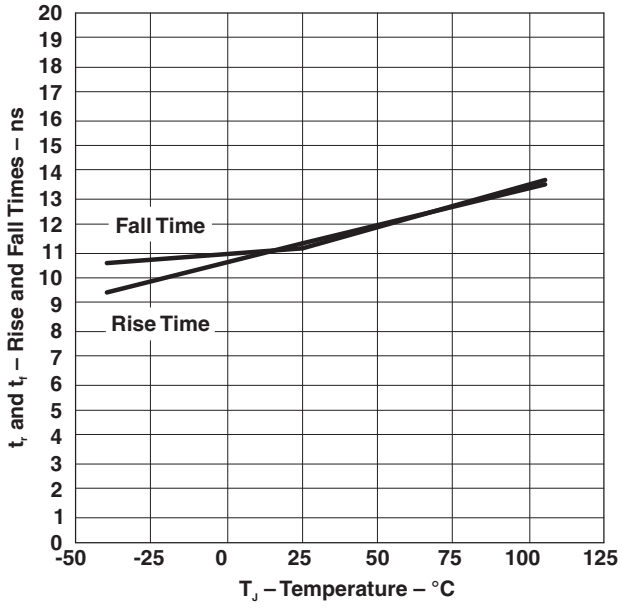


Figure 13.

TYPICAL CHARACTERISTICS (continued)

V_{OH} AND V_{OL} VS TEMPERATURE

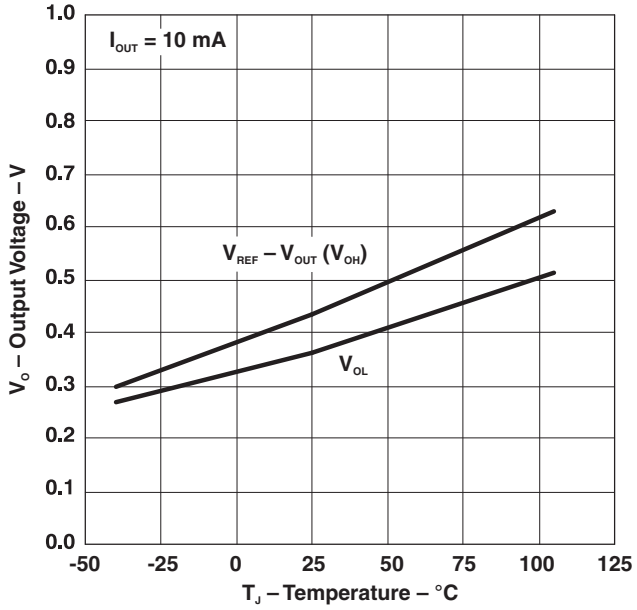


Figure 14.

SOFT-START CHARGE CURRENT VS TEMPERATURE

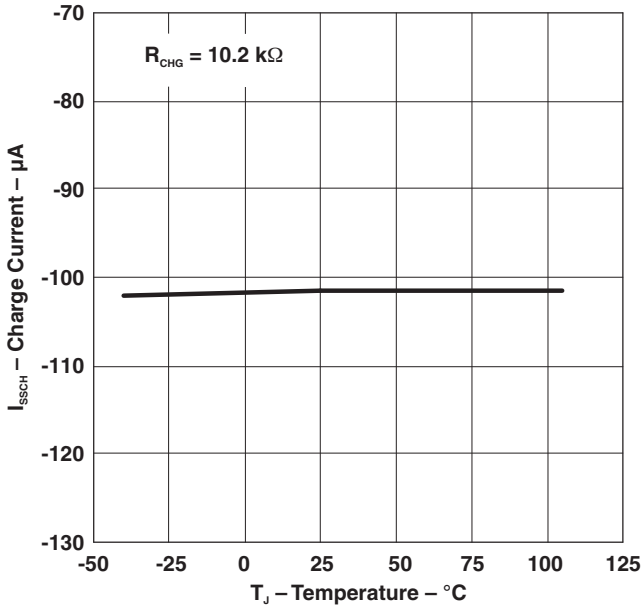


Figure 15.

SOFT-START DISCHARGE CURRENT VS TEMPERATURE

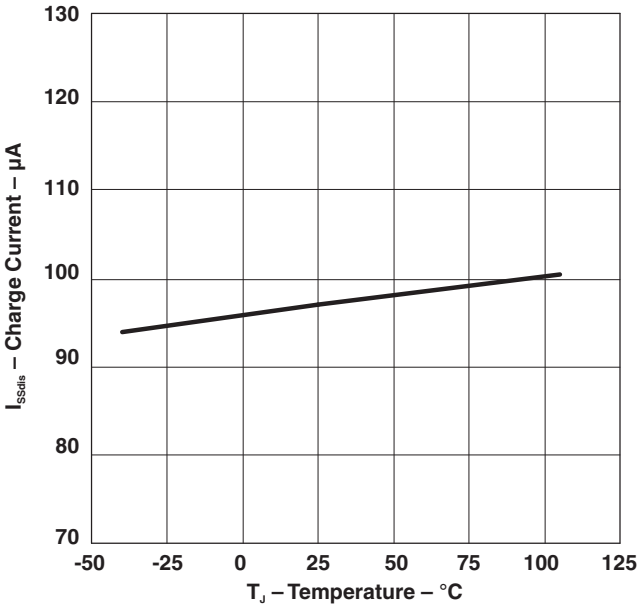


Figure 16.

PROGRAMMING RESISTORS VS SWITCHING FREQUENCY

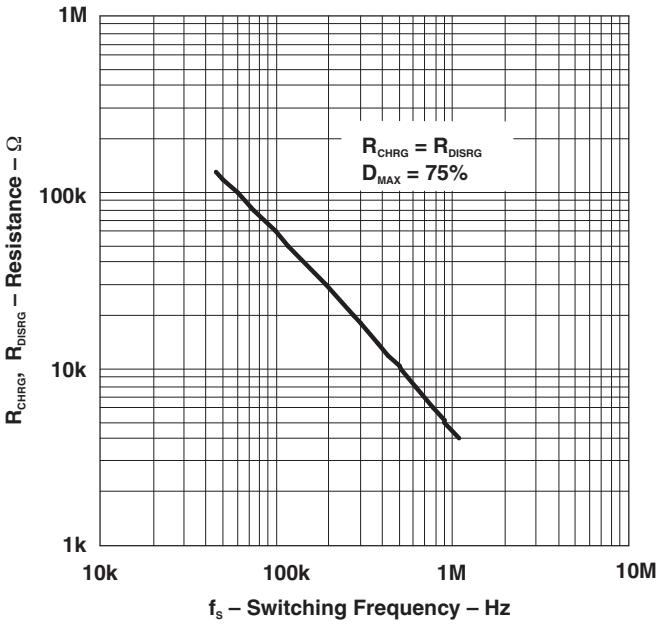


Figure 17.

TYPICAL CHARACTERISTICS (continued)

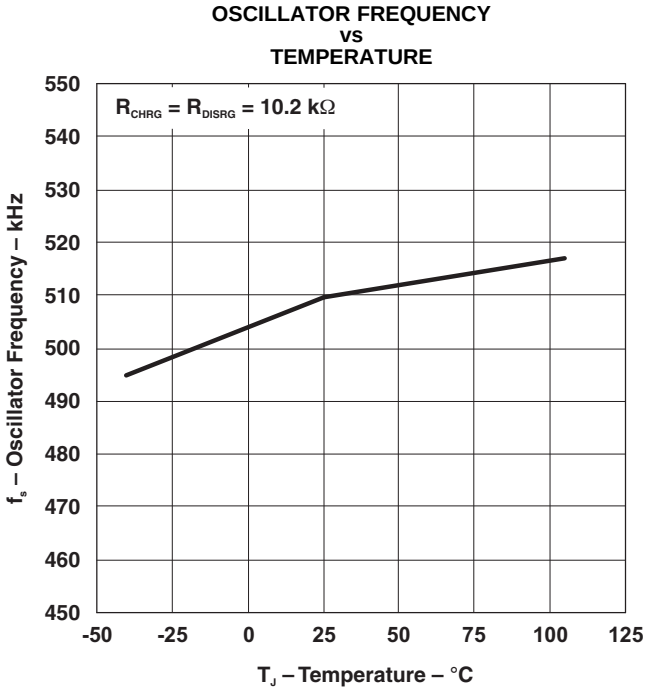


Figure 18.

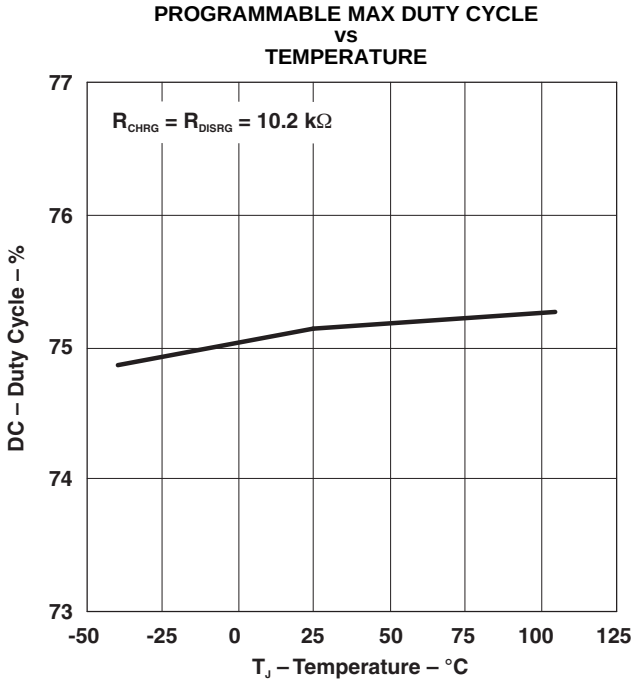


Figure 19.

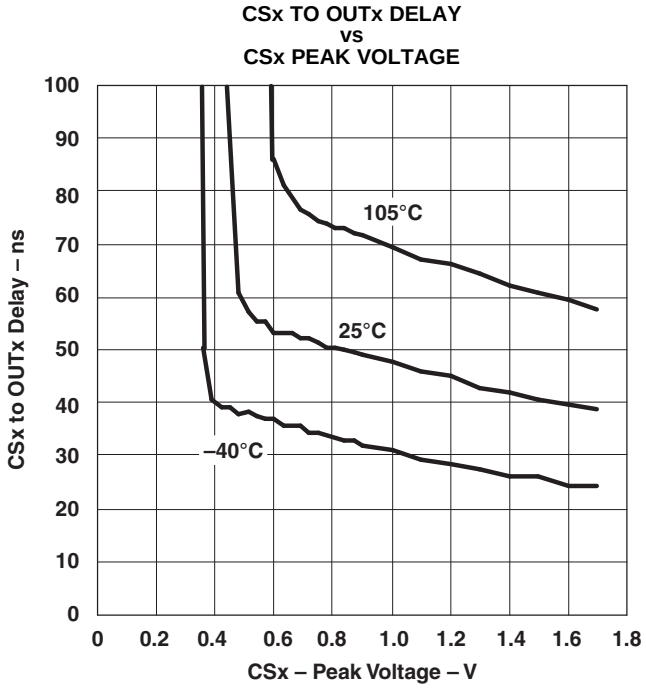


Figure 20.

Related Products

DEVICE	DESCRIPTION	PACKAGE OPTIONS
UCC27323/4/5	Dual 4-A High-Speed Low-Side MOSFET Drivers	SOIC-8, PowerPAD™ MSOP-8, PDIP-8
UCC27423/4/5	Dual 4-A High-Speed Low-Side MOSFET Drivers with Enable	SOIC-8, PowerPAD MSOP-8, PDIP-8
TPS2811/12/13	Dual 2.4-A High-Speed Low-Side MOSFET Drivers	SOIC-8, TSSOP-8, PDIP-8
UC3714/15	Dual 2.4-A High-Speed Low-Side MOSFET Drivers	SOIC-8, PowerSOIC-14, PDIP-8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28220QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28220Q	Samples
UCC28220QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28220Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC28220-Q1 :

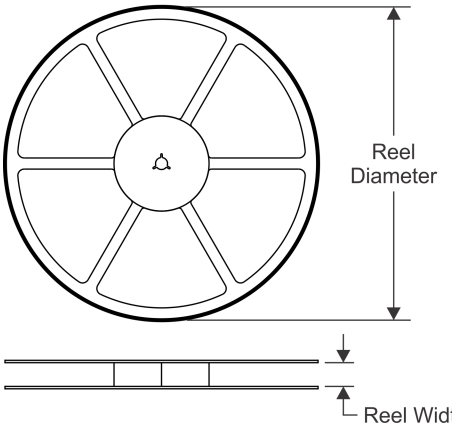
- Catalog: UCC28220

NOTE: Qualified Version Definitions:

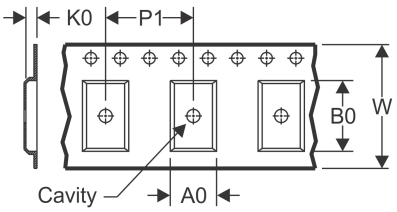
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

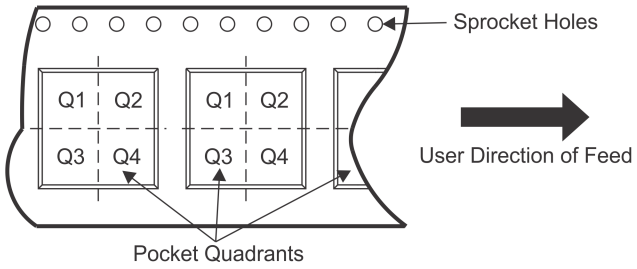


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

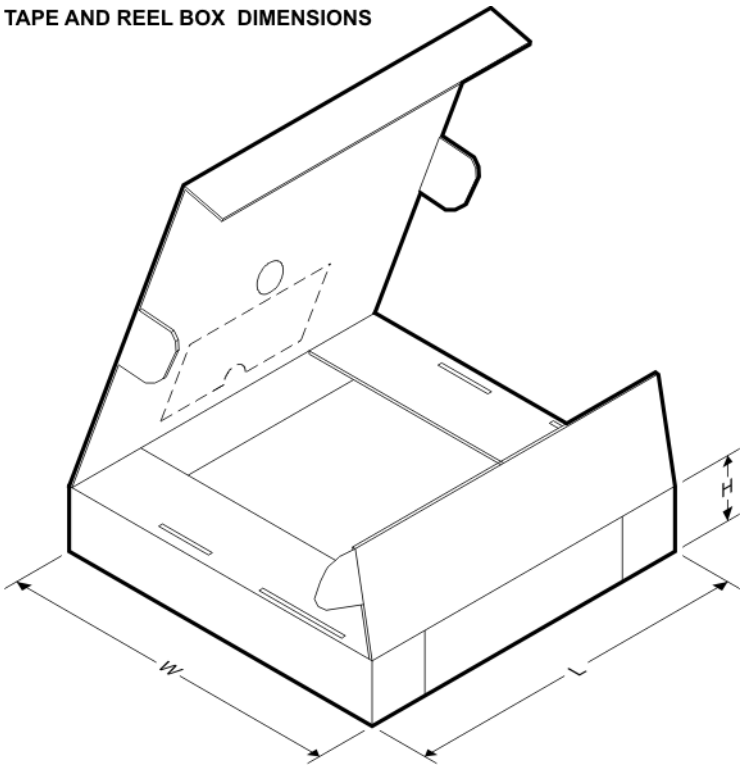
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28220QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC28220QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

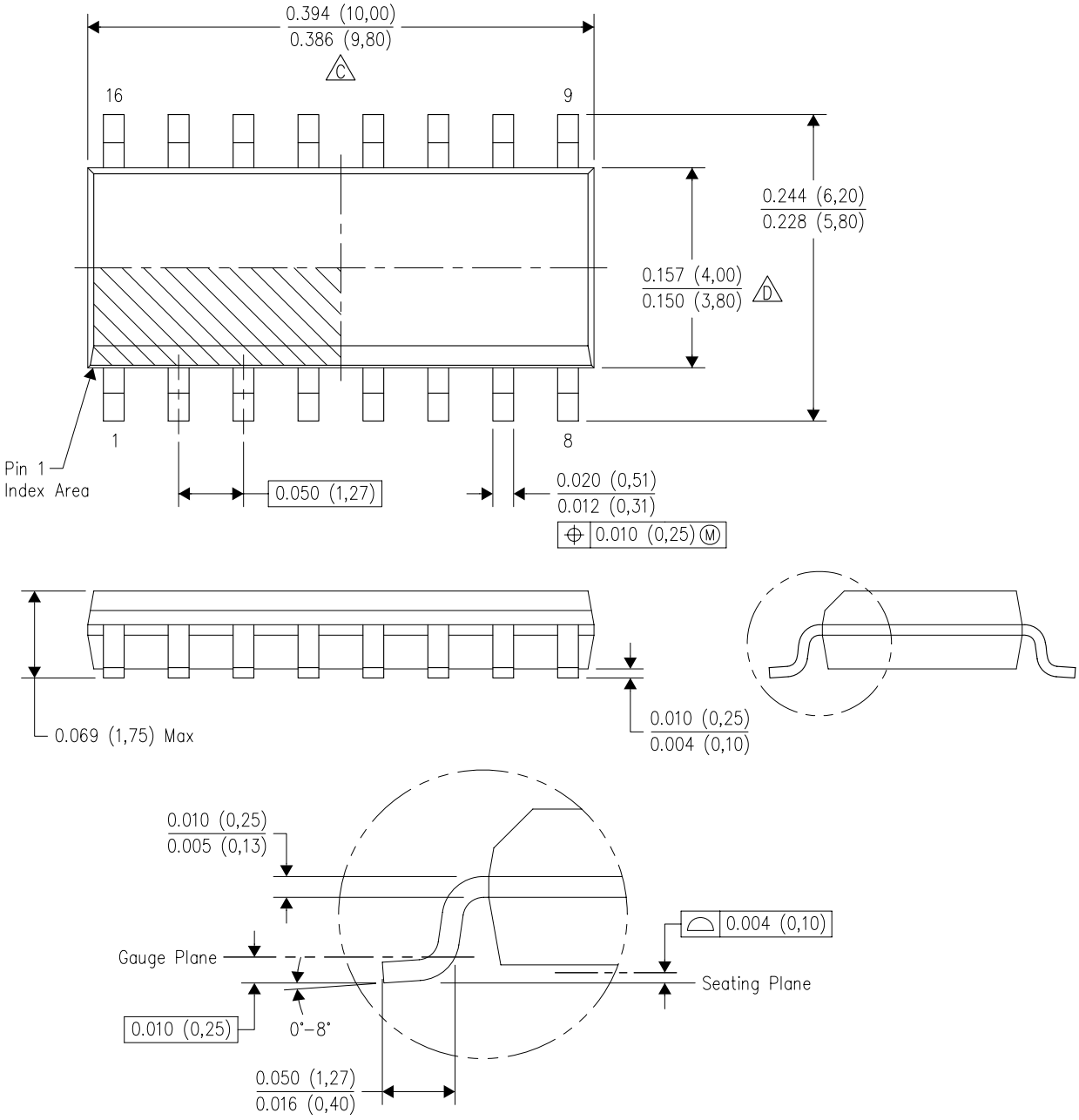
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28220QDRQ1	SOIC	D	16	2500	367.0	367.0	38.0
UCC28220QPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



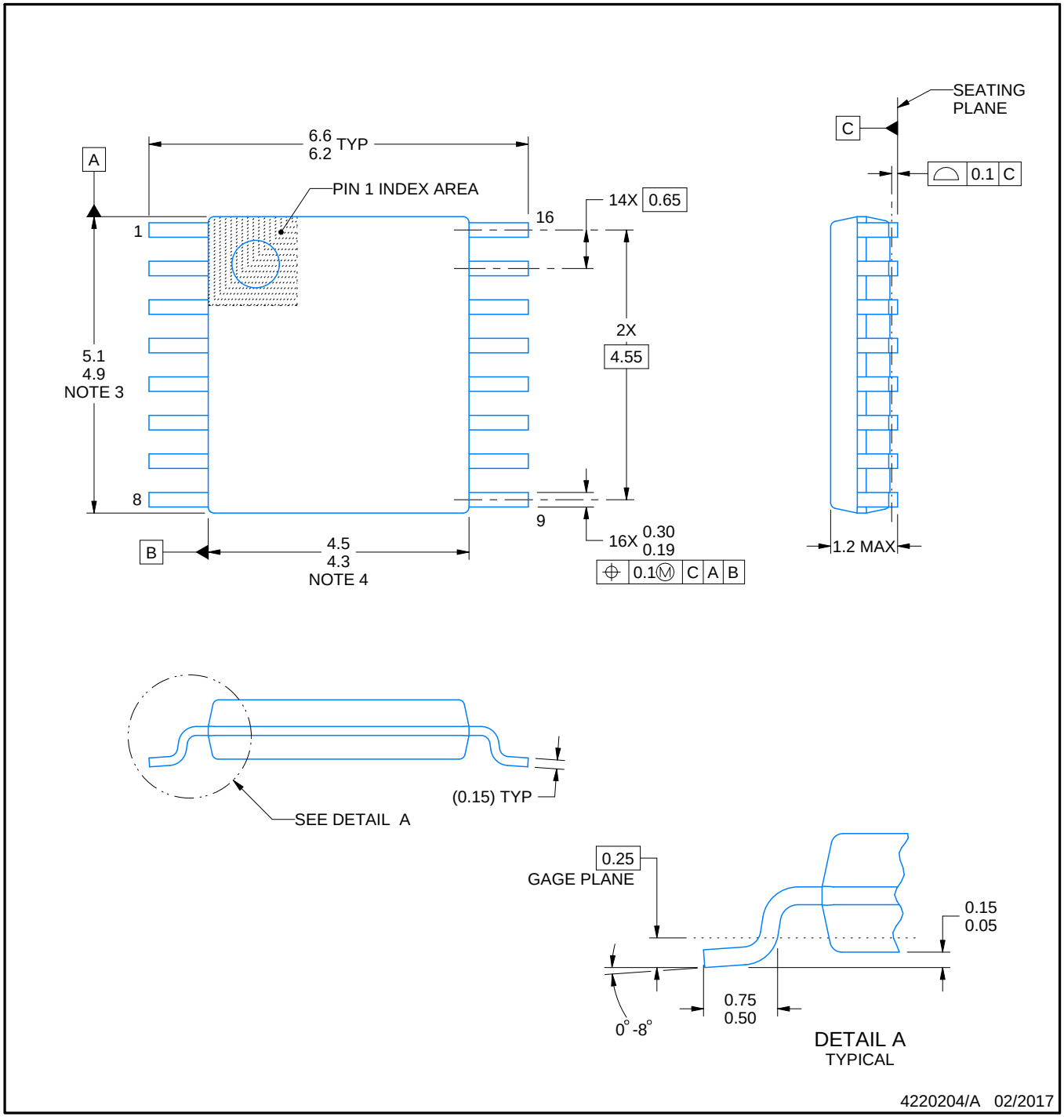
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

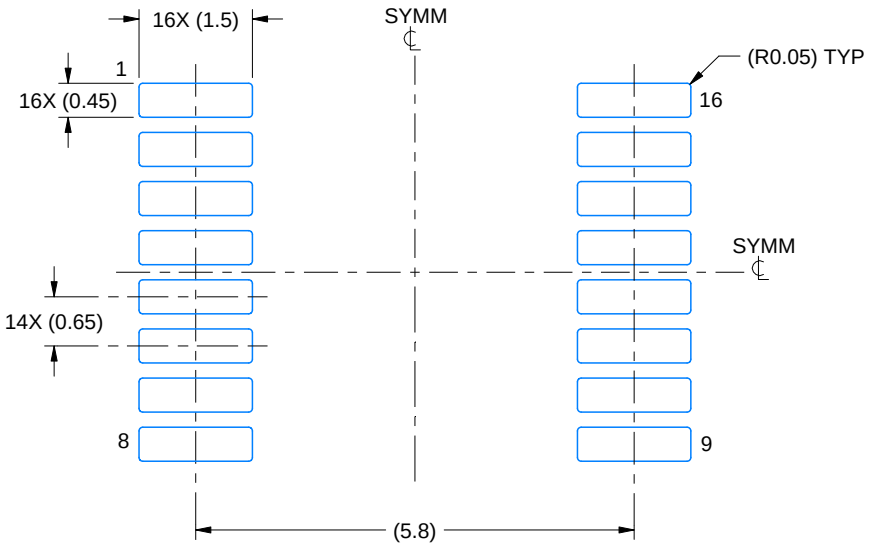
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

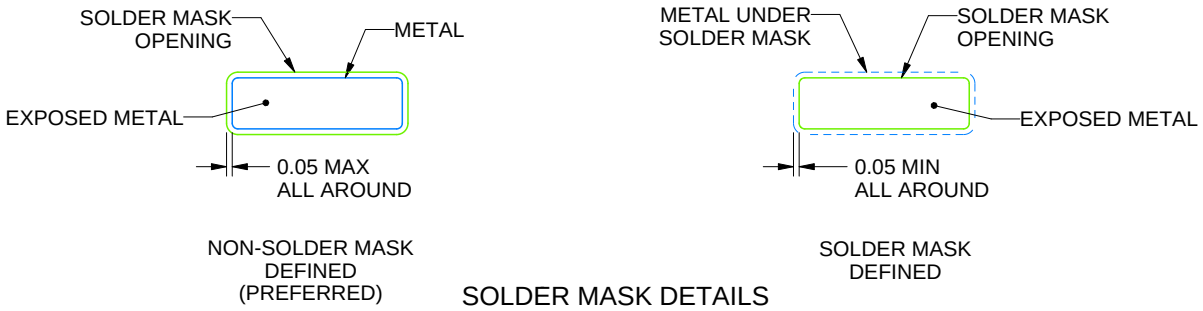


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

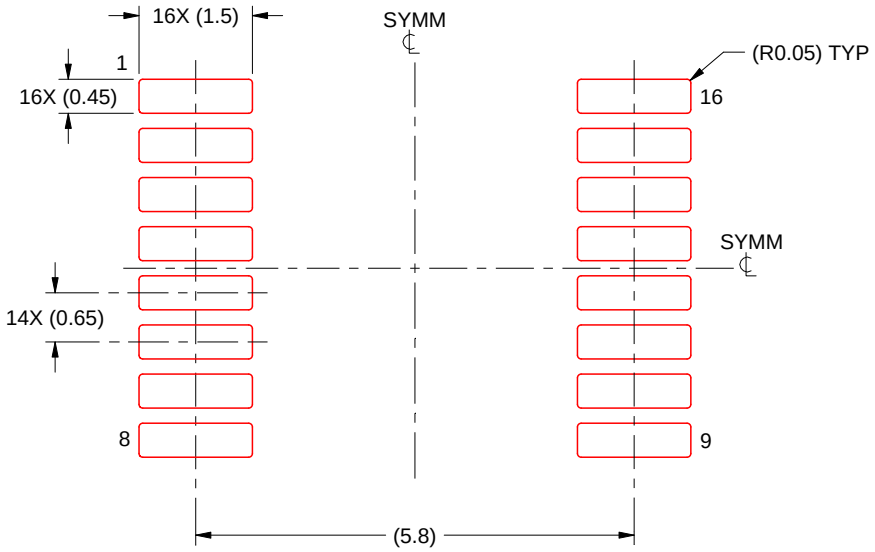


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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