



## UCD4015

CMOS IC

### CMOS Dual 4-Stage Static Shift Register

#### DESCRIPTION

**UCD4015** consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET input as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All registers stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one UCD4015 package or to more than 8 stages using additional UCD4015's is possible.

#### FEATURES

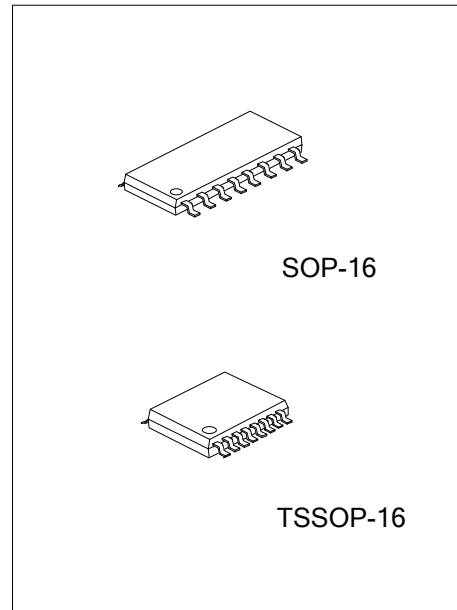
- \* 12MHz (typ.) clock rate at 10V
- \* Maximum input current of 1µA at 18V
- \* Fully static operation
- \* 8 master-slave flip-flops plus input and output buffering

#### APPLICATIONS

- \* General-purpose register
- \* Serial-input/parallel-output data queueing
- \* Serial to parallel data conversion

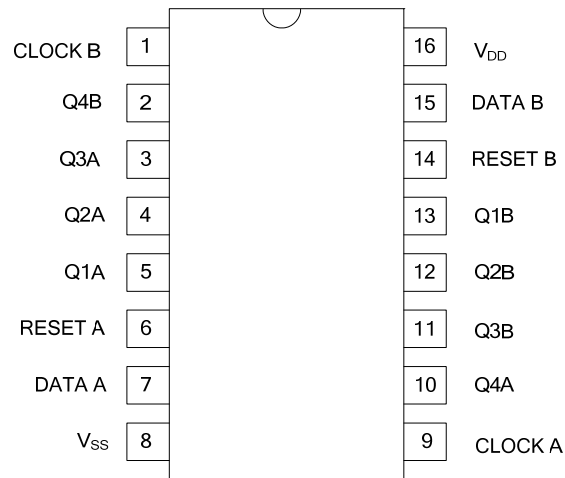
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4015L-S16-T	UCD4015G-S16-T	SOP-16	Tube
UCD4015L-S16-R	UCD4015G-S16-R	SOP-16	Tape Reel
UCD4015L-P16-T	UCD4015G-P16-T	TSSOP-16	Tube
UCD4015L-P16-R	UCD4015G-P16-R	TSSOP-16	Tape Reel

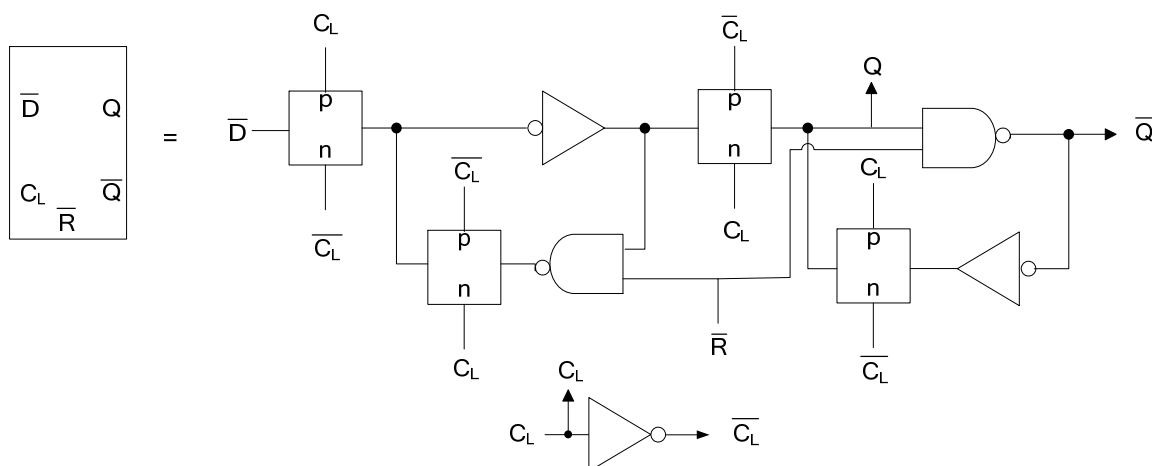
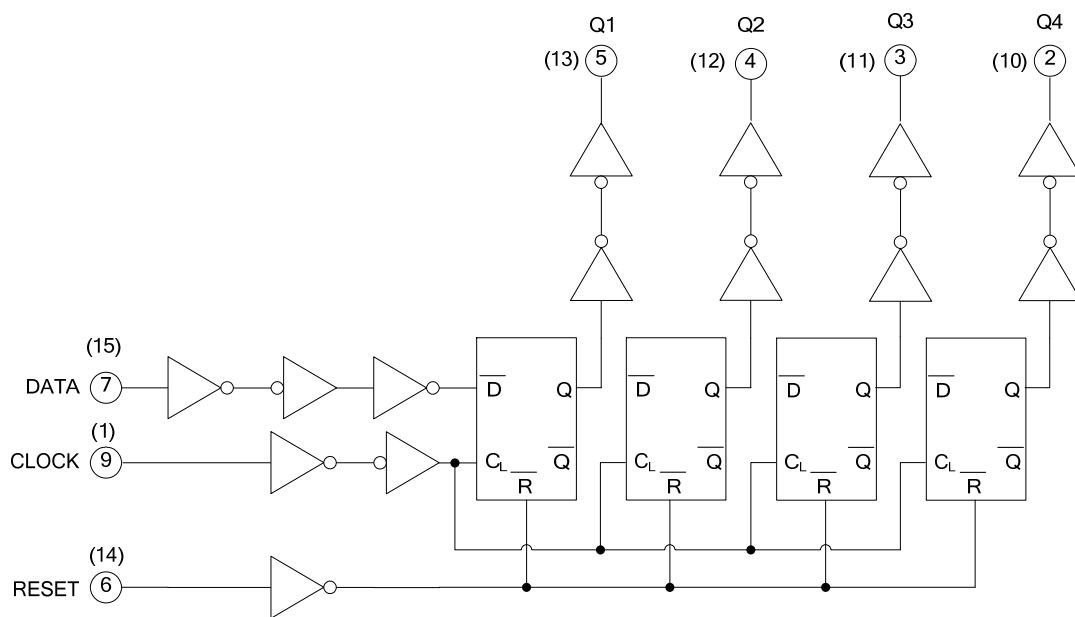


<p>UCD4015L-S16-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Free</p>	<p>(1) T: Tube, R: Tape Reel (2) S16: SOP-16, P16: TSSOP-16 (3) L: Lead Free, G: Halogen Free</p>
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## ■ PIN CONFIGURATION



## ■ LOGIC DIAGRAM



## ■ TRUE TABLE

$C_L$	D	R	$Q_1$	$Q_n$
	0	0	0	$Q_{n-1}$
	1	0	1	$Q_{n-1}$
X	X	1	0	0
	X	0	$Q_1$	$Q_n$ (NC)

Note: X = DON'T CARE CASE, NC = NO CHANGE

■ ABSOLUTE MAXIMUM RATING ( $T_A = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	-0.5 ~ 20	V
Input Voltage	$V_{IN}$	-0.5 ~ $V_{CC} + 0.5$	V
Output Voltage	$V_{OUT}$	-0.5 ~ $V_{CC} + 0.5$	V
Input Clamp Current ( $V_{IN} < 0$ , or $V_{IN} > V_{CC}$ )	$I_{IK}$	$\pm 10$	mA
Power Dissipation	$P_D$	500	mW
Operating Temperature	$T_{OPR}$	-40 ~ +125	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-65 ~ +150	$^\circ\text{C}$

Note: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	73	$^\circ\text{C/W}$
	TSSOP-16	108	$^\circ\text{C/W}$

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{DD}$		3		18	V
Clock Pulse Width	$t_w$	$V_{DD}=5\text{V}$	180			ns
		$V_{DD}=10\text{V}$	80			
		$V_{DD}=15\text{V}$	50			
Clock Frequency	$f_{CL}$	$V_{DD}=5\text{V}$			3	MHz
		$V_{DD}=10\text{V}$			6	
		$V_{DD}=15\text{V}$			8.5	
Clock Rise and Fall Time	$t_r, t_f$	$V_{DD}=5\text{V}$			15	$\mu\text{s}$
		$V_{DD}=10\text{V}$			6	
		$V_{DD}=15\text{V}$			2	
Data Set-up Time	$t_{SU}$	$V_{DD}=5\text{V}$	70			ns
		$V_{DD}=10\text{V}$	40			
		$V_{DD}=15\text{V}$	30			

■ ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current	$I_{DD}$	$V_{IN}=0, 5\text{V}, V_{DD}=5\text{V}$		0.04	5	$\mu\text{A}$
		$V_{IN}=0, 10\text{V}, V_{DD}=10\text{V}$		0.04	10	
		$V_{IN}=0, 15\text{V}, V_{DD}=15\text{V}$		0.04	20	
		$V_{IN}=0, 20\text{V}, V_{DD}=20\text{V}$		0.08	100	
Output Low (Sink) Current	$I_{OL}$	$V_{OUT}=0.4\text{V}, V_{DD}=5\text{V}$	0.51	1		mA
		$V_{OUT}=0.5\text{V}, V_{DD}=10\text{V}$	1.3	2.6		
		$V_{OUT}=1.5\text{V}, V_{DD}=15\text{V}$	3.4	6.8		
Output High (Source) Current	$I_{OH}$	$V_{OUT}=4.6\text{V}, V_{DD}=5\text{V}$	-0.51	-1		mA
		$V_{OUT}=2.5\text{V}, V_{DD}=5\text{V}$	-1.6	-3.2		
		$V_{OUT}=9.5\text{V}, V_{DD}=10\text{V}$	-1.3	-2.6		
		$V_{OUT}=13.5\text{V}, V_{DD}=15\text{V}$	-3.4	-6.8		
Output Voltage: Low-Level	$V_{OL}$	$V_{DD}=5\text{V}$		0	0.05	V
		$V_{DD}=10\text{V}$		0	0.05	
		$V_{DD}=15\text{V}$		0	0.05	
Output Voltage: High-Level	$V_{OH}$	$V_{DD}=5\text{V}$	4.95	5		V
		$V_{DD}=10\text{V}$	9.95	10		
		$V_{DD}=15\text{V}$	14.95	15		

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Low Voltage	$V_{IL}$	$V_{OUT}=0.5, 4.5V, V_{DD}=5V$			1.5	V
		$V_{OUT}=1, 9V, V_{DD}=10V$			3	
		$V_{OUT}=1.5, 13.5V, V_{DD}=15V$			4	
Input High Voltage	$V_{IH}$	$V_{OUT}=0.5, 4.5V, V_{DD}=5V$	3.5			V
		$V_{OUT}=1, 9V, V_{DD}=10V$	7			
		$V_{OUT}=1.5, 13.5V, V_{DD}=15V$	11			
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=0, 18V, V_{DD}=18V$			$\pm 0.1$	$\mu A$

■ SWITCHING CHARACTERISTICS ( $T_A=25^\circ C$ , Input  $t_r, t_f=20ns$ ,  $C_L=50pF$ ,  $R_L=200K\Omega$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CLOCKED OPERATION</b>						
Propagation Delay Time	$t_{PLH} / t_{PHL}$	$V_{DD}=5V$		160	320	ns
		$V_{DD}=10V$		80	160	
		$V_{DD}=15V$		60	120	
Transition Time	$t_{THL} / t_{TLH}$	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	
		$V_{DD}=15V$		40	80	
Maximum Clock Input Frequency	$f_{CL}$	$V_{DD}=5V$	3	6		MHz
		$V_{DD}=10V$	6	12		
		$V_{DD}=15V$	8.5	17		
Minimum Clock Pulse Width	$t_{WCL}$	$V_{DD}=5V$		90	180	ns
		$V_{DD}=10V$		40	80	
		$V_{DD}=15V$		25	50	
Clock Rise and Fall Time	$t_{rCL} / t_{fCL}$	$V_{DD}=5V$			15	$\mu s$
		$V_{DD}=10V$			6	
		$V_{DD}=15V$			2	
Minimum Data Setup Time	$t_{SU}$	$V_{DD}=5V$		35	70	ns
		$V_{DD}=10V$		20	40	
		$V_{DD}=15V$		15	30	
Minimum Data Hold Time	$t_H$	$V_{DD}=5V$			0	ns
		$V_{DD}=10V$			0	
		$V_{DD}=15V$			0	
Average Input Capacitance	$C_i$	Any Input		5	7.5	pF
<b>RESET OPERATION</b>						
Propagation Delay Time	$t_{PLH} / t_{PHL}$	$V_{DD}=5V$		200	400	ns
		$V_{DD}=10V$		100	200	
		$V_{DD}=15V$		80	160	
Minimum Reset Pulse Width	$t_{WR}$	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		40	80	
		$V_{DD}=15V$		30	60	

■ TEST CIRCUIT AND WAVEFORMS

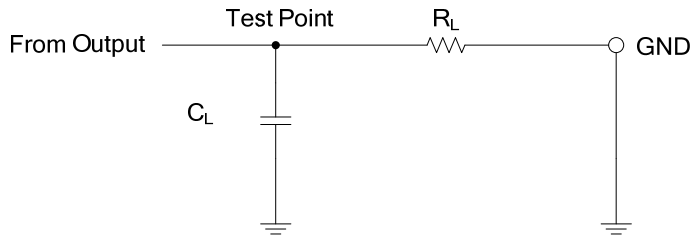


Fig 1. TEST CIRCUIT

Inputs		VM	VLOAD	CL	RL
VIN	tr, tf				
VDD	20 ns	VDD/2	VDD	50 pF	200 KΩ

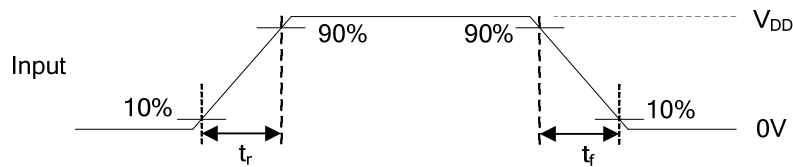


Fig2. VOLTAGE WAVEFORMS INPUT RISE AND FALL TIMES

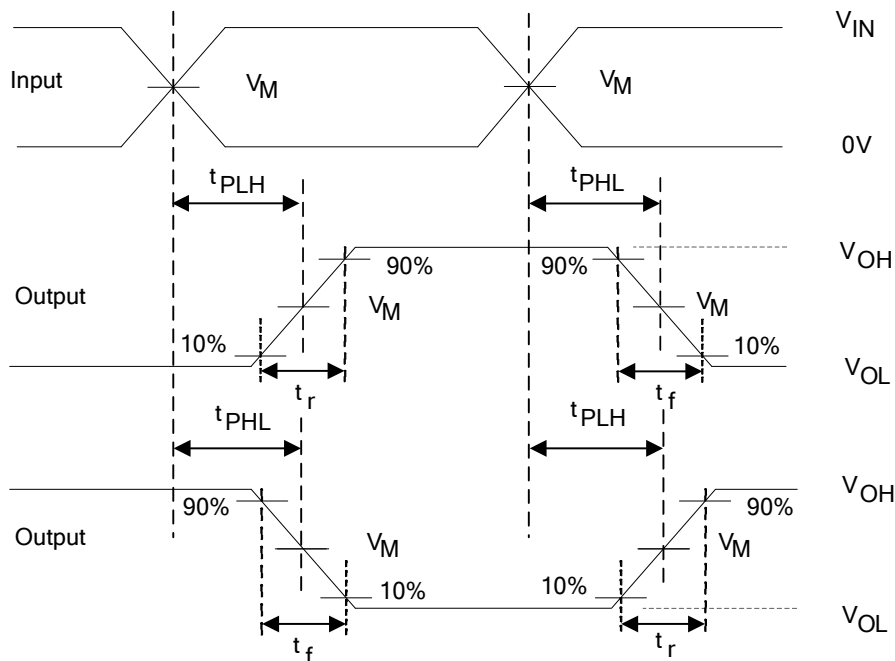


Fig3. VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- Notes: 1. CL includes probe and jig capacitance.
- 2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, ZO = 50Ω.

■ TEST CIRCUIT AND WAVEFORMS(Cont.)

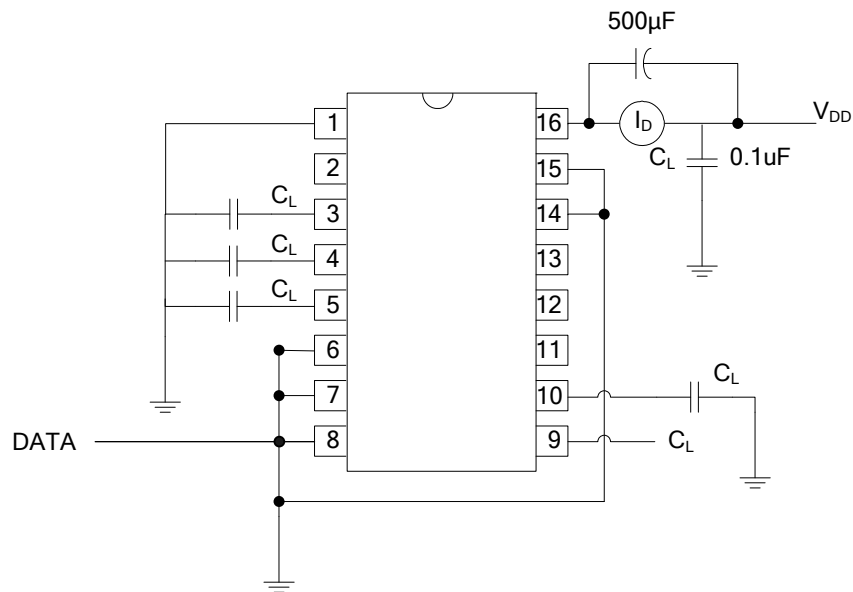


Fig4. Dynamic power dissipation test circuit

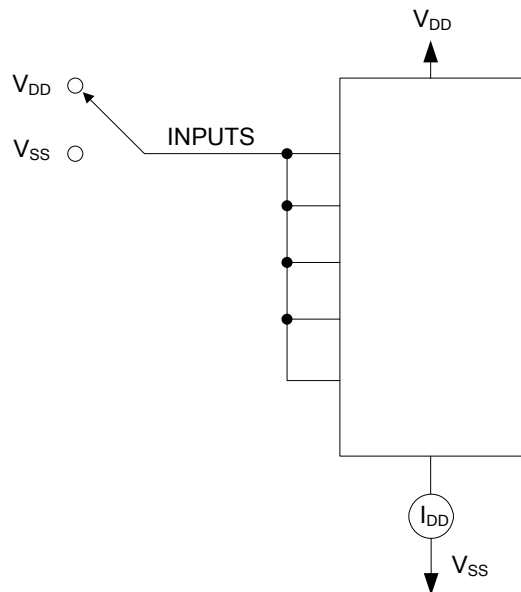
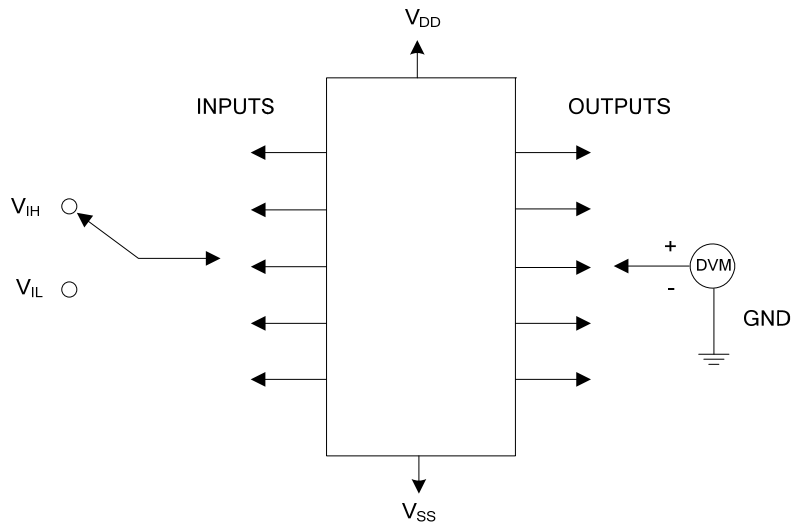
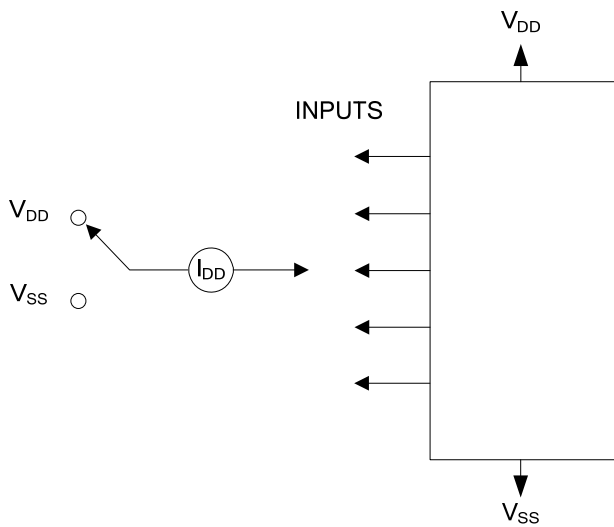


Fig5. Quiescent device current test circuit

■ TEST CIRCUIT AND WAVEFORMS(Cont.)



**Fig6 Input voltage test circuit**



**Fig7 Input current test circuit**

Note: measure inputs sequentially, to both  $V_{DD}$  and  $V_{SS}$ ; connect all unused inputs to either  $V_{DD}$  or  $V_{SS}$ .

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