

BIMOS LATCH/DRIVERS
ADVANCE DATA

- HIGH-VOLTAGE, HIGH-CURRENT OUTPUTS
- OUTPUT TRANSIENT PROTECTION
- CMOS, PMOS, NMOS, TTL COMPATIBLE INPUTS
- INTERNAL PULL-DOWN RESISTORS
- LOW-POWER CMOS LATCHES

the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

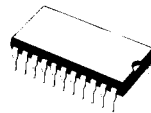
DESCRIPTION

The UCN4801A is a high-voltage, high-current latch/driver comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility.

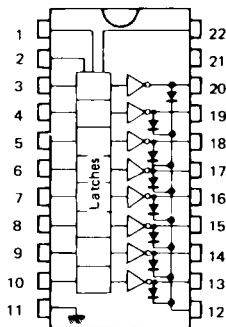
The CMOS inputs are compatible with standard CMOS, PMOS and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power load.

The unit feature open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation,

DIP-22
(Plastic)



ORDER CODE : UCN4801ADP

PIN CONNECTIONS (Top view)


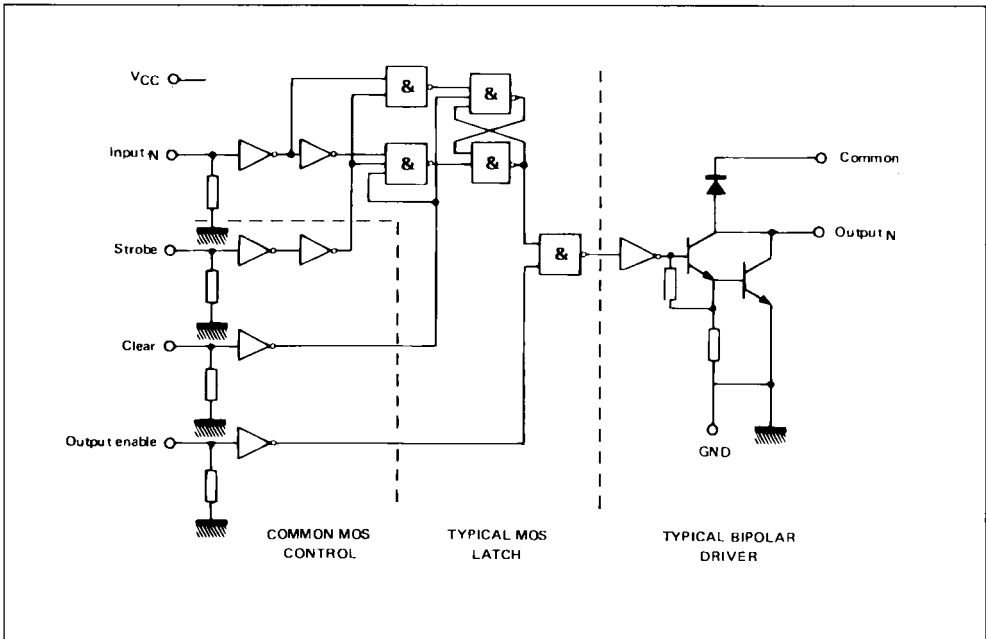
- | | |
|--------------|----------------------|
| 1 - Clear | 22 - Output enable |
| 2 - Strobe | 21 - V _{cc} |
| 3 - Input 1 | 20 - Output 1 |
| 4 - Input 2 | 19 - Output 2 |
| 5 - Input 3 | 18 - Output 3 |
| 6 - Input 4 | 17 - Output 4 |
| 7 - Input 5 | 16 - Output 5 |
| 8 - Input 6 | 15 - Output 6 |
| 9 - Input 7 | 14 - Output 7 |
| 10 - Input 8 | 13 - Output 8 |
| 11 - GND | 12 - Common |

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|-------------------------------------|-------------------------|------|
| V_O | Output Voltage | 50 | V |
| V_{CC} | Supply Voltage | 18 | V |
| V_I | Input Voltage Range | - 0.3 to $V_{CC} + 0.3$ | V |
| I_C | Continuous Collector Current | 500 | mA |
| P_{tot} | Power Dissipation* | 2.0 | W |
| T_{op} | Operating Ambient Temperature Range | - 20 to + 85 | °C |
| T_{stg} | Storage Temperature | - 55 to + 125 | °C |

* Derate at the rate of 20 mW/°C above $T_{amb} = + 25$ °C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS $T_{amb} = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------------------|---|-------------------------|-------------------|-------------------|------------------|
| I_O | Output Leakage Current ($V_O = 50\text{ V}$) $T_{amb} = +25\text{ }^{\circ}\text{C}$ $T_{amb} = +70\text{ }^{\circ}\text{C}$ | - - | - - | 50 100 | μA |
| $V_{O(Sat)}$ | Collector-emitter Saturation Voltage $I_O = 100\text{ mA}$ $I_O = 200\text{ mA}$ $I_O = 350\text{ mA}$, $V_{CC} = 7\text{ V}$ | - - - | 0.9 1.1 1.3 | 1.1 1.3 1.6 | V |
| $V_{I(O)}$ $V_{I(1)}$ | Input Voltage $V_{CC} = 15\text{ V}$ $V_{CC} = 10\text{ V}$ $V_{CC} = 5\text{ V}$ - (note 1) | - 13.5 8.5 3.5 | - - - - | 1 - - - | V |
| R_{IN} | Input Resistance $V_{CC} = 15\text{ V}$ $V_{CC} = 10\text{ V}$ $V_{CC} = 5\text{ V}$ | 50 50 50 | 200 300 600 | - - - | $\text{K}\Omega$ |
| $I_{CC(on)}$ (each stage) | Supply Current - Outputs Open $V_{CC} = 15\text{ V}$ $V_{CC} = 10\text{ V}$ $V_{CC} = 5\text{ V}$ | - - - | 1 0.9 0.7 | 2 1.7 1 | mA |
| $I_{CC(off)}$ | All Drivers off, All Inputs = 0 V | - | 50 | 100 | μA |
| I_R | Clamp Diode Leakage Current ($V_R = 50\text{ V}$) $T_{amb} = +25\text{ }^{\circ}\text{C}$ $T_{amb} = +70\text{ }^{\circ}\text{C}$ | - - | - - | 50 100 | μA |
| V_F | Clamp Diode Forward Voltage $I_F = 350\text{ mA}$ | - | 1.7 | 2 | V |

Note : 1. Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".

TRUTH TABLE

| IN_N | Strobe | Clear | Output Enable | OUT _N | |
|--------|--------|-------|---------------|------------------|-----|
| | | | | t-1 | t |
| 0 | 1 | 0 | 0 | X | OFF |
| 1 | 1 | 0 | 0 | X | ON |
| X | X | 1 | X | X | OFF |
| X | X | X | 1 | X | OFF |
| X | 0 | 0 | 0 | ON | ON |

X = irrelevant

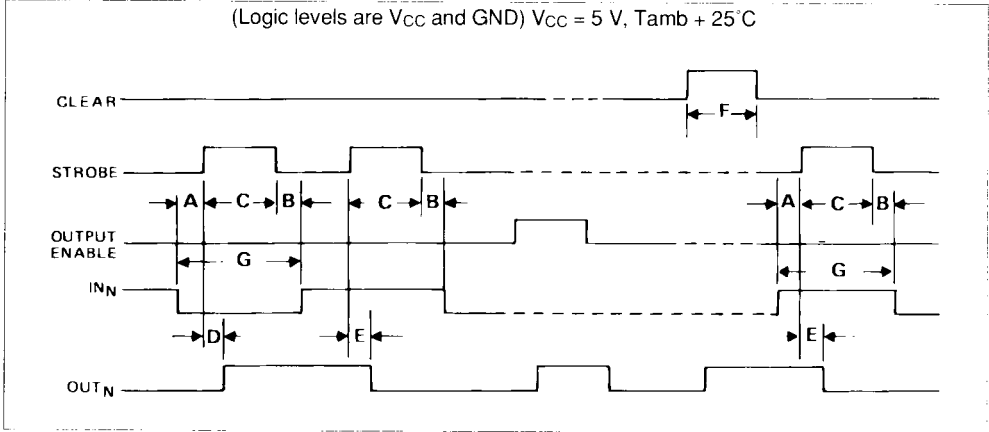
t-1 = previous output state

t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TIMING CONDITIONS

(Logic levels are V_{CC} and GND) V_{CC} = 5 V, T_{amb} + 25°C



- A. Minimum data active time before strobe enabled (data set-up time) 100 ns
- B. Minimum data active time after strobe disabled (data hold time) 100 ns
- C. Minimum strobe pulse width 300 ns
- D. Typical time between strobe activation and output on to off transition 500 ns
- E. Typical time between strobe activation and output off to on transition 500 ns
- F. Minimum clear pulse width 300 ns
- G. Minimum data pulse width 500 ns

