UCS1001

USB Port Power Controller with Charger Emulation

PRODUCT FEATURES

Datasheet

General Description

The UCS1001 provides a USB port power switch for precise control of up to 2.5 amperes continuous current with over-current limit (OCL), dynamic thermal management, latch or auto-recovery (low test current) fault handling, selectable active low or high enable, under- and over-voltage lockout, back-drive protection, and back-voltage protection.

Split supply support for VS and VDD is an option for low power in system standby states. This gives battery operated applications, like notebook PCs, the ability to detect attachments from a sleep or off state. After the Attach Detection is flagged, the system can decide to wake up and/or provide charging.

In addition to power switching and current limiting modes, the UCS1001 will automatically charge a wide variety of portable devices, including USB-IF BC1.2, YD/T-1591 (2009), most Apple® and RIM®, and many others. Nine preloaded charger emulation profiles maximize compatibility coverage of peripheral devices.

The UCS1001 is available in a 20-pin QFN 4 mm x 4 mm package.

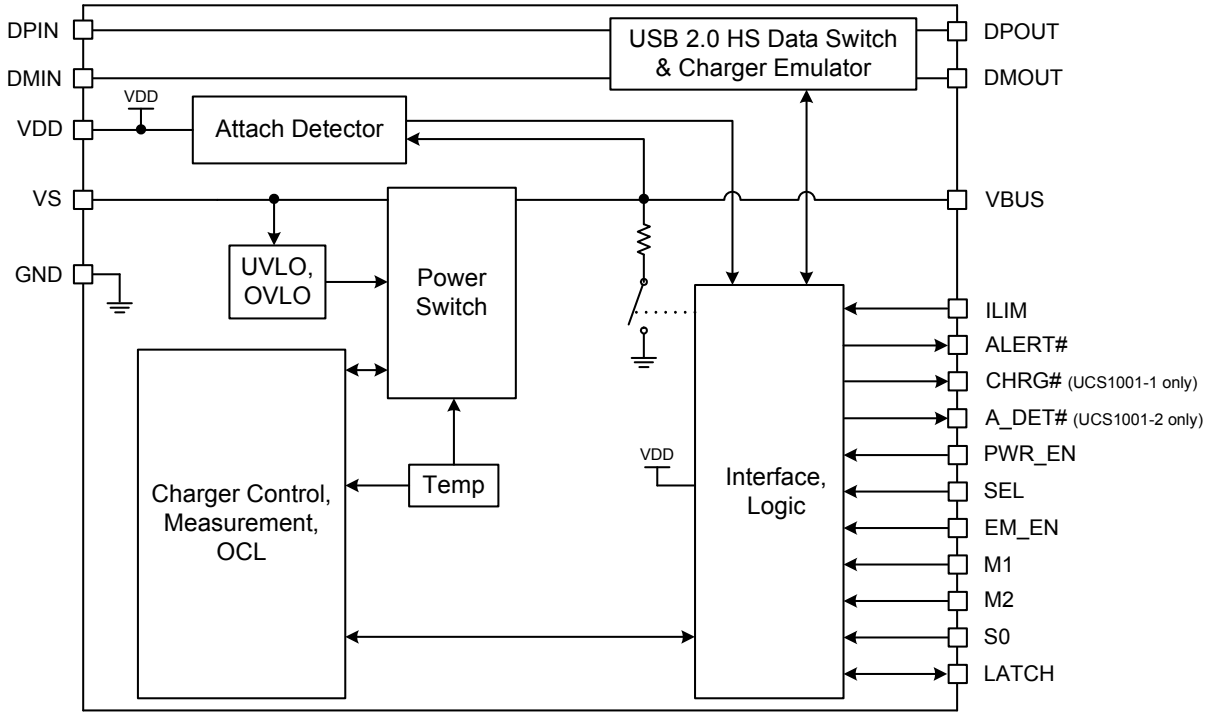
Applications

- Notebook and Netbook Computers
- Tablets and E-book readers
- Desktops and Monitors
- Docking Stations and Printers
- AC-DC wall adapters

Features

- Port power switch with two current limit behaviors
  - 2.9 V to 5.5 V source voltage range
  - Up to 2.5 A current with 55 mΩ On Resistance
  - Over-current trip or constant current limiting
  - Soft turn-on circuitry
  - Selectable current limit
  - Dynamic thermal management
  - Under- and over-voltage lockout
  - Back-drive, back-voltage protection
  - Latch or auto-recovery (low test current) fault handling
  - Selectable active high or low power switch enable
  - BC1.2 VBUS discharge port renegotiation function
- Selectable / automatic cycling of USB data line charger emulation profiles
  - USB-IF BC1.2 charging downstream port (CDP) & dedicated charging port (DCP) modes, YD/T-1591, and most Apple and RIM protocols standard
  - USB 2.0 compliant high-speed data switch (in Pass-through and CDP modes)
  - Nine preloaded charger emulation profiles for maximum compatibility coverage of peripheral devices
- Charging Active (UCS1001-1) or Attach Detection (UCS1001-2) open-drain output
- Fault Alert open-drain output
- Ultra low power Sleep state
- Optional split supply support for VBUS and VDD for low power in system standby states
- Wake on Attach USB (UCS1001-2)
- Wide operating temperature range: -40 °C to +85 °C
- IEC61000-4-2 8 / 15 kV ESD immunity
- UL recognized and EN/IEC 60950-1 (CB) certified

Block Diagram



ORDERING INFORMATION:

ORDERING NUMBER	PACKAGE	FEATURES
UCS1001-1-BP-TR	20 pin QFN 4 mm x 4 mm (Lead Free RoHS compliant)	USB Port Power Controller with Charger Emulation and charging active output indicator
UCS1001-2-BP-TR	20 pin QFN 4 mm x 4 mm (Lead Free RoHS compliant)	USB Port Power Controller with Charger Emulation and portable device attachment detected output indicator

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

Table of Contents

List of Figures

List of Tables

Chapter 1 Terms and Abbreviations

APPLICATION NOTE: The M1, M2, PWR_EN, and EM_EN pins are referenced in text as the <pin name> control.

Table 1.1 Terms and Abbreviations

TERM / ABBREVIATION	DESCRIPTION
Active mode	Active power state operation mode: Data Pass-through, BC1.2 SDP, BC1.2 CDP, BC1.2 DCP, or Dedicated Charger Emulation Cycle.
attachment	The physical insertion of a portable device into a USB port that UCS1001 is controlling.
CC	Constant current
CDM	Charged Device Model. JEDEC model for characterizing susceptibility of a device to damage from ESD.
CDP or USB-IF BC1.2 CDP	Charging downstream port. The combination of the UCS1001 CDP handshake and an active standard USB host comprises a CDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 1.5 A while data communication is active. The USB high-speed data switch is closed in this mode.
charge enable	When a charger emulation profile has been accepted by a portable device and charging commences.
charger emulation profile	Representation of a charger comprised of DPOUT, DMOUT, and VBUS signalling which make up a defined set of signatures or handshaking protocols.
connection	USB-IF term which refers to establishing active USB communications between a USB host and a USB device.
current limiting mode	Determines the action that is performed when the IBUS current reaches the ILIM threshold. Trip opens the port power switch. Constant current (variable slope) allows VBUS to be dropped by the portable device.
DCE	Dedicated charger emulation. Charger emulation in which the UCS1001 can deliver power only. No active USB data communication is possible when charging in this mode.
DCP or USB-IF BC1.2 DCP	Dedicated Charging Port. This functions as a dedicated charger for a BC1.2 portable device. This allows the portable device to draw currents up to 1.5 A with constant current limiting (and beyond 1.5 A with trip current limiting). No USB communications are possible.
DC	Dedicated charger. A charger which inherently does not have USB communications, such as an A/C wall adapter.
disconnection	USB-IF term which refers to the loss of active USB communications between a USB host and a USB device.
dynamic thermal management	The UCS1001 automatically adjusts port power switch limits and modes to lower internal power dissipation when the thermal regulation temperature value is approached.
enumeration	A USB-specific term that indicates that a host is detecting and identifying USB devices.
handshake	Application of a charger emulation profile that requires a response. Two-way communication between the UCS1001 and the portable device.
HBM	Human Body Model.
HSW	High-speed switch.

Table 1.1 Terms and Abbreviations (continued)

TERM / ABBREVIATION	DESCRIPTION
I_{BUS_R2MIN}	Current limiter mode boundary.
ILIM	The IBUS current threshold used in current limiting. In trip mode, when ILIM is reached, the port power switch is opened. In constant current mode, when the current exceeds ILIM, operation continues at a reduced voltage and increased current; if VBUS voltage drops below V_{BUS_MIN}, the port power switch is opened.
Legacy	USB devices that require non-BC1.2 signatures be applied on the DPOUT and DMOUT pins to enable charging.
OCL	Over-current limit.
portable device	USB device attached to the USB port.
power thief	A USB device that does not follow the handshaking conventions of a BC1.2 device or Legacy devices and draws current immediately upon receiving power (i.e., a USB book light, portable fan, etc).
removal	The physical removal of a portable device from a USB port that the UCS1001 is controlling.
SDP or USB-IF SDP	Standard downstream port. The combination of the UCS1001 high-speed switch being closed with an upstream USB host present comprises a BC1.2 SDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 0.5 A while data communication is active.
signature	Application of a charger emulation profile without waiting for a response. One-way communication from the UCS1001 to the portable device.

Chapter 2 Pin Description

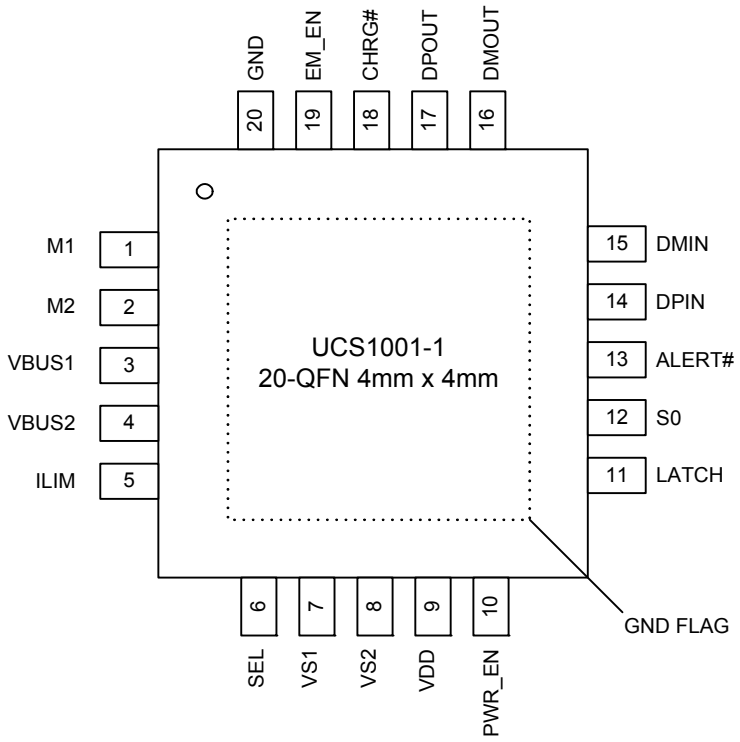


Figure 2.1 UCS1001-1 Pin Diagram

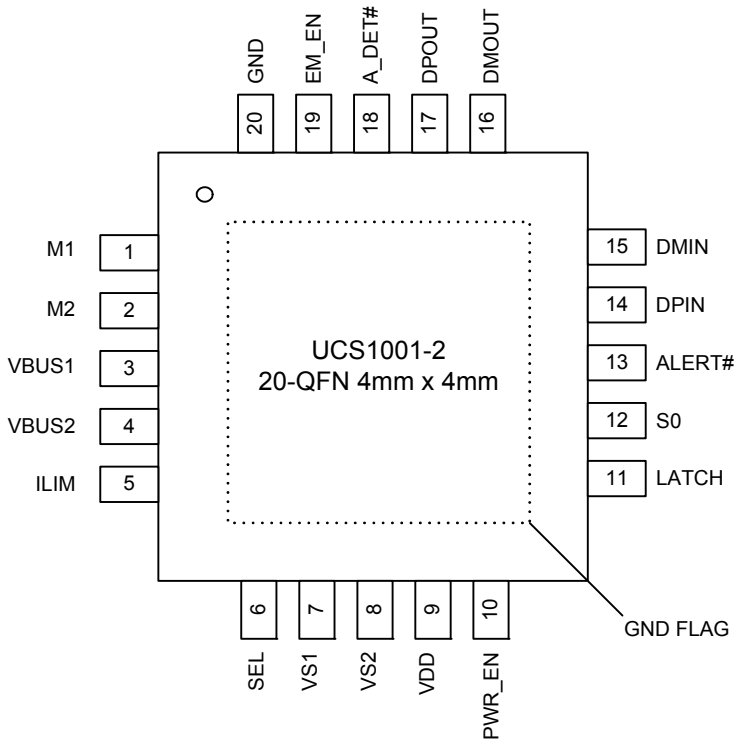


Figure 2.2 UCS1001-2 Pin Diagram

The pin types are described in Table 2.2. All pins are 5 V tolerant.

Table 2.1 UCS1001 Pin Description

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	IF PIN NOT USED CONNECTION
1	M1	Active mode selector input #1	DI	Connect to ground or VDD (see Note 2.2)
2	M2	Active mode selector input #2	DI	Connect to ground or VDD (see Note 2.2)
3	VBUS1	Voltage output from Power Switch. These pins must be tied together.	Hi-Power, AIO Note 2.1	Leave open
4	VBUS2			
5	ILIM	Selects the maximum current limit at power-up (see Table 6.1, "UCS1001 ILIM Selection")	AIO	n/a
6	SEL	Selects polarity of PWR_EN control (see Section 4.3.2, "SEL Input")	DI	n/a

Table 2.1 UCS1001 Pin Description (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE	IF PIN NOT USED CONNECTION
7	VS1	Voltage input to Power Switch. These pins must be tied together.	Hi-Power, AIO	Connect to ground
8	VS2			
9	VDD	Main power supply input for chip functionality	Power	n/a
10	PWR_EN	Port power switch enable input. Polarity determined by SEL pin.	DI	Connect to ground or VDD (see Note 2.2)
11	LATCH	Latch / Auto-recovery fault handling mechanism selection input (see Section 6.5, "Fault Handling Mechanism")	DI	n/a
12	S0	Enables Attach / Removal Detection feature (see Section 4.3.6, "S0 Input")	DI	n/a
13	ALERT#	Active low error event output flag (requires pull-up resistor)	OD	Connect to ground
14	DPIN	USB data input (plus)	AIO	Connect to ground or ground through a resistor
15	DMIN	USB data input (minus)	AIO	Connect to ground or ground through a resistor
16	DMOUT	USB data output (minus)	AIO	Connect to ground
17	DPOUT	USB data output (plus)	AIO	Connect to ground
18 (UCS1001-1)	CHRG#	Active low “Charging Active” output flag (requires pull-up resistor)	OD	Connect to ground
18 (UCS1001-2)	A_DET#	Active low Attach Detection output flag (requires pull-up resistor)	OD	Connect to ground
19	EM_EN	Active mode selector input	DI	Connect to ground or VDD (see Note 2.2)
20	GND	Ground	Power	n/a
Bottom Pad	GND FLAG	Thermal connection to ground plane	Thermal Pad	n/a

Note 2.1 Total leakage current from pins 3 and 4 (VBUS) to ground must be less than 100 µA for proper attach / removal detection operation.

Note 2.2 To ensure operation, the PWR_EN pin must be enabled, as determined by the SEL pin decode, when it is not driven by an external device. Furthermore, one of the M1, M2, or EM_EN pins must be connected to VDD if all three are not driven from an external device. If the PWR_EN is disabled or all of the M1, M2, and EM_EN are connected to ground, the UCS1001 will remain in the Sleep or Detect state indefinitely.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
Hi-Power	This pin is a high current pin.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
DI	Digital Input - this pin is used as a digital input.
OD	Open-drain Digital Output - used as a digital output. It is open-drain and requires a pull-up resistor.

Chapter 3 Electrical Specifications

Table 3.1 Absolute Maximum Ratings

Voltage on VDD, VS, and VBUS pins	-0.3 to 6	V
Pullup voltage (V_{PULLUP})	-0.3 to VDD + 0.3	
Data switch current (I_{HSW_ON}), switch on	±50	mA
Port power switch current	Internally limited	
Data switch pin voltage to ground (DPOUT, DPIN, DMOUT, DMIN); (VDD powered or unpowered)	-0.3 to VDD + 0.3	V
Differential voltage across open data switch (DPOUT - DPIN, DMOUT - DMIN, DPIN - DPOUT, DMIN - DMOUT)	VDD	V
Voltage on any other pin to ground	-0.3 to VDD + 0.3	V
Current on any other pin	±10	mA
Package power dissipation	See Table 3.2	
Operating ambient temperature range	-40 to 125	°C
Storage temperature range	-55 to 150	°C

Note: Stresses above those listed could cause permanent damage to the UCS1001. This is a stress rating only and functional operation of the UCS1001 at any other condition above those indicated in the operation sections of this specification is not implied.

Table 3.2 Power Dissipation Summary

BOARD	PKG	θ_{JC}	θ_{JA}	DERATING FACTOR ABOVE 25 °C	TA < 25 °C POWER RATING	TA = 70 °C POWER RATING	TA = 85 °C POWER RATING
High K (see Note 3.1)	20-pin QFN 4 mm x 4 mm	6 °C / W	41 °C / W	24.4 mW / °C	2193 mW	1095 mW	729 mW
Low K (see Note 3.1)	20-pin QFN 4 mm x 4 mm	6 °C / W	60 °C / W	16.67 mW / °C	1498 mW	748 mW	498 mW

Note 3.1 A High K board uses a thermal via design with the thermal landing soldered to the PCB ground plane with 0.3 mm (12 mil) diameter vias in a 3x3 matrix (9 total) at 0.5 mm (20 mil) pitch. The board is multi-layer with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom. A Low K board is a two layer board without thermal via design with 2-ounce copper traces on the top and bottom.

Table 3.3 Electrical Specifications

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, T_A = -40 °C to 85 °C all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Power and Interrupts - DC						
Supply Voltage	VDD	4.5	5	5.5	V	See Note 3.2
Source Voltage	VS	2.9	5	5.5	V	See Note 3.2
Supply Current in Active (I_{DD_ACTIVE} + I_{VS_ACT})	I_{ACTIVE}		650	750	µA	Average current IBUS = 0 mA
Supply Current in Sleep (I_{DD_SLEEP} + I_{VS_SLEEP})	I_{SLEEP}		5	8	µA	Average current $V_{PULLUP} \leq$ VDD
Supply Current in Detect (I_{DD_DETECT} + I_{VS_DETECT})	I_{DETECT}		185	220	µA	Average current No portable device attached.
Power-on Reset						
VS Low Threshold	V_{S_UVLO}		2.5	2.7	V	VS voltage increasing
VS Low Hysteresis	$V_{S\_UVLO\_HYST}$		100		mV	VS voltage decreasing
VDD Low Threshold	V_{DD_TH}		4	4.4	V	VDD voltage increasing
VDD Low Hysteresis	$V_{DD\_TH\_HYST}$		500		mV	VDD voltage decreasing
I/O Pins - EM_EN, M1, M2, PWR_EN, S0, LATCH, ALERT#, CHRG# (UCS1001-1), A_DET# (UCS1001-2) - DC Parameters						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK_IO} = 8 mA ALERT#, CHRG#, A_DET#
Input High Voltage	V_{IH}	2.0			V	PWR_EN, EM_EN, M1, M2, LATCH, S0
Input Low Voltage	V_{IL}			0.8	V	PWR_EN, EM_EN, M1, M2, EM_EN, LATCH, S0
Leakage Current	I_{LEAK}			±5	µA	Powered or unpowered V_{PULLUP} <= VDD T_A < 85 °C
Interrupt Pins - AC Parameters						
ALERT#, A_DET# (UCS1001-2) Pin Blanking Time	t_{BLANK}		25		ms	
ALERT# Pin Interrupt Masking Time	t_{MASK}		5		ms	

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, T_A = -40 °C to 85 °C all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
High-speed Data Switch						
High-speed Data Switch - DC Parameters						
Switch Leakage Current	I_{HSW_OFF}		±0.5		µA	Switch open - DPIN to DPOUT, DMIN to DMOUT, or all four pins to ground. VDD ≤ VS.
Charger Resistance	R_{CHG}	2			MΩ	DPOUT or DMOUT to VBUS or ground, see Figure 3.2 BC1.2 DCP charger emulation active
On Resistance	R_{ON_HSW}		2		Ω	Switch closed, VDD = 5 V test current = 8 mA, test voltage = 0.4 V, see Figure 3.2
On Resistance	$R_{ON\_HSW\_1}$		5		Ω	Switch closed, VDD = 5 V, test current = 8 mA, test voltage = 3.0 V, see Figure 3.2
Delta On Resistance	ΔR_{ON_HSW}		±0.3		Ω	Switch closed, VDD = 5 V I_{TST} = 8 mA, V_{TST} = 0 to 1.5 V, see Figure 3.2
High-speed Data Switch - AC Parameters						
DP, DM Capacitance to Ground	C_{HSW_ON}		4		pF	Switch closed VDD = 5 V
DP, DM Capacitance to Ground	C_{HSW_OFF}		2		pF	Switch open VDD = 5 V
Turn Off Time	t_{HSW_OFF}		400		µs	Time from state control (EM_EN, M1, M2) switch on to switch off, R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Turn On Time	t_{HSW_ON}		400		µs	Time from state control (EM_EN, M1, M2) switch off to switch on, R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Propagation Delay	t_{PD}		0.25		ns	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Propagation Delay Skew	Δt_{PD}		25		ps	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Rise/Fall Time	$t_{F/R}$		10		ns	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
DP - DM Crosstalk	X_{TALK}		-40		dB	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Off Isolation	O_{IRR}		-30		dB	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF f = 240 MHz

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, T_A = -40 °C to 85 °C all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
-3dB Bandwidth	BW		1100		MHz	R_{TERM} = 50 Ω, C_{LOAD} = 1.5 pF V_{DPOUT} = V_{DMOUT} = 350 mV DC
Total Jitter	t_J		200		ps	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF, rise time = fall time = 500 ps at 480 Mbps (PRBS = 2^{15} - 1)
Skew of Opposite Transitions of the Same Output	$t_{SK(P)}$		20		ps	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF
Port Power Switch						
Port Power Switch - DC Parameter						
Over-voltage Lockout	V_{S_OV}		6		V	
On Resistance	R_{ON_PSW}		55	65	mΩ	4.75 V < VS < 5.25 V
VS Leakage Current	I_{LEAK_VS}		2.2	5	µA	Sleep state into VS pin
Back-voltage Protection Threshold	V_{BV_TH}		150		mV	VBUS > VS VS > V_{S_UVLO}
Back-drive Current	I_{BD_1}		0	3	µA	VDD < V_{DD_TH}, Any powered power pin to any unpowered power pin. Current out of unpowered pin.
	I_{BD_2}		0	2	µA	VDD > V_{DD_TH}, Any powered power pin to any unpowered power pin, except for VDD to VBUS in Detect power state and VS to VBUS in Active power state. Current out of unpowered pin.

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, T_A = -40 °C to 85 °C all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Selectable Current Limits	I_{LIM1}	450	467	500	mA	ILIM Resistor = 47 kΩ (500 mA setting)
	I_{LIM2}	810	839	900	mA	ILIM Resistor = 56 kΩ (900 mA setting)
	I_{LIM3}	900	932	1000	mA	ILIM Resistor = 68 kΩ (1000 mA setting)
	I_{LIM4}	1080	1112	1200	mA	ILIM Resistor = 82 kΩ (1200 mA setting)
	I_{LIM5}	1350	1385	1500	mA	ILIM Resistor = 100 kΩ (1500 mA setting)
	I_{LIM6}	1620	1702	1800	mA	ILIM Resistor = 120 kΩ (1800 mA setting)
	I_{LIM7}	1800	1892	2000	mA	ILIM Resistor = 150 kΩ (2000 mA setting)
	I_{LIM8}	2250	2355	2500	mA	ILIM Resistor = VDD (2500 mA setting)
Thermal Regulation Limit	T_{REG}		110		°C	Die Temperature at which current limit will be reduced
Thermal Regulation Hysteresis	T_{REG_HYST}		10		°C	Hysteresis for t_{REG} functionality. Temperature must drop by this value before ILIM value restored to normal operation
Thermal Shutdown Threshold	T_{TSD}		135		°C	Die Temperature at which port power switch will turn off
Thermal Shutdown Hysteresis	T_{TSD_HYST}		35		°C	After shutdown due to T_{TSD} being reached, die temperature drop required before port power switch can be turned on again
Auto-recovery Test Current	I_{TEST}		190		mA	Portable device attached, VBUS = 0 V, Die temp < T_{TSD}
Auto-recovery Test Voltage	V_{TEST}		750		mV	Portable device attached, VBUS = 0 V before application, Die temp < T_{TSD}
Discharge Impedance	$R_{DISCHARGE}$	100			Ω	

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, T_A = -40 °C to 85 °C all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Port Power Switch - AC Parameters						
Turn On Delay	t_{ON_PSW}		0.75		ms	PWR_EN active toggle to switch on time, VBUS discharge not active
Turn Off Time	$t_{OFF\_PSW\_INA}$		0.75		ms	PWR_EN inactive toggle to switch off time C_{BUS} = 120 µF
Turn Off Time	$t_{OFF\_PSW\_ERR}$		1		ms	Over-current Error, VBUS Min Error, or Discharge Error to switch off C_{BUS} = 120 µF
Turn Off Time	$t_{OFF\_PSW\_ERR}$		100		ns	TSD or Back-drive Error to switch off C_{BUS} = 120 µF
VBUS Output Rise Time	t_{R_BUS}		1.1		ms	Measured from 10% to 90% of VBUS, C_{LOAD} = 220 µF ILIM = 1.0 A
Soft Turn on Rate	$\Delta I_{BUS} / \Delta_t$		100		mA / µs	
Temperature Update Time	t_{DC_TEMP}		200		ms	
Short Circuit Response Time	t_{SHORT_LIM}		1.5		µs	Time from detection of short to current limit applied. No C_{BUS} applied
Short Circuit Detection Time	t_{SHORT}		6		ms	Time from detection of short to port power switch disconnect and ALERT# pin assertion.
Latched Mode Cycle Time	t_{UL}		7		ms	From PWR_EN edge transition from inactive to active to begin error recovery
Auto-recovery Mode Cycle Time	t_{CYCLE}		25		ms	Time delay before error condition check
Auto-recovery Delay	t_{RST}		20		ms	Portable device attached, VBUS must be $\geq V_{TEST}$ after this time
Discharge Time	$t_{DISCHARGE}$		200		ms	Amount of time discharge resistor applied

Table 3.3 Electrical Specifications (continued)

VDD = 4.5 V to 5.5 V, VS = 2.9 V to 5.5 V, V_{PULLUP} = 3 V to 5.5 V, T_A = -40 °C to 85 °C all Typical values at VDD = VS = 5 V, T_A = 27 °C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Port Power Switch Operation With Trip Mode Current Limiting						
Region 2 Current Keep-out	I_{BUS_R2MIN}			0.1	A	
Minimum VBUS Allowed at Output	V_{BUS_MIN}	2.0			V	
Port Power Switch Operation With Constant Current Limiting (Variable Slope)						
Region 2 Current Keep-out	I_{BUS_R2MIN}			1.5	A	
Minimum VBUS Allowed at Output	V_{BUS_MIN}	2.0			V	
VBUS Bypass - DC						
On Resistance	R_{ON_BYP}		50		Ω	
Leakage Current	I_{LEAK_BYP}			3	µA	Switch off
Current Limit	I_{DET_CHG} / I_{BUS_BYP}		2		mA	VDD = 5 V and VBUS> 4.75 V
Allowed Charge Time	t_{DET_CHARGE}		800		ms	C_{BUS} = 500 µF max
Charger Emulation Profile						
General Emulation - DC						
DP-DM Shunt Resistor Value	R_{DCP_RES}			200	Ω	Connected between DPOUT and DMOUT 0 V < DPOUT = DMOUT ≤ 3 V
Voltage Output	SX_RXMAG_VOLT_BC	0.5			V	DMOUT 250 µA load
Pull-down Current	SX_PUPD_ACC_BC	50			µA	DPOUT or DMOUT = 0.15 V Compliance voltage
General Emulation - AC						
Emulation Reset Time	t_{EM_RESET}		50		ms	

Note 3.2 For split supply systems using the Attach Detection feature, VS must not exceed VDD + 150 mV.

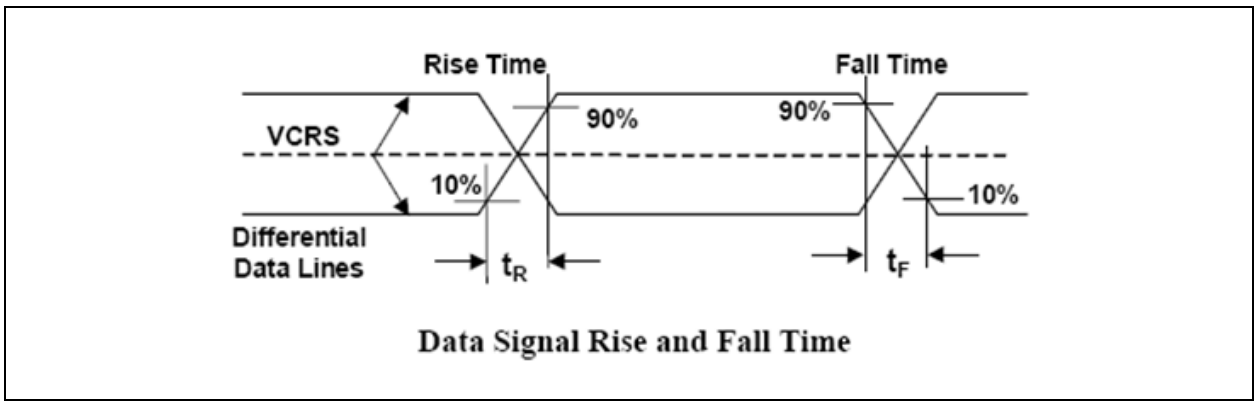


Figure 3.1 USB Rise Time / Fall Time Measurement

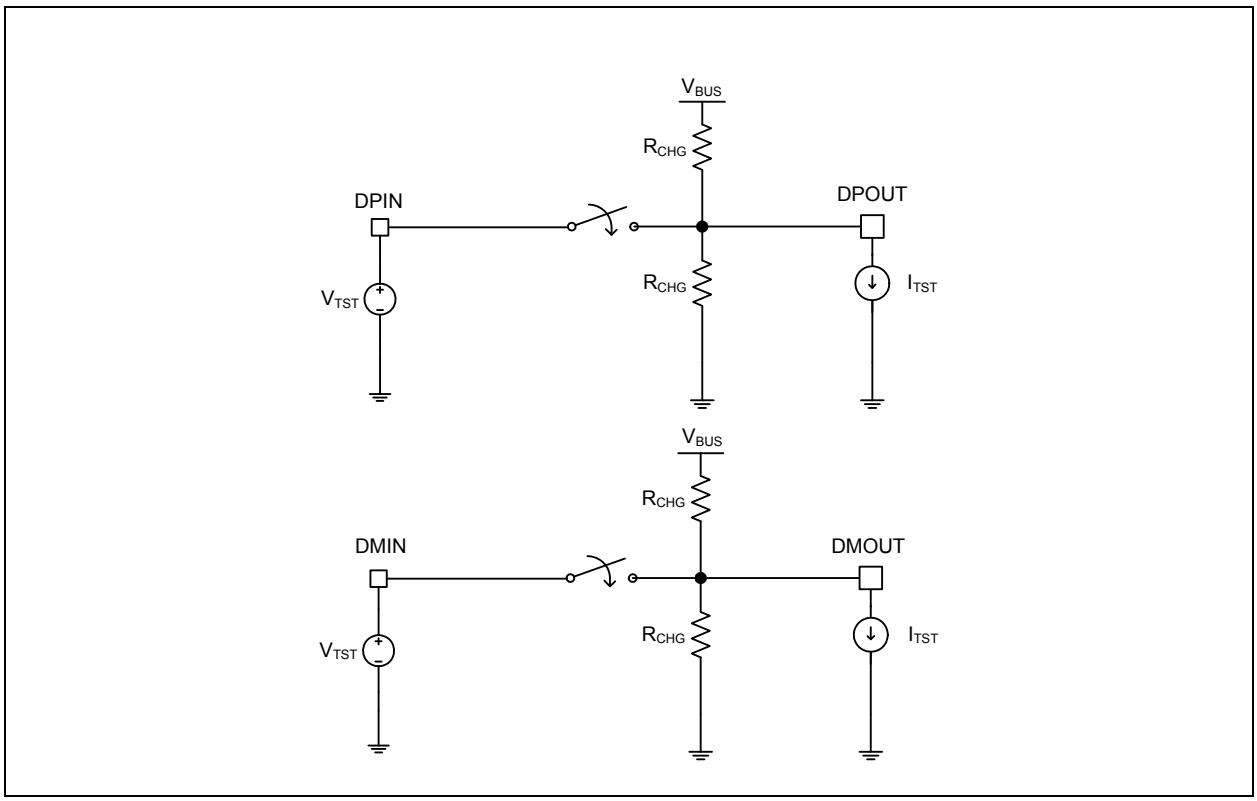


Figure 3.2 Description of DC Terms

3.1 ESD & Transient Performance

APPLICATION NOTE: Depending on the level of ESD protection required by the application, external protection devices may be required. The datasheet ESD levels were reached using external devices and standard USB-A connectors; refer to the EVB schematic and reference design for details.

Table 3.4 ESD Ratings

ESD SPEC	RATING OR VALUE
EN / IEC61000-4-2 (DPOUT, DMOUT pins) air gap, Operational Classification B (see Note 3.3)	Level 4 (15 kV)
EN / IEC61000-4-2 (DPOUT, DMOUT pins) direct contact, Operational Classification B (see Note 3.3)	Level 4 (8 kV)
EN / IEC61000-4-2 (VBUS, GND pins) air gap, Operational Classification A (see Note 3.4)	Level 4 (15 kV)
EN / IEC61000-4-2 (VBUS, GND pins) direct contact, Operational Classification A (see Note 3.4)	Level 4 (8 kV)
Human Body Model (JEDEC JESD22-A114) - All pins	8 kV
Charged Device Model (JEDEC JESD22-C101) - All pins	500 V

Note 3.3 Operational Classification B indicates that during and immediately after an ESD event, anomalous behavior may occur; however, it is non-damaging and the device is self-recovering. All IEC testing is performed using an SMSC evaluation board.

Note 3.4 Operational Classification A indicates that during and immediately after an ESD event no anomalous behavior will occur. All IEC testing is performed using an SMSC evaluation board.

3.1.1 Human Body Model (HBM) Performance

HBM testing verifies the ability to withstand ESD strikes like those that occur during handling and manufacturing and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

3.1.2 Charged Device Model (CDM) Performance

CDM testing verifies the ability to withstand ESD strikes like those that occur during handling and assembly with pick and place style machinery and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event.

3.1.3 IEC61000-4-2 Performance

The IEC61000-4-2 ESD specification is an international standard that addresses system-level immunity to ESD strikes while the end equipment is operational. These tests are performed while the device is powered.

Chapter 4 General Description

The UCS1001 provides a single USB port power switch for precise control of up to 2.5 amperes continuous current with over-current limit (OCL), dynamic thermal management, latch or auto-recovery fault handling, selectable active low or high enable, under- and over-voltage lockout, and back-voltage protection.

Split supply support for VBUS and VDD is an option for low power in system standby states.

In addition to power switching and current limiting, the UCS1001 provides charger emulation profiles to charge a wide variety of portable devices, including USB-IF BC1.2 (CDP or DCP modes), YD/T-1591 (2009), most Apple and RIM portable devices, and many others.

Figure 4.1 shows a system configuration in which the UCS1001-1 provides a port power switch, low power Attach Detection, and charging active signaling. Figure 4.2 shows a system configuration in which the UCS1001-2 provides a port power switch, low power Attach Detection, and portable device Attach Detection signaling. These configurations are useful for applications that already provide USB BC1.2 and/or legacy data line handshaking on the USB data lines, but still require port power switching.

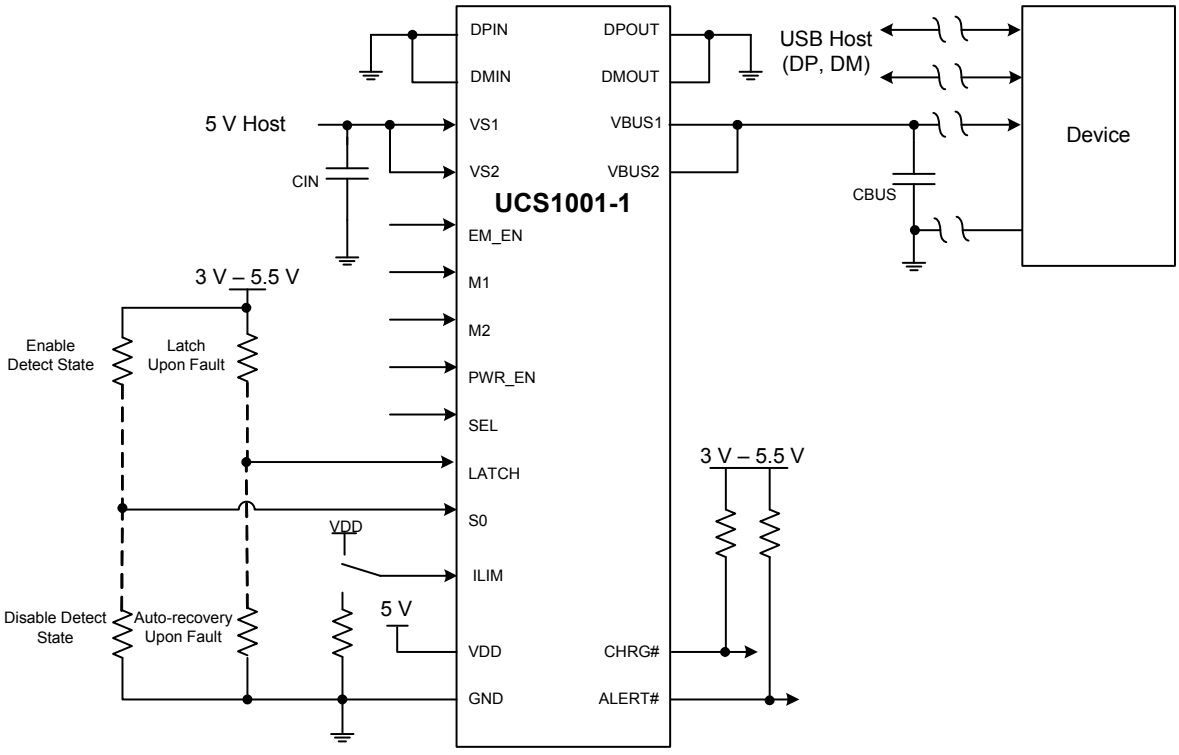


Figure 4.1 UCS1001-1 System Configuration (No Charger Emulation)

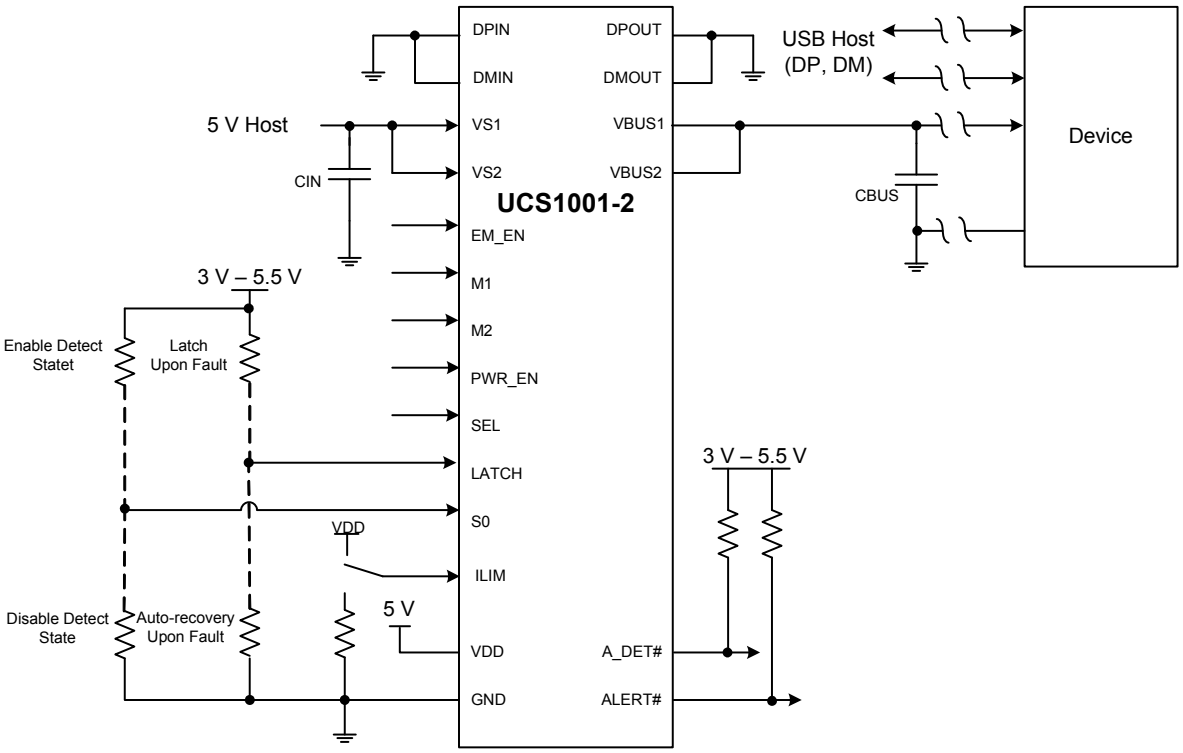


Figure 4.2 UCS1001-2 System Configuration (No Charger Emulation)

Figure 4.3 shows a system configuration in which the UCS1001-1 provides a port power switch, low power Attach Detection, charger emulation (with no USB host), and charging active signaling. Figure 4.4 shows a system configuration in which the UCS1001-2 provides a port power switch, low power Attach Detection, charger emulation (with no USB host), and portable device Attach Detection signaling. These configurations are useful for wall adapter type applications.

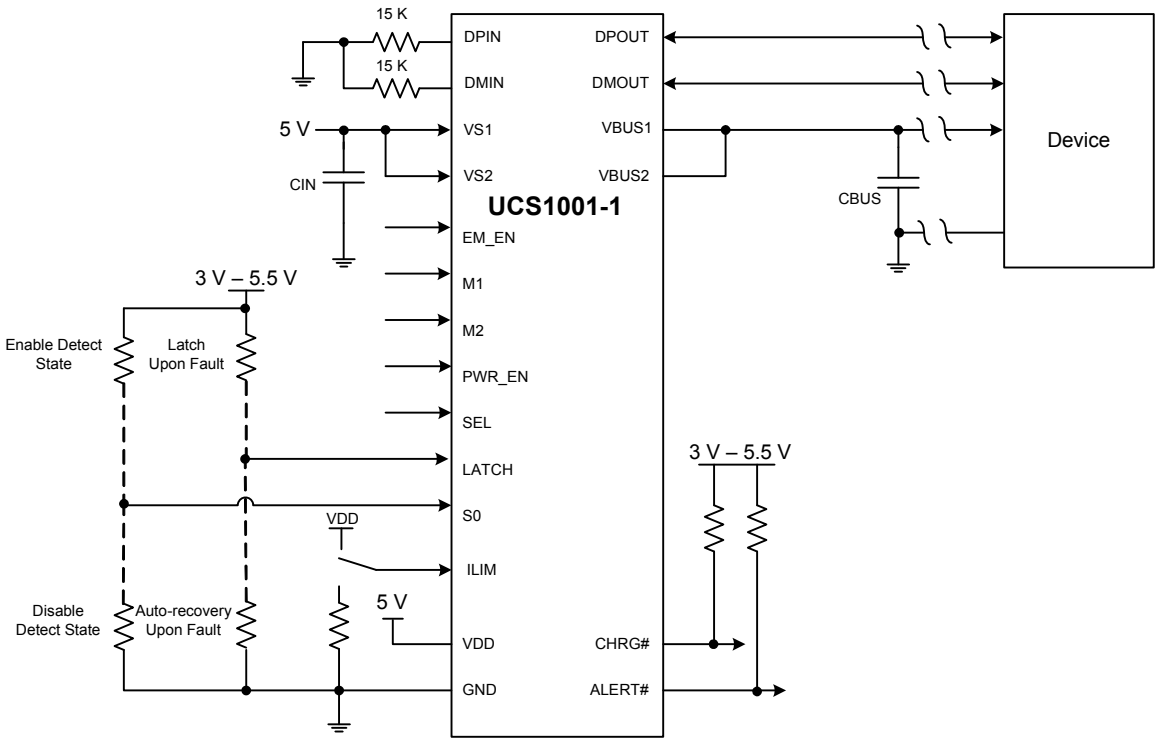


Figure 4.3 UCS1001-1 System Configuration (No USB Host, with Charger Emulation)

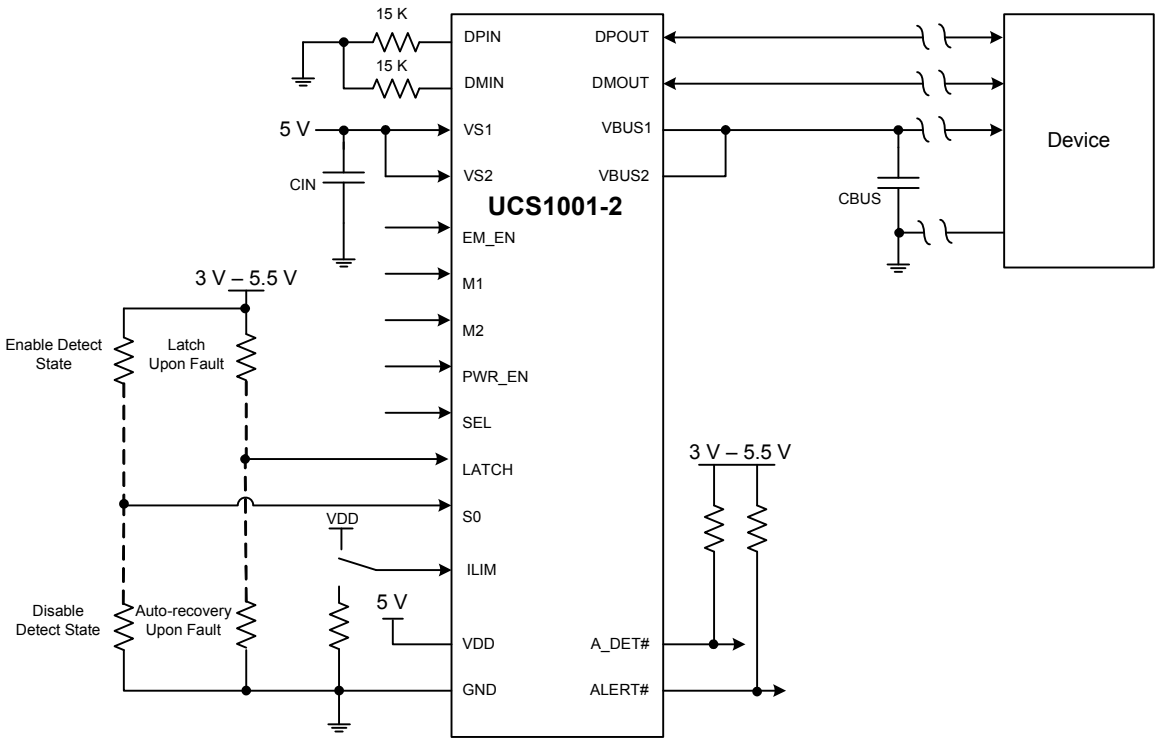


Figure 4.4 UCS1001-2 System Configuration (No USB Host, with Charger Emulation)

4.1 UCS1001 Power States

The UCS1001 has the following power states.

- **Off** - This power state is entered when the voltage at the VDD pin voltage is < V_{DD_TH}. In this state the device is considered “off”. The UCS1001 will not retain its digital states. The port power switch, bypass switch, and the high-speed data switches will be off. See Section 4.1.1, "Off State Operation".
- **Sleep** - This is the lowest power state available. While in this state, the UCS1001 will respond to changes in emulation controls. The high-speed switch and all other functionality will be disabled. See Section 4.1.2, "Sleep State Operation".
- **Detect** - This is a lower current power state. In this state, the device is actively looking for a portable device to be attached. The high-speed switch is disabled. See Section 4.1.3, "Detect State Operation".
- **Error** - This power state is entered when a fault condition exists. See Section 4.1.5, "Error State Operation".
- **Active** - This power state provides full functionality. While in this state, operations include activation of the port power switch, USB data line handshaking / charger emulation, and current limiting. See Section 4.1.4, "Active State Operation".

Table 4.1 shows the settings for the various power states, except Off and Error. If VDD < V_{DD_TH}, the UCS1001 is in the Off state. To determine the mode of operation in the Active state, see Table 8.1, "Active Mode Selection".

APPLICATION NOTE: Using configurations not listed in Table 4.1 is not recommended and may produce undesirable results.

Table 4.1 Power States Control Settings

POWER STATE	VS	PWR_EN	S0	M1, M2, EM_EN	PORTABLE DEVICE ATTACHED	BEHAVIOR
Sleep	X	disabled	0	Not set to Data Pass-through. See Note 4.1.	X	All switches disabled. VBUS will be near ground potential.
	X	enabled	0	All = 0b	X	
Detect (see Chapter 7, Detect State)	X	disabled	1	X	X	High-speed switch disabled. Port power switch disabled. Host-controlled transition to Active state (see Section 4.1.3.2, "Host-Controlled Transition from Detect to Active").
	< V_{S_UVLO}	enabled	1	All <> 0b	X	
	> V_{S_UVLO}	enabled	1	All <> 0b	No	High-speed switch disabled. Automatic transition to Active state when conditions met (see Section 4.1.3.1, "Automatic Transition from Detect to Active").
Active (see Chapter 8, Active State)	> V_{S_UVLO}	enabled	0	All <> 0b and not set to DCE Cycle	X	High-speed switch enabled / disabled based on mode. Port power switch is on at all times. Attach and Removal Detection disabled.
				Set to DCE Cycle	X	High-speed switch disabled. Port power switch is on at all times. Attach and Removal Detection disabled. See Note 4.2.
	> V_{S_UVLO}	enabled	1	All <> 0b	Yes	Port power switch is on. Removal Detection enabled.

Note 4.1 In order to transition from Active state Data Pass-through mode into Sleep with these settings, change the M1, M2, and EM_EN pins before changing the PWR_EN pin. See Section 8.4, "Data Pass-through (No Charger Emulation)".

Note 4.2 If S0='0' and a portable device is not attached in DCE Cycle mode, the UCS1001 will be cycling through charger emulation profiles. There is no guarantee which charger emulation profile will be applied first when a portable device attaches.

4.1.1 Off State Operation

The device will be in the off state if VDD is less than V_{DD_TH}. When the UCS1001 is in the Off state, it will do nothing, and all circuitry will be disabled.

4.1.2 Sleep State Operation

When the UCS1001 is in the Sleep state, the device will be in its lowest power state. The high-speed switch, bypass switch, and the port power switch will be disabled. The Attach and Removal Detection feature will be disabled. VBUS will be near ground potential. The ALERT# pin will not be asserted. If asserted prior to entering the Sleep state, the ALERT# pin will be released. The A_DET# pin (UCS1001-2 only) will be released.

Figure 4.5 shows timing diagrams for waking the UCS1001.

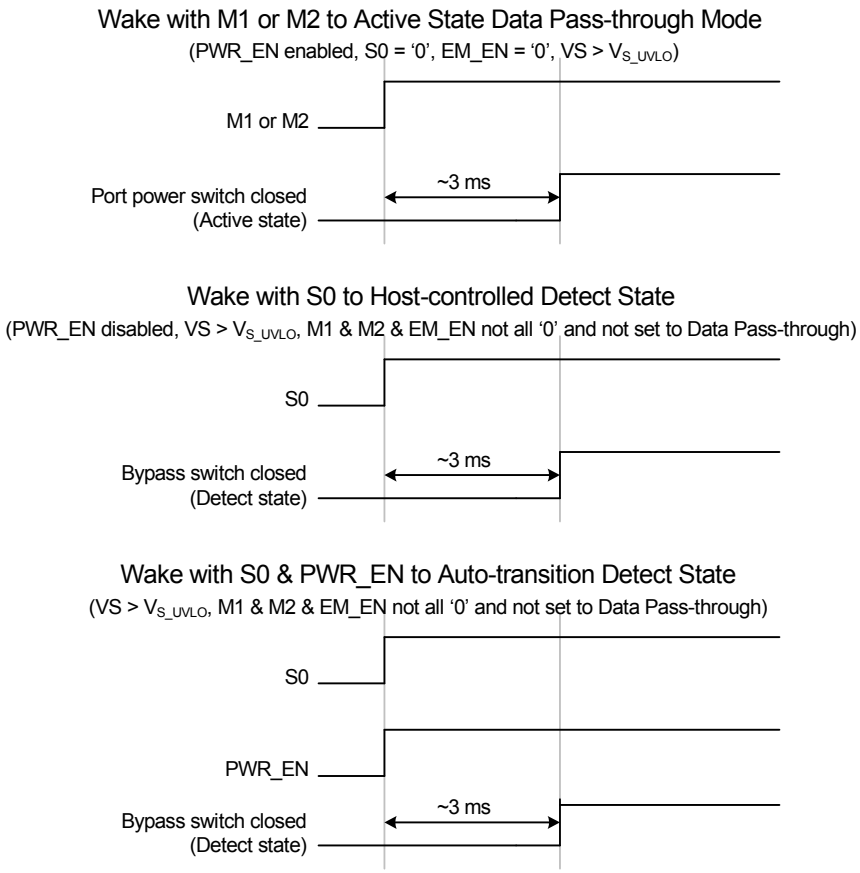


Figure 4.5 Wake Timing

4.1.3 Detect State Operation

When the UCS1001 is in the Detect state, the port power switch will be disabled. The high-speed switch is also disabled. The VBUS output will be connected to the VDD voltage by a secondary bypass switch (see Chapter 7, Detect State).

There is one **non-recommended** configuration which places the UCS1001 in the Detect state, but V_{BUS} will not be discharged and a portable device attachment will not be detected. For the recommended configurations, see Table 4.1, "Power States Control Settings".

- **NOT RECOMMENDED:** PWR_EN is enabled, S0 = ‘1’, and M1, M2, and EM_EN are all ‘0’.

There are two methods for transitioning from the Detect state to the Active state: automatic and host-controlled.

4.1.3.1 Automatic Transition from Detect to Active

For the Detect state, set S0 to ‘1’, enable PWR_EN, set the EM_EN, M1, and M2 controls to the desired Active mode (Table 8.1, "Active Mode Selection"), and supply VS > V_{S_UVLO}. When a portable device is attached and an Attach Detection event occurs, the UCS1001 will automatically transition to the Active state and operate according to the selected Active mode.

4.1.3.2 Host-Controlled Transition from Detect to Active

For the Detect state, set S0 to ‘1’, set the EM_EN, M1, and M2 controls to the desired Active mode (Table 8.1, "Active Mode Selection"), and configure one of the following: 1) disable PWR_EN and supply VS, or 2) enable PWR_EN and don’t supply VS. When a portable device is attached and an Attach Detection event occurs, the host must respond to transition to the Active state. Depending on the control settings in the Detect state, this could entail 1) enabling PWR_EN or 2) supplying VS above the threshold.

APPLICATION NOTE: If S0 is '1', PWR_EN is enabled, and VS is not present, the A_DET# pin will cycle if the current draw exceeds the current capacity of the bypass switch.

4.1.3.3 State Change from Detect to Active

When conditions cause the UCS1001 to transition from the Detect state to the Active state, the following occurs:

1. The Attach Detection feature will be disabled; the Removal Detection feature remains enabled, unless S0 is changed to ’0’.
2. The bypass switch will be turned off.
3. The discharge switch will be turned on briefly.
4. The port power switch will be turned on.

4.1.4 Active State Operation

Every time that the UCS1001 enters the Active state and the port power switch is closed, it will enter the mode as instructed by the host controller (see Chapter 8, Active State). The UCS1001 cannot be in the Active state (and therefore, the port power switch cannot be turned on) if any of the following conditions exist:

1. VS < V_{S_UVLO}.
2. PWR_EN is disabled.
3. M1, M2, and EM_EN are all set to '0'.
4. S0 is set to ‘1’ and an Attach Detection event has not occurred.

4.1.5 Error State Operation

The UCS1001 will enter the Error state from the Active state when any of the following events are detected:

1. The maximum allowable internal die temperature (T_{TSD}) has been exceeded (see Section 6.3.1.2).
2. An over-current condition has been detected (see Section 6.2.1).
3. An under-voltage condition on VBUS has been detected (see Section 4.2.5).
4. A back-drive condition has been detected (see Section 4.2.3).
5. A discharge error has been detected (see Section 6.4).
6. An over-voltage condition on the VS pins.

The UCS1001 will enter the Error state from the Detect state when a back-drive condition has been detected or when the maximum allowable internal die temperature has been exceeded.

The UCS1001 will enter the Error state from the Sleep state when a back-drive condition has been detected.

When the UCS1001 enters the Error state, the port power switch, the VBUS bypass switch, the high-speed switch are turned off, and the ALERT# pin is asserted. They will remain off while in this power state. The UCS1001 will leave this state as determined by the fault handling selection (see Section 6.5, "Fault Handling Mechanism").

When using the Latch fault handler and the user has re-activated the device by or toggling the PWR_EN control, the UCS1001 will check that all of the error conditions have been removed. If using Auto-recovery fault handler, after the t_{CYCLE} time period, the UCS1001 will check that all of the error conditions have been removed.

If all of the error conditions have been removed, the UCS1001 will return to the Active state or Detect state, as applicable. Returning to the Active state will cause the UCS1001 to restart the selected mode (see Section 8.2, "Active Mode Selection").

If the device is in the Error state and a Removal Detection event occurs, it will check the error conditions and then return to the power state defined by the PWR_EN, M1, M2, EM_EN, and S0 controls.

4.2 Supply Voltages

4.2.1 VDD Supply Voltage

The UCS1001 requires 4.5 V to 5.5 V present on the VDD pin for core device functionality.

4.2.2 VS Source Voltage

VS can be a separate supply and can be greater than VDD to accommodate high current applications in which current path resistances result in unacceptable voltage drops that may prevent optimal charging of some portable devices.

4.2.3 Back-voltage Detection

Whenever the following conditions are true, the port power switch will be disabled, the VBUS bypass switch will be disabled, the high-speed data switch will be disabled, and a Back-voltage event will be flagged. This will cause the UCS1001 to enter the Error power state (see Section 4.1.5, "Error State Operation").

1. The VBUS voltage exceeds the VS voltage by V_{BV_TH} and the port power switch is closed. The port power switch will be opened immediately. If the condition lasts for longer than t_{MASK}, then the UCS1001 will enter the Error state. Otherwise, the port power switch will be turned on as soon as the condition is removed.
2. The VBUS voltage exceeds the VDD voltage by V_{BV_TH} and the VBUS bypass switch is closed. The bypass switch will be opened immediately. If the condition lasts for longer than t_{MASK}, then the UCS1001 will enter the Error state. Otherwise, the bypass switch will be turned on as soon as the condition is removed.

4.2.4 Back-drive Current Protection

If a portable device is attached that is self-powered, it may drive the VBUS port to its power supply voltage level; however, the UCS1001 is designed such that leakage current from the VBUS pins to the VDD or VS pins shall not exceed I_{BD_1} (if the VDD voltage is zero) or I_{BD_2} (if the VDD voltage exceeds V_{DD_TH}).

4.2.5 Under-voltage Lockout on VS

The UCS1001 requires a minimum voltage (V_{S_UVLO}) be present on the VS pin for Active power state.

4.2.6 Over-voltage Detection and Lockout on VS

The UCS1001 port power switch will be disabled if the voltage on the VS pin exceeds a voltage (V_{S_OV}) for longer than the specified time (t_{MASK}). This will cause the device to enter the Error state.

4.3 Discrete Input Pins

APPLICATION NOTE: If it is necessary to connect any of the control pins except the ILIM or SEL pins via a resistor to VDD or GND, the resistor value should not exceed 100 kΩ in order to meet the VIH and VIL specifications.

4.3.1 ILIM Input

The ILIM input determines the initial ILIM setting, as shown in Table 6.1, "UCS1001 ILIM Selection".

4.3.2 SEL Input

The SEL pin selects the polarity of the PWR_EN control. If the SEL pin is high, the PWR_EN control is active high enable. If the SEL pin is low, the PWR_EN control is active low enable. This pin state is latched upon device power-up and further changes will have no effect on the PWR_EN control polarity.

APPLICATION NOTE: If it is necessary to connect the SEL pin to ground via a resistor, a value less than 33kΩ must be used. If it is necessary to connect the SEL pin to VDD via a resistor, the pull-up resistor may be any value up to 100 kΩ.

4.3.3 M1, M2, and EM_EN Inputs

The M1, M2, and EM_EN input controls determine the Active mode and affect the power state (see Table 4.1, "Power States Control Settings" and Table 8.1, "Active Mode Selection"). When these controls are all set to ‘0’ and PWR_EN is enabled, the UCS1001 Attach and Removal Detection feature is disabled.

4.3.4 PWR_EN Input

The PWR_EN control enables the port power switch to be turned on if conditions are met and affects the power state (see Table 4.1, "Power States Control Settings"). The port power switch cannot be closed if PWR_EN is disabled. However, if PWR_EN is enabled, the port power switch is not necessarily closed (see Section 4.1.4, "Active State Operation"). Polarity is controlled by the SEL pin.

4.3.5 Latch Input

The Latch input control determines the behavior of the fault handling mechanism (see Section 6.5, "Fault Handling Mechanism").

4.3.6 S0 Input

The S0 control enables the Attach and Removal Detection feature and affects the power state (see Table 4.1, "Power States Control Settings"). When S0 is set to ‘1’, an Attach Detection event must occur before the port power switch can be turned on. When S0 is set to ‘0’, the Attach and Removal Detection feature is not enabled.

4.4 Discrete Output Pins

4.4.1 ALERT#, CHRG#, and A_DET# Output Pins

The ALERT# pin is an active low open-drain interrupt to the host controller. The ALERT# pin is asserted when an error occurs (see Section 4.1.5, "Error State Operation"). The ALERT# pin is released when all error conditions have been removed.

The CHRG# pin (UCS1001-1 only) provides an active low open-drain output indication that charging of an attached device is active. It will remain asserted until this condition no longer exists and then will be automatically released.

The A_DET# pin (UCS1001-2 only) provides an active low open-drain output indication that a valid Attach Detection event has occurred. It will remain asserted until the UCS1001 is placed into the Sleep state or a Removal Detection event occurs. For wake on USB, the A_DET# pin assertion can be utilized by the system. If the S0 control is ‘0’ and the UCS1001 is in the Active state, the A_DET# pin will be asserted regardless if a portable device is attached or not. If S0 is '1', PWR_EN is enabled, and VS is not present, the A_DET# pin will cycle if the current draw exceeds the current capacity of the bypass switch.

4.4.2 Interrupt Blanking

The ALERT#, CHRG# (UCS1001-1 only), and A_DET# (UCS1001-2 only) pins will not be asserted for a specified time (up to t_{BLANK}) after power-up. Additionally, an error condition (except for the thermal shutdown) must be present for longer than a specified time (t_{MASK}) before the ALERT# pin is asserted.

Chapter 5 USB High-speed Data Switch

5.1 USB High-speed Data Switch

The UCS1001 contains a series USB 2.0 compliant high-speed switch between the DPIN and DMIN pins and between the DPOUT and DMOUT pins. This switch is designed for high-speed, low latency functionality to allow USB 2.0 full-speed and high-speed communications with minimal interference.

Nominally, the switch is closed in the Active state, allowing uninterrupted USB communications between the upstream host and the portable device. The switch is opened when:

1. The UCS1001 is actively emulating using any of the charger emulation profiles except CDP.
2. The UCS1001 is operating as a dedicated charger.
3. The UCS1001 is in the Detect state or in the Sleep state.

APPLICATION NOTE: If the VDD voltage is less than V_{DD_TH}, the high-speed data switch will be disabled and opened.

5.1.1 USB-IF High-speed Compliance

The USB data switch will not significantly degrade the signal integrity through the device DP / DM pins with USB high-speed communications.

Chapter 6 USB Port Power Switch

6.1 USB Port Power Switch

To assure compliance to various charging specifications, the UCS1001 contains a USB port power switch that supports two current limiting modes: trip and constant current (variable slope). The current limit (ILIM) is pin selectable. The switch also includes soft start circuitry and a separate short circuit current limit.

The port power switch is on in the Active state (except when VBUS is discharging).

6.2 Current Limiting

6.2.1 Current Limit Setting

The UCS1001 hardware set current limit, ILIM, can be one of eight values (see Table 6.1). This resistor value is read once upon UCS1001 power-up. Unless connected to VDD, the resistors in Table 6.1 are pull-down resistors.

APPLICATION NOTE: If it is necessary to connect the ILIM pin to VDD via a pull-up resistor, it is recommended that this resistor value not exceed 100 kΩ.

APPLICATION NOTE: ILIM pin pull-down resistors with values less than 33 kΩ will cause unexpected behavior.

Table 6.1 UCS1001 ILIM Selection

ILIM RESISTOR (±5%)	ILIM SETTING
47 kΩ	500 mA
56 kΩ	900 mA
68 kΩ	1000 mA
82 kΩ	1200 mA
100 kΩ	1500 mA
120 kΩ	1800 mA
150 kΩ	2000 mA
VDD	2500 mA

6.2.2 Short Circuit Output Current Limiting

Short circuit current limiting occurs when the output current is above the selectable current limit (I_{LIMx}). This event will be detected and the current will immediately be limited (within t_{SHORT_LIM} time). If the condition remains, the port power switch will flag an Error condition and enter the Error state (see Section 4.1.5, "Error State Operation").

6.2.3 Soft Start

When the PWR_EN control changes states to enable the port power switch, or an Attach Detection event occurs in the Detect power state and the PWR_EN control is already enabled, the UCS1001 invokes a soft start routine for the duration of the VBUS rise time (t_{R_BUS}). This soft start routine will limit current flow from VS into VBUS while it is active. This circuitry will prevent current spikes due to a step in the portable device current draw.

In the case when a portable device is attached while the PWR_EN pin is already enabled, if the bus current exceeds ILIM, the UCS1001 current limiter will respond within a specified time (t_{SHORT_LIM}) and will operate normally at this point. The C_{BUS} capacitor will deliver the extra current, if any, as required by the load change.

6.2.4 Current Limiting Modes

The UCS1001 current limiting has two modes: trip and constant current (variable slope). Either mode functions at all times when the port power switch is closed. The current limiting mode used depends on the Active state mode (see Section 8.9, "Current Limit Mode Associations"). When operating in the Detect power state (see Section 4.1.3), the current capacity at VBUS is limited to I_{BUS_BYP} as described in Section 7.2, "VBUS Bypass Switch".

6.2.4.1 Trip Mode

When using trip current limiting, the UCS1001 USB port power switch functions as a low resistance switch and rapidly turns off if the current limit is exceeded. While operating using trip current limiting, the VBUS output voltage will be held relatively constant (equal to the VS voltage minus the R_{ON} * IBUS current) for all current values up to the ILIM.

If the current drawn by a portable device exceeds ILIM, the following occurs:

1. The port power switch will be turned off (trip action).
2. The UCS1001 will enter the Error state and assert the ALERT# pin.
3. The fault handling circuitry will then determine subsequent actions.

Trip current limiting is used when the UCS1001 is in Data Pass-through and Dedicated Charger Emulation Cycle (except when the BC1.2 DCP or Legacy 2 charger emulation profile is accepted), and when there's no handshake.

APPLICATION NOTE: To avoid cycling in trip mode, set ILIM higher than the highest expected portable device current draw.

Figure 6.1 shows operation of current limits in trip mode with the shaded area representing the USB 2.0 specified VBUS range. Dashed lines indicate the port power switch output will go to zero (e.g., trip) when ILIM is exceeded. Note that operation at all possible values of ILIM are shown in Figure 6.1 for illustrative purposes only; in actual operation only one ILIM can be active at any time.

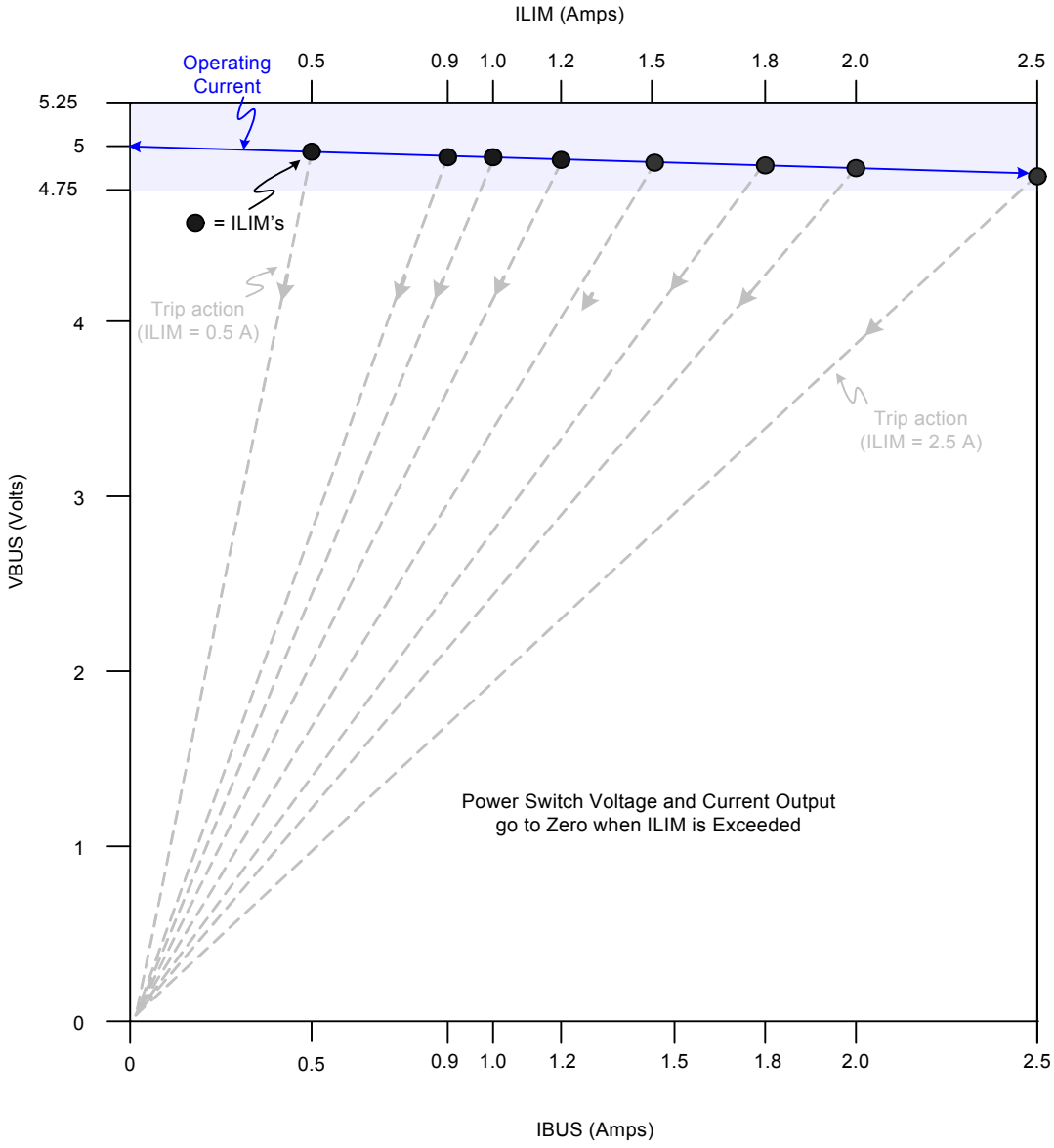


Figure 6.1 Trip Current Limiting Operation

6.2.4.2 Constant Current Limiting (Variable Slope)

Constant current limiting is used when a portable device handshakes using the BC1.2 DCP or Legacy 2 charger emulation profiles and the current drawn is greater than ILIM (and ILIM $\leq$ 1.5 A). It's also used in BC1.2 CDP mode and during the DCE Cycle when a charger emulation profile is being applied and the timeout is active.

In CC mode, the port power switch allows the attached portable device to reduce VBUS output voltage to less than the input VS voltage while maintaining current delivery. The V/I slope depends on the user set ILIM value. This slope is held constant for a given ILIM value.

Figure 6.2 shows operation of current limits while using CC mode. Unlike trip mode, once IBUS current exceeds ILIM, operation continues at a reduced voltage and increased current. Note that the shaded area representing the USB 2.0 specified VBUS range is now restricted to an upper current limit of I_{BUS_R2MIN}. Note that the UCS1001 will heat up along each load line as voltage decreases. If the internal temperature exceeds the T_{REG} or T_{TSD} thresholds, the port power switch will open. Also note that when the VBUS voltage is brought low enough, the port power switch will open.

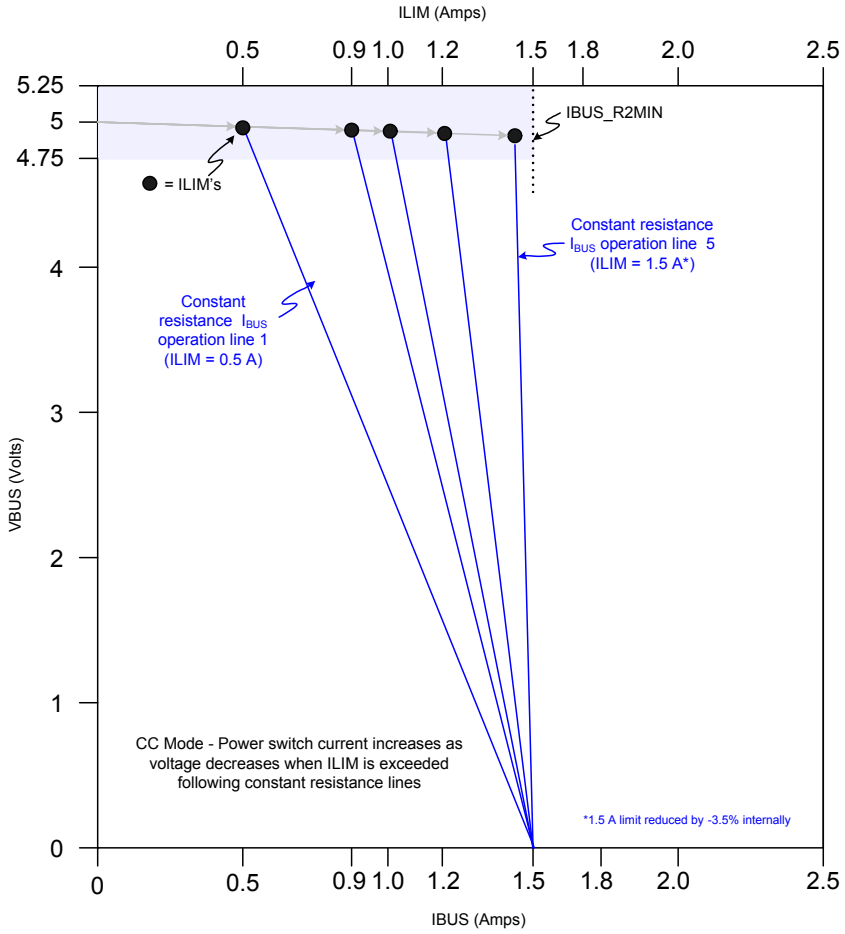


Figure 6.2 Constant Current Limiting (Variable Slope) Operation

6.3 Thermal Management and Voltage Protection

6.3.1 Thermal Management

The UCS1001 utilizes two-stage internal thermal management. The first is named dynamic thermal management and the second is a fixed thermal shutdown.

6.3.1.1 Dynamic Thermal Management

For the first stage (active in both current limiting modes), referred to as dynamic thermal management, the UCS1001 automatically adjusts port power switch limits and modes to lower power dissipation when the thermal regulation temperature value is approached, as described below.

If the internal temperature exceeds the T_{REG} value, the port power switch is opened, the current limit (ILIM) will be lowered by one step and a timer is started (t_{DC_TEMP}). When this timer expires, the port power switch is closed and the internal temperature will be checked again. If it remains above the T_{REG} threshold, the UCS1001 will repeat this cycle (open port power switch and reduce the ILIM setting by one step) until ILIM reaches its minimum value.

APPLICATION NOTE: If the temperature exceeds the TREG threshold while operating in the DCE Cycle mode after a charger emulation profile has been accepted, the profile will be removed. The UCS1001 will not restart the DCE Cycle until one of the control inputs changes states to restart emulation.

APPLICATION NOTE: The UCS1001 will not actively discharge VBUS as a result of the temperature exceeding TREG; however, any load current provided by a portable device or other load will cause VBUS to be discharged when the port power switch is opened, possibly resulting in an attached portable device resetting.

If the UCS1001 is operating using constant current limiting (variable slope) and the ILIM setting has been reduced to its minimum set point and the temperature is still above T_{REG}, the UCS1001 will switch to operating using trip current limiting. This will be done by reducing the I_{BUS_R2MIN} setting to 100 mA and restoring the ILIM setting to the value immediately below the programmed setting (e.g., if the programmed ILIM is 1.8 A, the value will be set to 1.5 A). If the temperature continues to remain above T_{REG}, the UCS1001 will continue this cycle (open the port power switch and reduce the ILIM setting by one step).

If the UCS1001 internal temperature drops below T_{REG} - T_{REG_HYST}, the UCS1001 will take action based on the following:

1. If the current limit mode changed from CC mode to trip mode, then a timer is started. When this timer expires, the UCS1001 will reset the port power switch operation to its original configuration allowing it to operate using constant current limiting (variable slope).
2. If the current limit mode did not change from CC mode to trip mode, or was already operating in trip mode, the UCS1001 will reset the port power switch operation to its original configuration.

If the UCS1001 is operating using trip current limiting and the ILIM setting has been reduced to its minimum set point and the temperature is above T_{REG}, the port power switch will be closed and the current limit will be held at its minimum setting until the temperature drops below T_{REG} - T_{REG_HYST}.

6.3.1.2 Thermal Shutdown

The second stage thermal management consists of a hardware implemented thermal shutdown corresponding to the maximum allowable internal die temperature (T_{TSD}). If the internal temperature exceeds this value, the port power switch will immediately be turned off until the temperature is below T_{TSD} - T_{TSD_HYST}.

6.4 VBUS Discharge

The UCS1001 will discharge V_{BUS} through an internal 100 Ω resistor when at least one of the following conditions occurs:

- The PWR_EN control is disabled (triggered on the inactive edge of the PWR_EN control).
- A portable device Removal Detection event is flagged.
- The VS voltage drops below a specified threshold (V_{S_UVLO}) that causes the port power switch to be disabled.
- When commanded into the Sleep power state via the EM_EN, M1, and M2 controls.
- Before each charger emulation profile is applied.
- Upon recovery from the Error state.
- Any time that the port power switch is activated after the VBUS bypass switch has been on (i.e., whenever VBUS voltage transitions from being driven from VDD to being driven from VS, such as going from Detect to Active power state).
- Any time that the VBUS bypass switch is activated after the port power switch has been on (i.e., going from Active to Detect power state).

When the VBUS discharge circuitry is activated, the UCS1001 will confirm that VBUS was discharged. If the VBUS voltage is not below the V_{TEST} level, a discharge error will be flagged and the UCS1001 will enter the Error state.

6.5 Fault Handling Mechanism

The UCS1001 has two modes for handling faults: Latch (latch-upon-fault) or Auto-recovery (automatically attempt to restore the Active power state after a fault occurs). The fault handling mechanism used depends on the state of the LATCH pin. Faults include over-current, over-voltage (on VS), under-voltage (on VBUS), back-voltage (VBUS to VS or VBUS to VDD), discharge error, and maximum allowable internal die temperature (T_{TSD}) exceeded (see Section 4.1.5, "Error State Operation").

6.5.1 Auto-recovery Fault Handling

When the LATCH pin is low, auto-recovery fault handling is used. When an error condition is detected, the UCS1001 will immediately enter the Error state and assert the ALERT# pin (see Section 4.1.5). Independently from the host controller, the UCS1001 will wait a preset time (t_{CYCLE}), check error conditions (t_{TST}), and restore Active operation if the error condition(s) no longer exist. The ALERT# pin will be released.

6.5.2 Latched Fault Handling

When the LATCH pin is high, latch fault handling is used. When an error condition is detected, the UCS1001 will enter the Error power state and assert the ALERT# pin. Upon command from the host controller (by toggling the PWR_EN pin from enabled to disabled), the UCS1001 will check error conditions once and restore Active operation if error conditions no longer exist. If an error condition still exists, the host controller is required to issue the command again to check error conditions.

Chapter 7 Detect State

7.1 Device Attach / Removal Detection

The UCS1001 can detect the attachment and removal of a portable device on the USB port. Attach and Removal Detection does not perform any charger emulation or qualification of the device. The high-speed switch is “off” during the Detect power state.

7.2 VBUS Bypass Switch

In the Detect state, VDD is the voltage source; in the Active state, VS is the voltage source. The bypass switch and the port power switch are never both on at the same time.

While the VBUS bypass switch is active, the current available to a portable device will be limited, and the Attach Detection feature is active.

7.3 Attach Detection

The Attach Detection feature is only active in the Detect power state. When active, this feature constantly monitors for portable device attachment. When an Attach Detection event occurs, the UCS1001-2 will assert the A_DET# pin low. The UCS1001-1 internally flags the event.

Once an Attach Detection event occurs, the UCS1001 will wait for the PWR_EN control to be enabled (if not already). When PWR_EN is enabled and VS is above the threshold, the UCS1001 will activate the USB port power switch and operate in the selected Active mode (see Chapter 8, Active State).

7.4 Removal Detection

The Removal Detection feature will be active in the Active and Detect power states if S0 = 1. This feature monitors for portable device removal.

When a Removal Detection event is flagged, the following will be done:

1. Disable the port power switch and the bypass switch.
2. De-assert the A_DET# pin (UCS1001-2 only).
3. Enable an internal discharging device that will discharge the VBUS line.
4. Once the VBUS pin has been discharged, the device will return to the Detect state regardless of the PWR_EN control state.

Chapter 8 Active State

8.1 Active State Overview

The UCS1001 has the following modes of operation in the Active state: Data Pass-through, BC1.2 DCP, BC1.2 SDP, BC1.2 CDP, and Dedicated Charger Emulation Cycle. The current limiting mode depends on the Active mode behavior (see Table 8.2, "Current Limit Mode Options").

8.2 Active Mode Selection

The Active mode selection is controlled by three controls: EM_EN, M1, and M2, as shown in Table 8.1.

Table 8.1 Active Mode Selection

#	M1	M2	EM_EN	ACTIVE MODE
1	0	0	1	Dedicated Charger Emulation Cycle
2	0	1	0	Data Pass-through
3	0	1	1	BC1.2 DCP
4	1	0	0	BC1.2 SDP - See Note 8.1
5	1	0	1	Dedicated Charger Emulation Cycle
6	1	1	0	Data Pass-through
7	1	1	1	BC1.2 CDP

Note 8.1 BC1.2 SDP behaves the same as the Data Pass-through mode with the exception that it is preceded by a VBUS discharge when the mode is entered per the BC1.2 specification.

8.3 BC1.2 Detection Renegotiation

The BC1.2 specification allows a charger to act as an SDP, CDP, or DCP and to change between these roles. To force an attached portable device to repeat the charging detection procedure, VBUS must be cycled. In compliance with this specification, the UCS1001 automatically cycles VBUS when switching between the BC1.2 SDP, BC1.2 DCP, and BC1.2 CDP modes.

8.4 Data Pass-through (No Charger Emulation)

When commanded to Data Pass-through mode, UCS1001 will close its USB high-speed data switch to allow USB communications between a portable device and host controller and will operate using trip current limiting. No charger emulation profiles are applied in this mode. Data Pass-through mode will persist until commanded otherwise by the M1, M2, and EM_EN controls.

APPLICATION NOTE: If it is desired that the Data Pass-through mode operates as a traditional / standard port power switch, the S0 control should be set to ‘0’. When entering this mode, there is no automatic VBUS discharge.

APPLICATION NOTE: When the M1, M2, and EM_EN controls are set to ‘0’, ‘1’, ‘0’ or to ‘1’, ‘1’, ‘0’ respectively, Data Pass-through mode will persist if the PWR_EN control is disabled; however, the UCS1001 will draw more current. To leave Data Pass-through mode, the PWR_EN control must be enabled before the M1, M2, and EM_EN controls are changed to the desired mode.

8.5 BC1.2 SDP (No Charger Emulation)

When commanded to BC1.2 SDP mode, UCS1001 will discharge VBUS, close its USB high-speed data switch to allow USB communications between a portable device and host controller, and will operate using trip current limiting. No charger emulation profiles are applied in this mode. BC1.2 SDP mode will persist until commanded otherwise by the M1, M2, EM_EN, and PWR_EN controls.

APPLICATION NOTE: If it is desired that the BC1.2 SDP mode operates as a traditional / standard port power switch, the S0 control should be set to ‘0’.

8.6 BC1.2 CDP

When BC1.2 CDP is selected as the Active mode, UCS1001 will discharge VBUS, close its USB high-speed data switch, and apply the BC1.2 CDP charger emulation profile which performs handshaking per the specification. The combination of the UCS1001 CDP handshake along with a standard USB host comprises a charging downstream port.

If the handshake is successful, the UCS1001 will operate using constant current limiting (variable slope). If the handshake is not successful, the UCS1001 will leave the applied CDP profile in place, leave the high-speed switch closed, enable constant current limiting, and persist in this condition until commanded otherwise by the M1, M2, EM_EN, and PWR_EN controls.

The UCS1001 will respond per the BC1.2 specification to portable device initiated charger renegotiation requests.

APPLICATION NOTE: BC1.2 compliance testing may require the S0 control to be set to ‘0’ (Attach and Removal Detection feature disabled) while testing is in progress.

APPLICATION NOTE: When the UCS1001 is in BC1.2 CDP mode and the Attach and Removal Detection feature is enabled, if a power thief, such as a USB light or fan, attaches but does not assert DP, a Removal event will not occur when the portable device is removed. However, if a standard USB device is subsequently attached, Removal Detection will again be fully functional. As well, if PWR_EN is cycled or M1, M2, and / or EM_EN change state, a Removal event will occur and Attach Detection will be reactivated.

8.6.1 BC1.2 CDP Charger Emulation Profile

The BC1.2 CDP charger emulation profile acts as described below.

APPLICATION NOTE: All CDP handshaking is performed with the high-speed switch closed.

1. VBUS voltage is applied.
2. Primary Detection - When the portable device drives a voltage between 0.4 V and 0.8 V onto the DPOUT pin, the UCS1001 will drive 0.6 V onto the DMOUT pin within 20 ms.
3. When the portable device drives the DPOUT pin back to ‘0’, the UCS1001 will then drive the DMOUT pin back to ‘0’ within 20 ms.
4. Optional Secondary Detection - If the portable device then drives a voltage of 0.6 V (nominal) onto the DMOUT pin, the UCS1001 will take no other action. This will cause the portable device to observe a ‘0’ on the DPOUT pin and know that it is connected to a CDP.

8.7 BC1.2 DCP

When BC1.2 DCP is selected as the Active mode, UCS1001 will discharge VBUS and apply the BC1.2 DCP charger emulation profile per the specification. In BC1.2 DCP mode, the emulation timeout and requirement for portable device current draw are automatically disabled. When the BC1.2 DCP charger emulation profile is applied within the Dedicated Charger Emulation Cycle (see Section 8.10.1, "BC1.2 DCP Charger Emulation Profile Within DCE Cycle"), the timeout and current draw requirement are enabled.

If the portable device is charging after the DCP charger emulation profile is applied, the UCS1001 will leave in place the resistive short, leave the high-speed switch open, and enable constant current limiting (variable slope).

APPLICATION NOTE: BC1.2 compliance testing may require the S0 control to be set to '0' (Attach and Removal Detection feature disabled) while testing is in progress.

8.7.1 BC1.2 DCP Charger Emulation Profile

The BC1.2 DCP charger emulation profile is described below.

1. VBUS voltage is applied. A resistor (R_{DCP_RES}) is connected between the DPOUT and DMOUT pins.
2. Primary Detection - If the portable device drives 0.6 V (nominal) onto the DPOUT pin, the UCS1001 will take no other action than to leave the resistor connected between DPOUT and DMOUT. This will cause the portable device to see 0.6 V (nominal) on the DMOUT pin and know that it is connected to a DCP.
3. Optional Secondary Detection - If the portable device drives 0.6 V (nominal) onto the DMOUT pin, the UCS1001 will take no other action than to leave the resistor connected between DPOUT and DMOUT. This will cause the portable device to see 0.6 V (nominal) on the DPOUT pin and know that it is connected to a DCP.

8.8 Dedicated Charger

When commanded to Dedicated Charger Emulation Cycle mode, the UCS1001 enables an attached portable device to enter its charging mode by applying specific charger emulation profiles in a predefined sequence. Using these profiles, the UCS1001 is capable of generating and recognizing several signal levels on the DPOUT and DMOUT pins. The preloaded charger emulation profiles include ones compatible with BC1.2 DCP, YD/T-1591 (2009) and most Apple and RIM portable devices.

No active USB data communication is possible when charging in this mode.

8.8.1 Emulation Reset

Prior to applying any of the charger emulation profiles, the UCS1001 will perform an emulation reset. This involves the following:

1. The UCS1001 resets the VBUS line by disconnecting the port power switch and connecting VBUS to ground via an internal 100 Ω resistor. The port power switch will be held open for a time equal to t_{EM_RESET} at which point the port power switch will be closed and the VBUS voltage applied.
2. The DPOUT and DMOUT pins will be pulled low using internal 15 kΩ pull-down resistors.

APPLICATION NOTE: To help prevent possible damage to a portable device, the DPOUT and DMOUT pins have current limiting in place when the emulation profiles are applied.

8.8.2 Emulation Cycling

In Dedicated Charger Emulation Cycle mode, the charger emulation profiles will be applied in the following order:

1. Legacy 1
2. BC1.2 DCP
3. Legacy 2
4. Legacy 3
5. Legacy 4
6. Legacy 5
7. Legacy 6
8. Legacy 7

APPLICATION NOTE: If S0='0' and a portable device is not attached in DCE Cycle mode, the UCS1001 will be cycling through charger emulation profiles. There is no guarantee which charger emulation profile will be applied first when a portable device attaches.

8.8.3 DCE Cycle Retry

If none of the charger emulation profiles cause a charge current to be drawn, the UCS1001 will perform emulation reset and cycle through the profiles again. The UCS1001 will continue to cycle through the profiles so as long as charging current is not drawn and the PWR_EN control is enabled.

8.9 Current Limit Mode Associations

The UCS1001 will close the port power switch and use the current limiting mode as shown in Table 8.2.

Table 8.2 Current Limit Mode Options

ACTIVE MODE	CURRENT LIMIT MODE
Data Pass-through	Trip mode
BC1.2 DCP	CC mode if ILIM $\leq$ 1.5 A, otherwise, trip mode
BC1.2 SDP	Trip mode
BC1.2 CDP	CC mode if ILIM $\leq$ 1.5 A, otherwise, trip mode
DCE CYCLE	
During DCE Cycle when a charger emulation profile is being applied	CC mode if ILIM $\leq$ 1.5 A, otherwise, trip mode
BC1.2 DCP charger emulation profile accepted	CC mode if ILIM $\leq$ 1.5 A, otherwise, trip mode
Legacy 2 charger emulation profile accepted	CC mode if ILIM $\leq$ 1.5 A, otherwise, trip mode
Legacy 1 or Legacy 3 - Legacy 7 charger emulation profile accepted	Trip mode

8.10 Preloaded Charger Emulation Profiles

The following charger emulation profiles are resident to the UCS1001:

1. Legacy 1 - See Section 8.10.3
2. Legacy 2 - See Section 8.10.2
3. Legacy 3 - See Section 8.10.3
4. Legacy 4 - See Section 8.10.3
5. Legacy 5 - See Section 8.10.4
6. Legacy 6 - See Section 8.10.4
7. Legacy 7 - See Section 8.10.5
8. BC1.2 CDP - See Section 8.6.1
9. BC1.2 DCP - See Section 8.7.1

8.10.1 BC1.2 DCP Charger Emulation Profile Within DCE Cycle

When the BC1.2 DCP charger emulation profile (Section 8.7.1, "BC1.2 DCP Charger Emulation Profile") is applied within the DCE Cycle (Dedicated Charger Emulation Cycle is selected as the Active mode), the behavior after the profile is applied is different than Active mode BC1.2 DCP (BC1.2 DCP in Table 8.1) because the $t_{EM\_TIMEOUT}$ timer is enabled during the DCE Cycle.

During the DCE Cycle after the DCP charger emulation profile, the UCS1001 will perform one of the following:

1. If the portable device is charging, the UCS1001 will internally flag that a BC1.2 DCP was detected. The UCS1001 will leave in place the resistive short, leave the high-speed switch open, and then enable constant current limiting (variable slope).
2. If the portable device is not charging, the UCS1001 will stop applying the DCP charger emulation profile and proceed to the next charger emulation profile in the DCE Cycle.

8.10.2 Legacy 2 Charger Emulation Profile

The Legacy 2 charger emulation profile does the following:

1. The UCS1001 will connect a resistor (R_{DCP_RES}) between DPOUT and DMOUT.
2. VBUS is applied.
3. If the portable device is charging, the UCS1001 will accept that this is the correct charger emulation profile for the attached portable device. The resistive short between the DPOUT and DMOUT pins will be left in place. The UCS1001 will use constant current limiting.
4. If the portable device is not charging, the UCS1001 will stop the Legacy 2 charger emulation. This will cause resistive short between the DPOUT and DMOUT pins to be removed. Emulation reset occurs, and the UCS1001 will initiate the next charger emulation profile.

8.10.3 Legacy 1, 3, 4, and 6 Charger Emulation Profiles

Legacy 1, 3, 4, and 6 charger emulation profiles follow the same pattern of operation although the voltage that is applied on the DPOUT and DMOUT pins will vary. They do the following:

1. The UCS1001 will apply a voltage on the DPOUT pin using either a current-limited voltage source or a voltage divider between VBUS and ground with the center tap on the DPOUT pin.

2. The UCS1001 will apply a possibly different voltage on the DMOUT pin using either a current-limited voltage source or a voltage divider between VBUS and ground with the center tap on the DMOUT pin.
3. VBUS voltage is applied.
4. If the portable device is charging, the UCS1001 will accept that the currently applied profile is the correct charger emulation profile for the attached portable device. The voltages applied to the DPOUT and DMOUT pins will remain in place. The UCS1001 will begin operating in trip mode
5. If the portable device is not charging, the UCS1001 will stop the currently applied charger emulation profile. This will cause all voltages put onto the DPOUT and DMOUT pins to be removed. Emulation reset occurs, and the UCS1001 will initiate the next charger emulation profile.

8.10.4 Legacy 5 Charger Emulation Profile

Legacy 5 charger emulation profile does the following:

1. The UCS1001 will apply 900 mV to both the DPOUT and the DMOUT pins.
2. VBUS voltage is applied.
3. If the portable device is charging, the UCS1001 will accept that the currently applied profile is the correct charger emulation profile for the attached portable device. The voltages applied to the DPOUT and DMOUT pins will remain in place. The UCS1001 will begin operating in trip mode
4. If the portable device is not charging, the UCS1001 will stop the currently applied charger emulation profile. This will cause all voltages put onto the DPOUT and DMOUT pins to be removed. Emulation reset occurs, and the UCS1001 will initiate the next charger emulation profile.

8.10.5 Legacy 7 Charger Emulation Profile

The Legacy 7 charger emulation profile does the following:

1. The UCS1001 will apply a voltage on the DPOUT pin using a voltage divider between VBUS and ground with the center tap on the DPOUT pin.
2. VBUS voltage is applied.
3. If the portable device is charging, the UCS1001 will accept that Legacy 7 is the correct charger emulation profile for the attached portable device. The voltage applied to the DPOUT pin will remain in place. The UCS1001 will begin operating in trip mode
4. If the portable device is not charging, the UCS1001 will stop the Legacy 7 charger emulation profile. This will cause the voltage put onto the DPOUT pin to be removed. Emulation reset occurs, and the UCS1001 will initiate the next charger emulation profile.

Chapter 9 Package Information

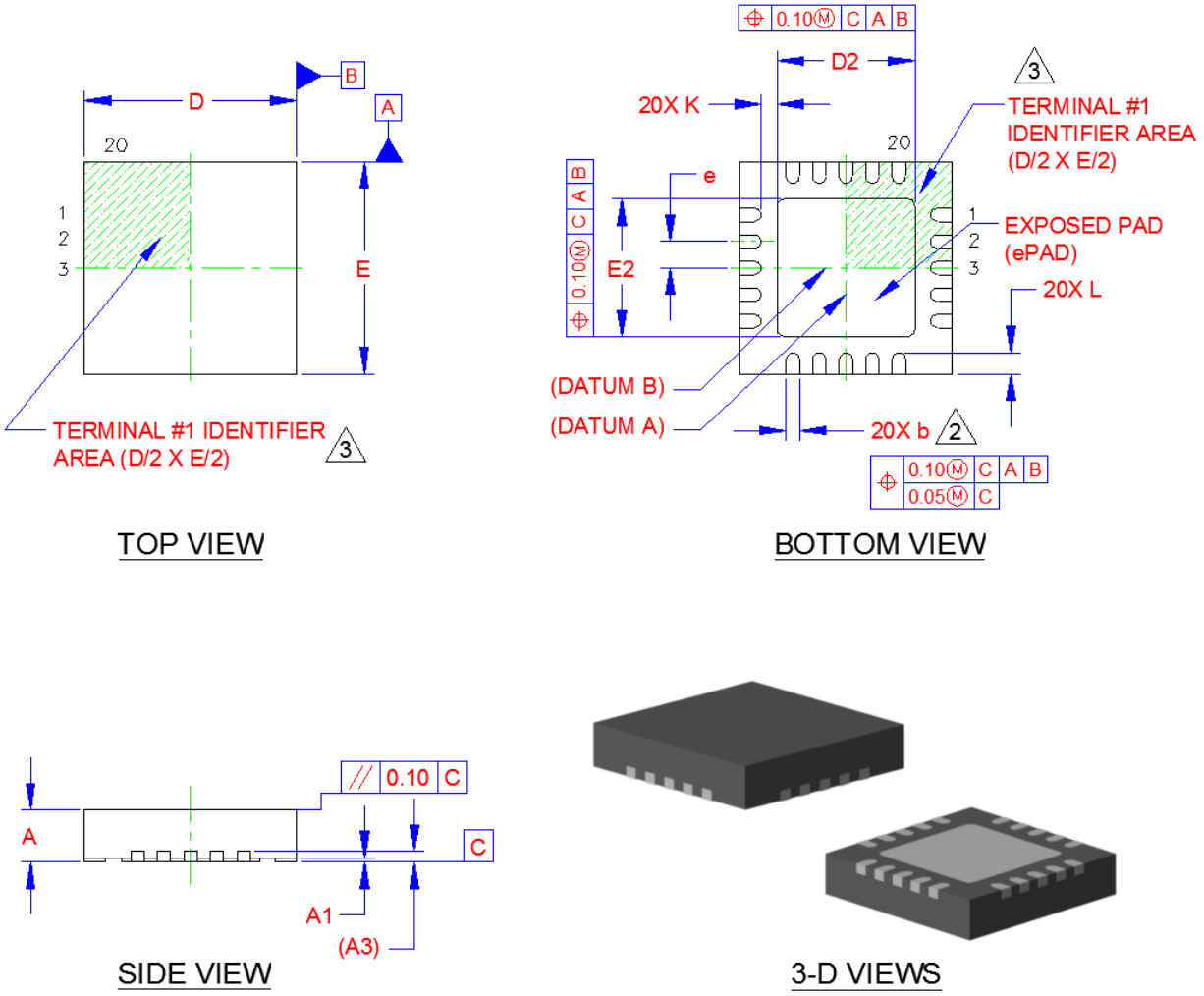
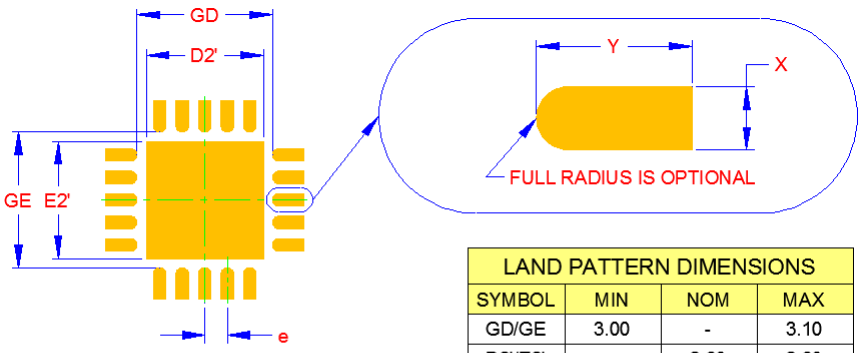


Figure 9.1 UCS1001 Package View

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3		0.20 REF		-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.50	2.60	2.70	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
K	0.25	0.30	-	-	TERMINAL TO PAD DISTANCE
e		0.50 BSC		-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

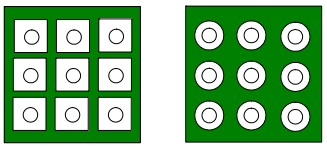
Figure 9.2 UCS1001 Package Dimensions and Notes



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	3.00	-	3.10
D2'/E2'	-	2.60	2.60
X	-	0.28	0.28
Y	0.69	-	-
e		0.50	

PCB LAND PATTERN

Figure 9.3 UCS1001 PCB Layout Notes



12 MIL VIA PATTERN

Figure 9.4 Recommended Thermal Landing Solder Paste Pattern

9.1 Package Markings

The package is marked as shown in Figure 9.5.

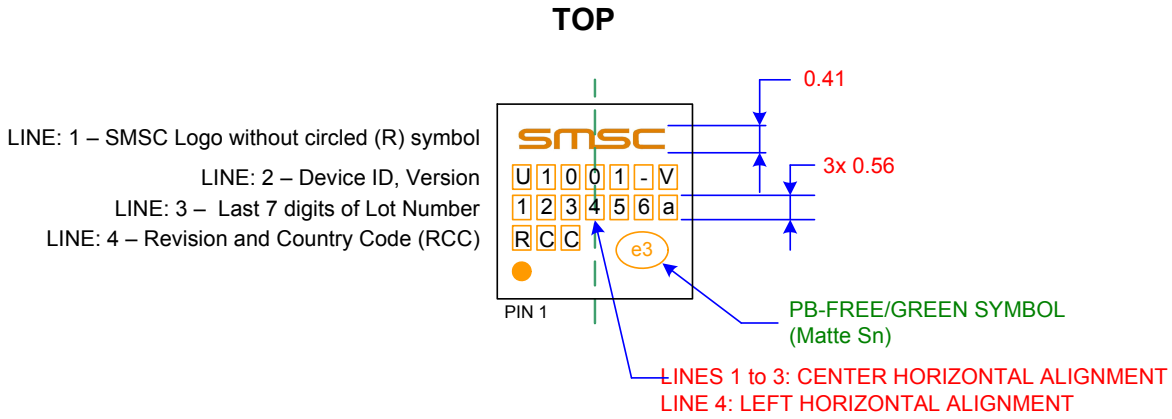


Figure 9.5 UCS1001 Package Markings

Chapter 10 Typical Operating Curves

Figure 10.1 USB-IF High-speed Eye Diagram (without data switch)

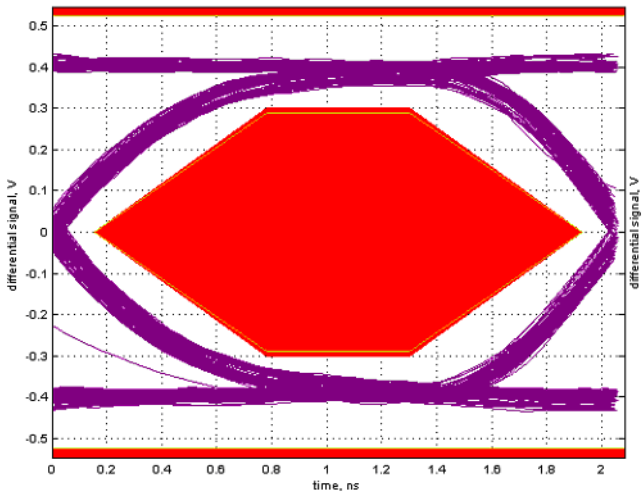


Figure 10.2 USB-IF High-speed Eye Diagram (with data switch)

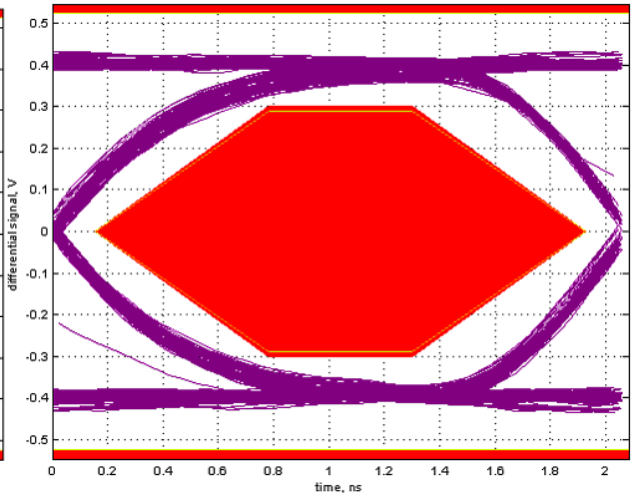


Figure 10.3 Short Applied After Power Up

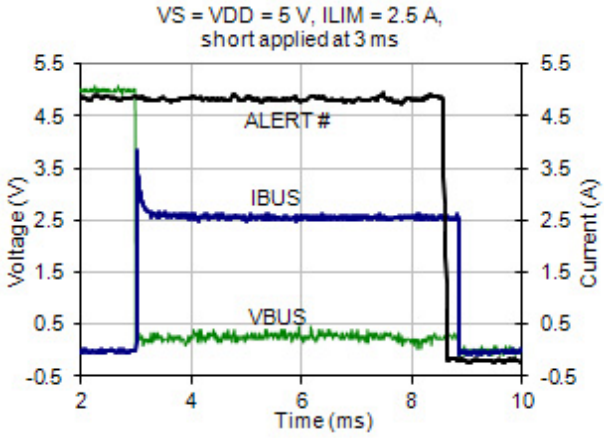


Figure 10.4 Power Up Into A Short

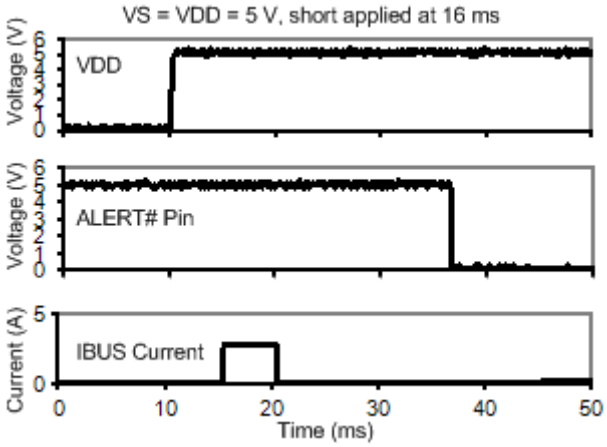


Figure 10.5 Internal Power Switch Short Response

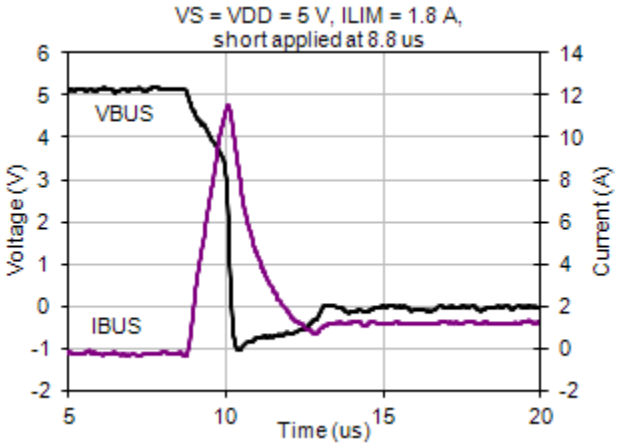


Figure 10.6 VBUS Discharge Behavior

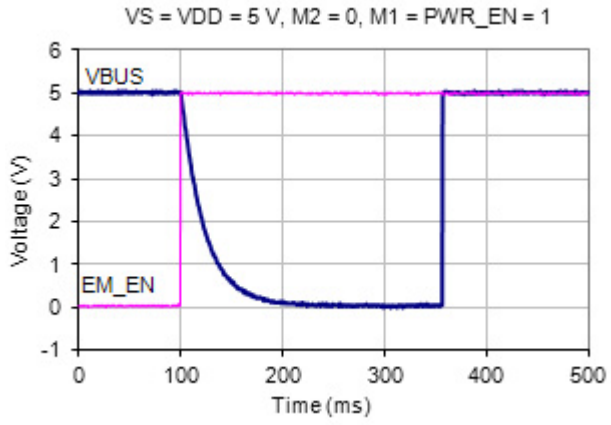


Figure 10.7 Data Switch Off Isolation vs. Frequency

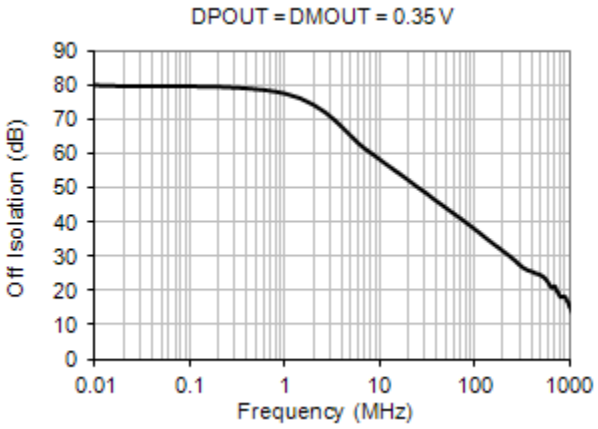


Figure 10.8 Data Switch Bandwidth vs. Frequency

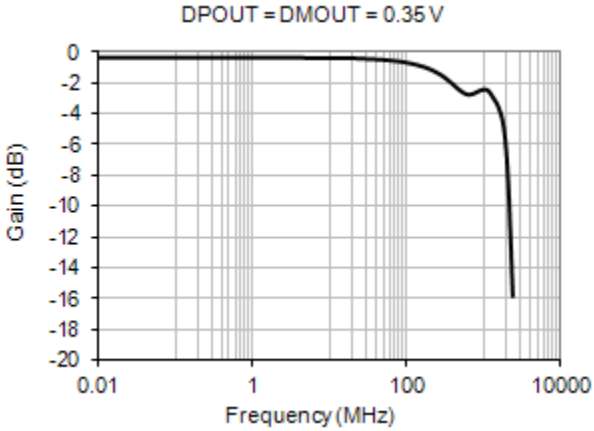


Figure 10.9 Data Switch On Resistance vs. Temp

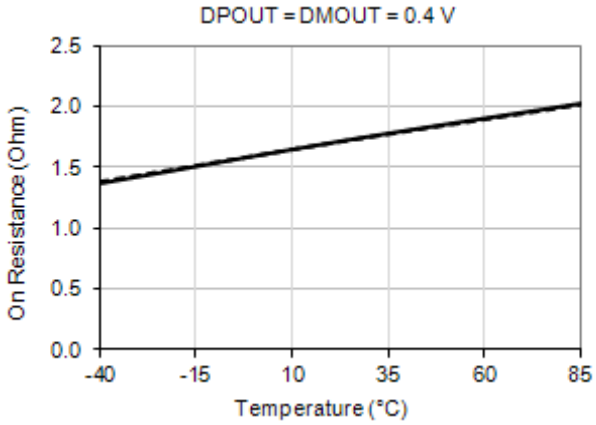


Figure 10.10 Power Switch On Resistance vs. Temp

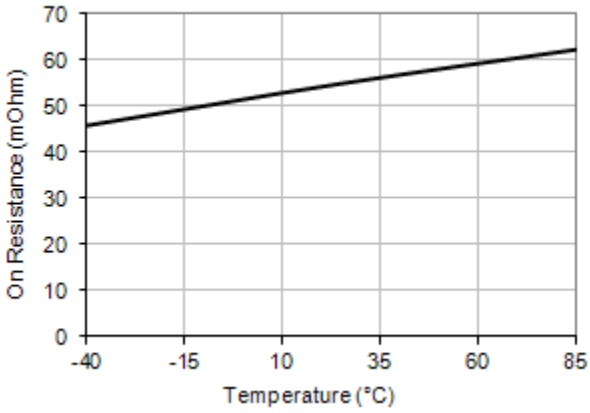


Figure 10.11 R_{DCP_RES} Resistance vs.Temp

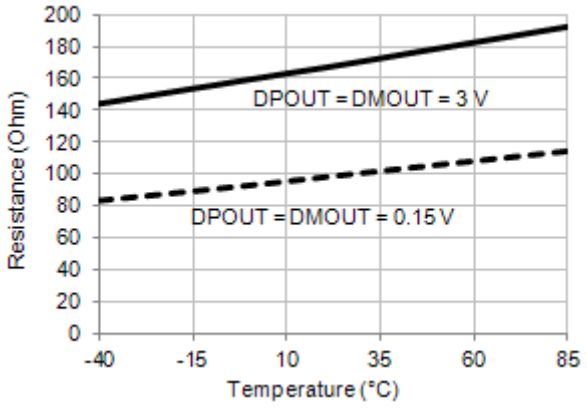


Figure 10.12 Power Switch On / Off Time vs. Temp

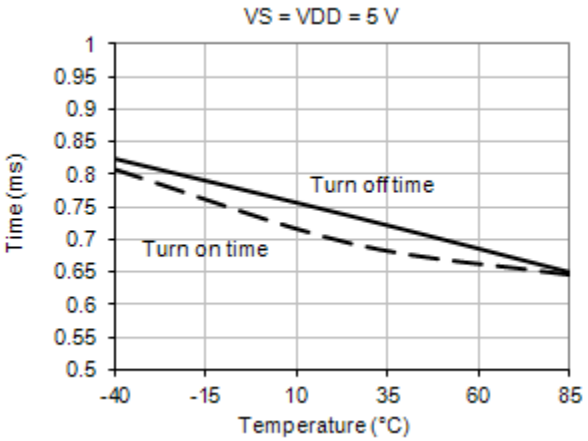


Figure 10.13 VS Over-Voltage Threshold vs. Temp

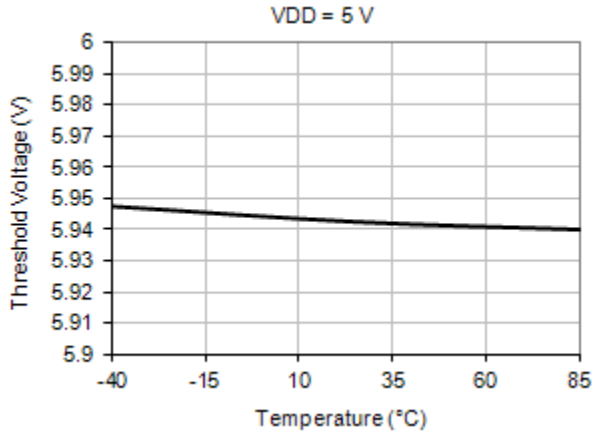


Figure 10.14 VS Under Voltage Threshold vs. Temp

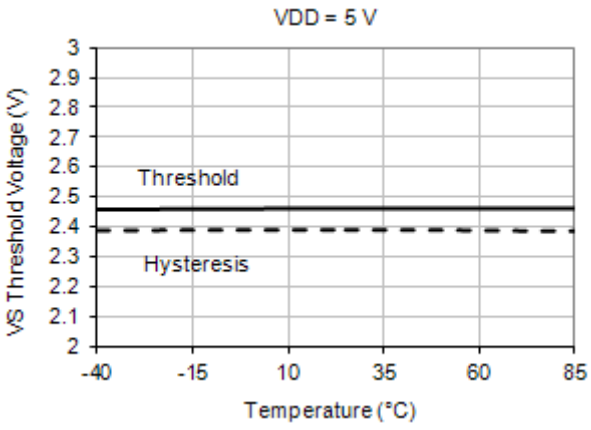


Figure 10.15 Detect State VBUS vs. IBUS

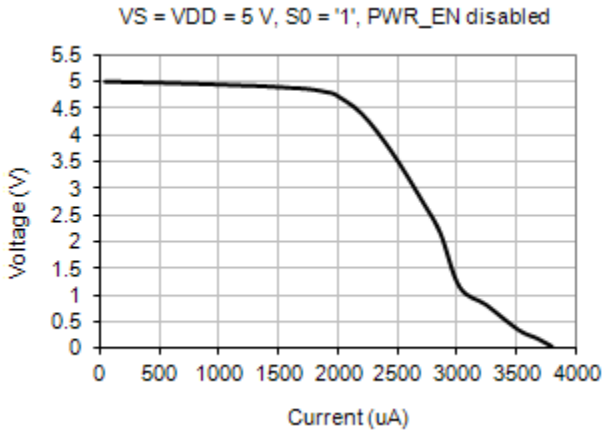


Figure 10.16 Trip Current Limit Operation vs. Temp.

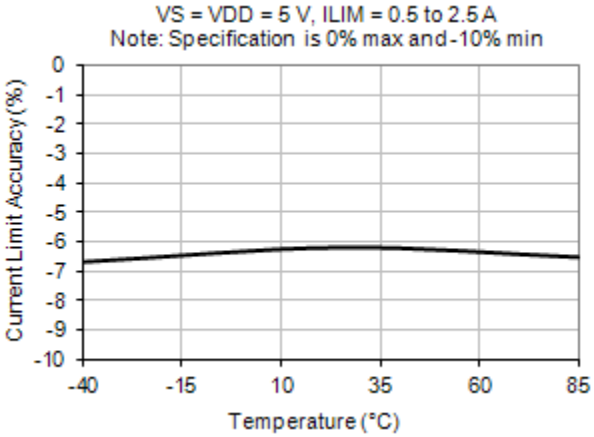


Figure 10.17 IBUS Measurement Accuracy

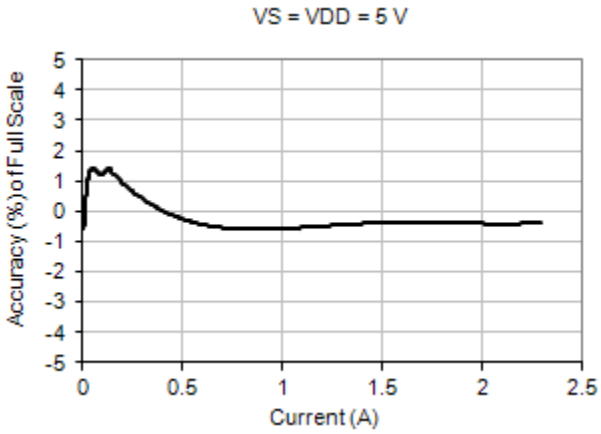


Figure 10.18 Active State Current vs. Temp

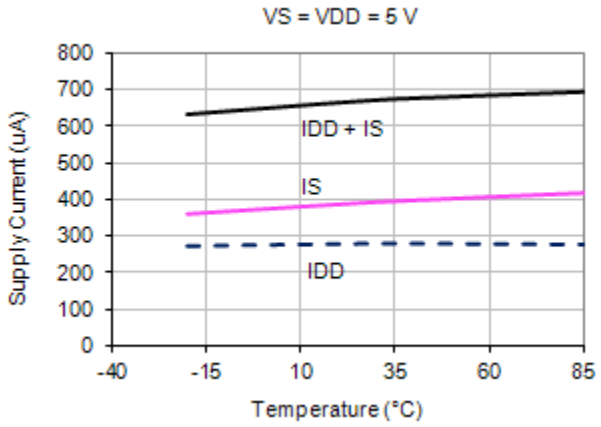


Figure 10.19 Detect State Current vs. Temp

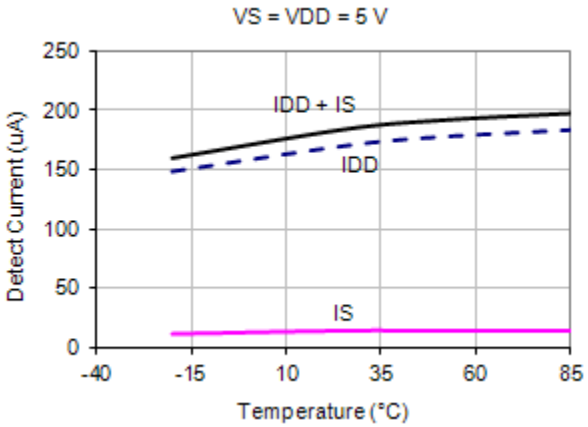
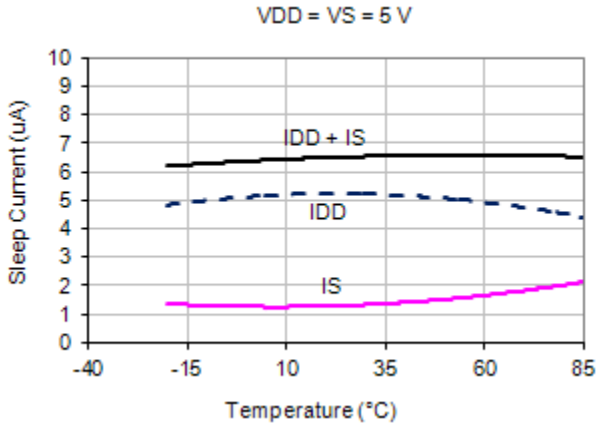


Figure 10.20 Sleep State Current vs. Temp



Chapter 11 Document Revision History

Table 11.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Revision 1.2 (05-21-12)	Cover	▪ Certification added: “UL recognized and EN/IEC 60950-1 (CB) certified”
Revision 1.2 (05-16-12)	Cover	▪ Source voltage: Vs MIN moved from 2.7 to 2.9 V to accomodate UL
	Table 3.3, "Electrical Specifications"	▪ Source voltage: Vs MIN moved from 2.7 to 2.9 V to accomodate UL
Revision 1.2 (03-16-12)	Cover	▪ There are nine preloaded charger emulation profiles.
	Chapter 2, Pin Description	▪ Changed “unused connection” to n/a for ILIM, SEL, LATCH, and S0 pins as they must be used. ▪ Added Note 2.1: Total leakage current from pins 3 and 4 (VBUS) to ground must be less than 100 µA for proper attach / removal detection operation.
	Table 3.3, "Electrical Specifications"	▪ Updated selectable current limits (ILIMx) min and max values. Typical values did not change. ▪ Changed I_{ACTIVE} from 500 µA (TYP) to 650 µA (TYP). ▪ Changed I_{ACTIVE} from TBD µA (MAX) to 750 µA (MAX). ▪ Changed I_{SLEEP} from TBD µA (MAX) to 8 µA (MAX). ▪ Changed I_{DETECT} from 190 µA (TYP) to 185 µA (TYP). ▪ Changed I_{DETECT} from TBD µA (MAX) to 220 µA (MAX). ▪ Removed V_{S_OV} MIN value (5.6 V) and MAX value (TBD). ▪ Changed R_{ON_PSW} from 70 mΩ (MAX) to 65 mΩ (MAX). ▪ Changed I_{LEAK_VS} from TBD µA (MAX) to 5 µA (MAX). ▪ Changed I_{LEAK_BYP} from 0.5 µA (MAX) to 3 µA (MAX). ▪ Changed I_{BD_1} from 2 µA (MAX) to 3 µA (MAX).
	Table 4.1, "Power States Control Settings"	▪ "Behavior" cell in the "Sleep" row: Clarified behavior by adding "VBUS will be near ground potential”.
	Section 4.1.2, "Sleep State Operation"	▪ Clarified behavior by adding "VBUS will be near ground potential”.
	Section 4.2.3, "Back-voltage Detection" and Section 4.2.4, "Back-drive Current Protection"	▪ Section “Back-voltage / Back-drive Detection” split into two. ▪ In Section 4.2.4, "Back-drive Current Protection", corrected reference I_{BD_LK} to match elec spec symbol I_{BD_1} and rewrote back-drive description.
	Section 6.2.4, "Current Limiting Modes"	▪ Added: The current limiting mode used depends on the Active state mode (see Section 8.9, "Current Limit Mode Associations").
	Section 6.2.4.1, "Trip Mode"	▪ Added application note: To avoid cycling in trip mode, set ILIM higher than the highest expected portable device current draw.
	Table 8.2, "Current Limit Mode Options"	▪ Rearranged rows so DCE Cycle is grouped together. ▪ Added row for DCE Cycle when a charger emulation profile is being applied.

Table 11.1 Customer Revision History (continued)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Revision 1.2 (03-16-12) cont.	Section 8.8.2, "Emulation Cycling" and Section 8.10.5, "Legacy 7 Charger Emulation Profile"	▪ Legacy 7 charger emulation profile added.
	Chapter 10, Typical Operating Curves	▪ Rearranged order of TOCs. ▪ Added new TOCs: — Figure 10.3, "Short Applied After Power Up" — Figure 10.5, "Internal Power Switch Short Response" — Figure 10.16, "Trip Current Limit Operation vs. Temp." — Figure 10.17, "IBUS Measurement Accuracy" — Figure 10.18, "Active State Current vs. Temp" — Figure 10.19, "Detect State Current vs. Temp" — Figure 10.20, "Sleep State Current vs. Temp" ▪ Updated the following: — Figure 10.6, "VBUS Discharge Behavior" — Figure 10.11, "RDCP_RES Resistance vs.Temp" — Figure 10.13, "VS Over-Voltage Threshold vs. Temp" — Figure 10.14, "VS Under Voltage Threshold vs. Temp" — Figure 10.15, "Detect State VBUS vs. IBUS"
Revision 1.1 (11-21-11)	Table 3.2, "Power Dissipation Summary"	▪ Missing units added.
	Table 3.3, "Electrical Specifications"	▪ Changed t_{DET_CHARGE} from 400 ms to 800 ms typ and changed condition from C_{BUS} = 220 µF to C_{BUS} = 500 µF max. ▪ VS Leakage Current changed from 0.8 µA typical to 2.2 µA. ▪ Changed I_{BD_1} and I_{BD_2} from TBD typ to 0 µA typ and from 1.5 µA max to 2 µA max ▪ Changed I_{TST} to I_{TEST} and changed typ from 165 to 190 mA. ▪ Changed t_{ON_PSW} from 3 ms to 0.75 ms typical and $t_{OFF\_PSW\_INA}$ from 1 ms to 0.75 ms typical. ▪ Added Discharge Time ($T_{DISCHARGE}$) and Allowed Charge Time (t_{DET_CHARGE}).
	Table 3.4, "ESD Ratings"Section 3.1	▪ Charged Device Model: changed from 200 V to 500 V
	Note 4.1	▪ Added note: In order to transition from Active state Data Pass-through mode into Sleep with these settings, change the M1, M2, and EM_EN pins before changing the PWR_EN pin.
	Table 4.1, "Power States Control Settings", Section 4.1.2, "Sleep State Operation", Section 5.1, "USB High-speed Data Switch"	▪ The high-speed switch is open in Sleep.
	Section 4.2.2, "VS Source Voltage"	▪ Added.
	Cover, Section 8.10.3, "Legacy 1, 3, 4, and 6 Charger Emulation Profiles"	▪ Legacy 6 profile has been defined.

Table 11.1 Customer Revision History (continued)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Revision 1.1 (11-21-11) cont.	Section 8.4, "Data Pass-through (No Charger Emulation)"	▪ Data Pass-through persists until M1, M2, or EM_EN controls are changed. It is no longer affected by PWR_EN. Added application note: When the M1, M2, and EM_EN controls are set to ‘0’, ‘1’, ‘0’ or to ‘1’, ‘1’, ‘0’ respectively, Data Pass-through mode will persist if the PWR_EN control is disabled; however, the UCS1001 will draw more current. To leave Data Pass-through mode, the PWR_EN control must be enabled before the M1, M2, and EM_EN controls are changed to the desired mode.
	Section 8.6, "BC1.2 CDP"	▪ BC1.2 CDP mode uses constant current limiting. Added application note: BC1.2 compliance testing may require the S0 control to be set to ‘0’ (Attach and Removal Detection feature disabled) while testing is in progress. ▪ Added application note: When the UCSX100X is in BC1.2 CDP mode and the Attach and Removal Detection feature is enabled, if a power thief, such as a USB light or fan, attaches but does not assert DP, a Removal event will not occur when the portable device is removed. However, if a standard USB device is subsequently attached, Removal Detection will again be fully functional. As well, if PWR_EN is cycled or M1, M2, and / or EM_EN change state, a Removal event will occur and Attach Detection will be reactivated.
	Section 8.7, "BC1.2 DCP"	▪ Added application note: BC1.2 compliance testing may require the S0 control to be set to ‘0’ (Attach and Removal Detection feature disabled) while testing is in progress.
	Table 8.2, "Current Limit Mode Options"	▪ BC1.2 CDP charger emulation changed from using “trip” to “CC mode if ILIM < 1.5 A, otherwise, trip mode”.
	Section 8.10.4, "Legacy 5 Charger Emulation Profile"	▪ Added. The Legacy 5 charger emulation profile no longer applies a voltage divider. It applies 900 mV to DPOUT and DMOUT.
Revision 1.0 (08-18-11)	Initial Release	