

LINEAR INTEGRATED CIRCUIT

HIGH PERFORMANCE CURRENT MODE POWER SWITCH

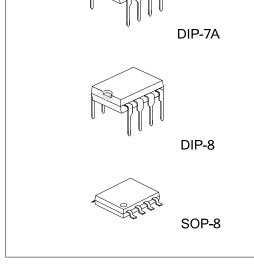
DESCRIPTION

The UTC **UCS1704S** is an integrated PWM controller and Power MOSFET specifically designed for switching operation with minimal external components. The UTC **UCS1704S** is designed to provide several special enhancements to satisfy the needs, for example, Power-Saving mode for low standby power, Frequency Hopping, Constant Output Power Limiting, Slope Compensation ,Over Current Protection (OCP), Over Voltage Protection (OVP), Over Load Protection (OLP), Under Voltage Lock Out (UVLO), Over Temperature Protection (OTP), etc. IC will be shutdown or can auto-restart in situations.

FEATURE

- * Internal Power MOSFET (700V)
- * Programming Gate Driver Capability
- * Frequency hopping for Improved EMI Performance.
- * Lower than 30mW Standby Power Design
- * Linearly decreasing frequency to 20~35KHz during light load
- * Internal Soft start
- * Internal Slope Compensation
- * Constant Power Limiting for universal AC input Range

ORDERING INFORMATION



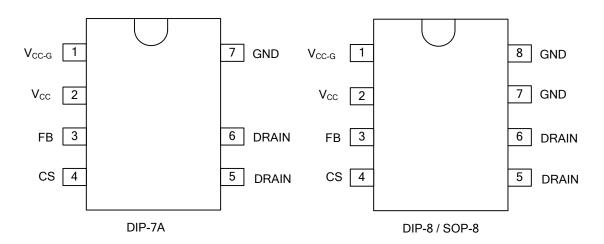
- * Gate Output Maximum Voltage Clamp(16V)
- * Over temperature protection
- * Over load protection
- * Over voltage protection
- * Leading edge blanking
- * Cycle-by-Cycle current limiting
- * Under Voltage Lock Out

Ordering Number		Daakaga	Decking	
Lead Free	Halogen Free	Package	Packing	
UCS1704SL-D07A-T	UCS1704SG-D07A-T	DIP-7A	Tube	
UCS1704SL-D08-T	UCS1704SG-D08-T	DIP-8	Tube	
UCS1704SL-S08-R	UCS1704SG-S08-R	SOP-8	Tape Reel	

MARKING

PACKAGE	MARKING
DIP-7A	7 6 5 Date Code UTC □□□□ L: Lead Free UCS1704S□ → G: Halogen Free □□□ ↓ Lot Code 1 2 3
DIP-8	8 7 6 5 Date Code UTC □□□□ L: Lead Free UCS1704S□ → G: Halogen Free □□ ↓ Lot Code 1 2 4
SOP-8	⑧ ⑦ ⑤ UTC □□□□ L: Lead Free UCS1704S□ → G: Halogen Free ● □□□ → Lot Code

■ PIN CONFIGURATION



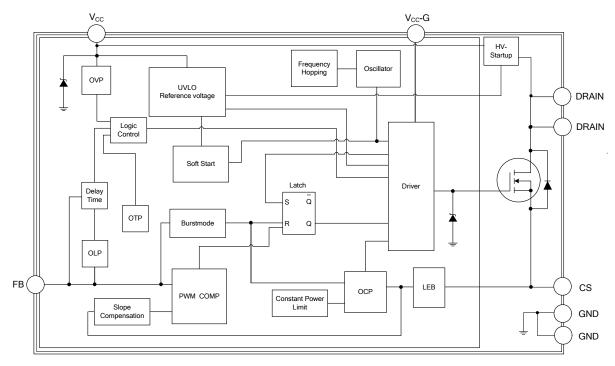
PIN DESCRIPTION

PIN NO.			DECODIDION	
DIP-7A	DIP-8 / SOP-8	PIN NAME	DESCRIPTION	
1	1	V _{CC-G}	Supply voltage	
2	2	V _{CC}	Supply voltage	
3	3	FB	Feedback	
4	4	CS	Current sense input	
5	5	DRAIN	Power MOSFET drain	
6	6	DRAIN	Power MOSFET drain	
-	7	GND	Ground	
7	8	GND	Ground	



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BLOCK DIAGRAM



Notes: OLP (Over Load Protection) OVP (Over Voltage Protection) OTP (Over Temperature Protection) OCP (Over Current Protection) UVLO (Under Voltage Latch-Out) LEB (Led Edge Blanking)



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■ **ABSOLUTE MAXIMUM RATING** (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	Vcc	32	V
Input Voltage to FB Pin	V _{FB}	-0.3 ~ 6.5	V
Input Voltage to CS Pin	V _{CS}	-0.3 ~ 6.5	V
Junction Temperature	TJ	+150	°C
Operating Temperature	T _{OPR}	-40 ~ +125	°C
Storage Temperature	T _{STG}	-50 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

OPERATING RANGE

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{cc}	10 ~ 24	V
V _{CC-G} Pin Series Resistor	V _{CC GR}	51 ~ 510	Ω

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=15V, unless otherwise specified)

	X UNIT	MAX	TYP	MIN	TEST CONDITIONS	SYMBOL	TER	PARAMET
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$								SUPPLY SECTION
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	5 μΑ	15	2		$V_{CC} = V_{THD(ON)} - 1V$	I _{ST}		Start Up Current
	5 mA	5.5	3.2		V _{FB} = 3.5V	I _{OP}		Supply Current with Switch
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	2 V	32	30	29	I _{VDD} =20mA	VCLAMP		V _{DD} Zener Clamp Voltage
$\begin{array}{c c c c c c c c c c c c c c c c c c c $							OUT SECTION	UNDER-VOLTAGE LOCK
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	2 V	22	20	18		V _{THD(ON)}		Start Threshold Voltage
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	5 V	9.5	8	6.5		V _{CC(MIN)}		Min. Operating Voltage
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $								CONTROL SECTION
Burst-Mode Out FB VoltageV FB(OUT)V CS = 01.42Burst-Mode Enter FB VoltageNormal Initial Burst mode BaseV FB(N)V VCS = 01.35Switching FrequencyBurst mode Base FrequencyF F(SW)V FB = 3.5V60657Duty CycleD Frequency HoppingD FJ(SW)V FB = 3.5V, V VCS = 070809Frequency HoppingFJ(SW)F J(SW)-9+Frequency Variation vs. V CC DeviationFDV TOVVCC = 10 ~ 20V1Frequency Variation vs. Temperature DeviationFDT T T = -40 ~ 110°C1Soft-Start TimeTSOFTS5PROTECTION SECTIONV VDPV FB(OLP)25272OLP ThresholdV VDPV FB(OLP)4.4140OUP ThresholdT TO-OLP608812OTP ThresholdT TO-OLP140140CURRENT LIMITING SECTIONV SENSE-H20045070Peak Current LimitationV SENSE-HV FB = 3.9V0.730.790.79POWER MOS-TRANSISTOR SECTIONV SENSE-LV FB = 3.9V0.730.790.79	uA		240		V _{FB} =0	I _{FB}		Feedback Source Current
Burst-Mode Out FB Voltage $V_{FB(OUT)}$ $V_{CS} = 0$ 1.42Burst-Mode Enter FB VoltageNormal Initial $V_{FB(IN)}$ $V_{CS} = 0$ 1.35Switching FrequencyBurst mode Base Frequency $F_{(SW)}$ $V_{FB} = 3.5V$ 60657Duty CycleD _{MAX} $V_{FB} = 3.5V$, $V_{CS} = 0$ 70809Frequency Hopping $F_{J(SW)}$ -9+Frequency Variation vs. V _{CC} Deviation F_{DV} $V_{CC} = 10 \sim 20V$ 1Frequency Variation vs. Temperature Deviation F_{DT} $T = .40 \sim 110^{\circ}C$ 1Soft-Start Time T_{SOFTS} 55PROTECTION SECTIONOVP Threshold V_{OVP} $V_{FB} = 3.5V$ 25272OLP Threshold T_{CHR} T_{CHR} 140140CURRENT LIMITING SECTIONLeading Edge Blanking Time t_{LEB} 2004507(Peak Current Limitation $V_{SENSE-H}$ $V_{FB} = 3.9V$ 0.730.790.POWER MOS-TRANSISTOR SECTION	V		5.4			V_{FB_Open}	vel	V _{FB} Open Loop Voltage Lev
Burst-Mode Enter FB VoltageV Normal Initial Burst mode Base FrequencyV F Burst mode Base FrequencyV F SWitching FrequencyNormal Initial Burst mode Base FrequencyV F SWitching FrequencyV SV SCCCCTTSS	V		1.42		V _{CS} =0		9	Burst-Mode Out FB Voltage
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FrequencyDPPPDuty Cycle D_{MAX} $V_{FB}=3.5V$, $V_{CS}=0$ 70809Frequency Hopping $F_{J(SW)}$ -9+Frequency Variation vs. V_{CC} Deviation F_{DV} $V_{CC}=10 \sim 20V$ 1Frequency Variation vs. Temperature Deviation F_{DT} $T=-40 \sim 110^{\circ}C$ 1Soft-Start Time T_{SOFTS} 5PROTECTION SECTION V_{OVP} $V_{FB}=3.5V$ 2527OVP Threshold V_{OVP} $V_{FB}=3.5V$ 25272OLP Threshold $V_{CS}=0$ 4.4140140Delay Time Of OLP T_{D-OLP} 608812OTP Threshold $T_{(THR)}$ 140140CURRENT LIMITING SECTIONLeading Edge Blanking Time t_{LEB} 200450Peak Current Limitation $V_{SENSE-H}$ $V_{FB}=3.9V$ 0.92Threshold Voltage For Valley $V_{SENSE-L}$ $V_{FB}=3.9V$ 0.730.79POWER MOS-TRANSISTOR SECTIONImage: Colspan="2">Image: Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2"Colspan=	0 kHz	70	65	60	V _{FB} = 3.5V		Normal Initial	
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$				00		F _(SW)	Burst mode Base	Switching Frequency
Frequency HoppingFFFFFrequency Variation vs. V _{CC} DeviationFF-9+Frequency Variation vs. Temperature DeviationFT-91Frequency Variation vs. Temperature DeviationFT-91Soft-Start TimeTT=-40 ~ 110°C1Soft-Start TimeTT5PROTECTION SECTIONOVP ThresholdVVOVP ThresholdVVVDelay Time Of OLPT04.4Delay Time Of OLPT060OTP ThresholdT140CURRENT LIMITING SECTIONIm140Leading Edge Blanking Timet1Leading Edge Blanking TimeVVPeak Current LimitationVVVSENSE-HV0.73OVP RMOS-TRANSISTOR SECTIONIm	kHz			20			Frequency	
Frequency Variation vs. V_{CC} Deviation F_{DV} $V_{CC}=10 \sim 20V$ 1Frequency Variation vs. Temperature Deviation F_{DT} $T=-40 \sim 110^{\circ}C$ 1Soft-Start Time T_{SOFTS} 5PROTECTION SECTIONOVP Threshold V_{OVP} $V_{FB}=3.5V$ 25272OLP Threshold V_{OVP} $V_{FB}=3.5V$ 25272OLP Threshold V_{OVP} $V_{FB}=0.0LP$ 608812OTP Threshold T_{D-OLP} 608812OTP Threshold $T_{(THR)}$ 140140CURRENT LIMITING SECTIONLeading Edge Blanking Time t_{LEB} 20045070Peak Current Limitation $V_{SENSE-H}$ $V_{FB}=3.9V$ 0.730.790.4POWER MOS-TRANSISTOR SECTION	0 %	90	80	70	V _{FB} =3.5V, V _{CS} =0	D _{MAX}		Duty Cycle
Frequency Variation vs. Temperature Deviation F_{DT} $T=-40 \sim 110^{\circ}C$ 1Soft-Start Time T_{SOFTS} 5PROTECTION SECTIONOVP Threshold V_{OVP} $V_{FB}=3.5V$ 25272OLP Threshold V_{OVP} $V_{FB}=3.5V$ 25272Delay Time Of OLP T_{D-OLP} 608812OTP Threshold $T_{(THR)}$ 140140CURRENT LIMITING SECTIONLeading Edge Blanking Time t_{LEB} 20045070Peak Current Limitation $V_{SENSE-H}$ $V_{FB}=3.9V$ 0.730.790.4POWER MOS-TRANSISTOR SECTION	9 %	+9		-9		F _{J(SW)}		Frequency Hopping
Soft-Start Time T_{SOFTS} 5PROTECTION SECTION V_{OVP} $V_{FB}=3.5V$ 25272OVP Threshold V_{OVP} $V_{FB}(OLP)$ $V_{CS}=0$ 4.4Delay Time Of OLP T_{D-OLP} 608812OTP Threshold $T_{(THR)}$ 140140CURRENT LIMITING SECTIONLeading Edge Blanking Time t_{LEB} 200450Peak Current Limitation $V_{SENSE-H}$ $V_{FB}=3.9V$ 0.92Threshold Voltage For Valley $V_{SENSE-L}$ $V_{FB}=3.9V$ 0.730.79POWER MOS-TRANSISTOR SECTION	0 %	10			V _{CC} =10 ~ 20V	F _{DV}	_C Deviation	Frequency Variation vs. V _C
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$\begin{array}{c c c c c c c c c c c c c c c c c c c $								PROTECTION SECTION
Delay Time Of OLP T_D-OLP 60 88 12 OTP Threshold T(THR) 140 14	8 V	28	27	25	V _{FB} =3.5V	V _{OVP}		OVP Threshold
Delay Time Of OLP T _{D-OLP} 60 88 12 OTP Threshold T(THR) 140 1	V		4.4		V _{CS} =0	V _{FB(OLP)}		OLP Threshold
OTP Threshold T _(THR) 140 CURRENT LIMITING SECTION 140 Leading Edge Blanking Time tLEB 200 450 70 Peak Current Limitation V _{SENSE-H} V _{FB} =3.9V 0.92 10.92 Threshold Voltage For Valley V _{SENSE-L} V _{FB} =3.9V 0.73 0.79 0.10 POWER MOS-TRANSISTOR SECTION Image: Contract Section	20 ms	120	88	60				Delay Time Of OLP
Leading Edge Blanking Time t_LEB 200 450 70 Peak Current Limitation V _{SENSE-H} V _{FB} =3.9V 0.92 1 Threshold Voltage For Valley V _{SENSE-L} V _{FB} =3.9V 0.73 0.79 0.1 POWER MOS-TRANSISTOR SECTION Image: Comparison of the section of the sectio	°C		140					OTP Threshold
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Threshold Voltage For Valley V _{SENSE-L} V _{FB} =3.9V 0.73 0.79 0.79 POWER MOS-TRANSISTOR SECTION	00 nS	700	450	200		t _{LEB}	ne	Leading Edge Blanking Tim
Threshold Voltage For Valley V _{SENSE-L} V _{FB} =3.9V 0.73 0.79 0.79 POWER MOS-TRANSISTOR SECTION	V		0.92		V _{FB} =3.9V	V _{SENSE-H}		Peak Current Limitation
POWER MOS-TRANSISTOR SECTION	35 V	0.85	0.79	0.73	V _{FB} =3.9V		еу	Threshold Voltage For Valle
	•							
Drain-Source Breakdown Voltage V _{DSS} V _{GS} =0V, I _D =250µA 700	V			700	V _{GS} =0V, I _D =250µA	V _{DSS}	/oltage	Drain-Source Breakdown V
	l V	4		2			ate and source	Turn-on voltage between g
	5 A	3.5						
		1.5			V _{GS} =10V, I _D =0.8A		ate Resistance	Static Drain-Source On-Sta

Notes: 1. Pulse Test: Pulse width \leq 300µs, Duty cycle \leq 2%.

2. Essentially independent of operating temperature.

FUNCTIONAL DESCRIPTION

The internal reference voltages and bias circuit work at V_{CC}> V_{THD(ON)}, and shutdown at V_{CC}<V_{CC(MIN)}.

(1) Soft-Start

When every IC power on, driver output duty cycle will be decided by inter-slope voltage V_{SOFTS} and V_{CS} on current sense resistor at beginning. After the whole soft-start phase end, and driver duty cycle depend on V_{FB} and V_{CS} . The relation among V_{SOFTS} , V_{FB} and V_{OUT} as followed Fig.3. Furthermore, soft-start phase should end before V_{CC} reach $V_{CC(MIN)}$ during V_{CC} power on. Otherwise, if soft-start phase remain not end before V_{CC} reach $V_{CC(MIN)}$ during V_{CC} power on, IC will enter auto-restart phase and not set up V_{OUT} .

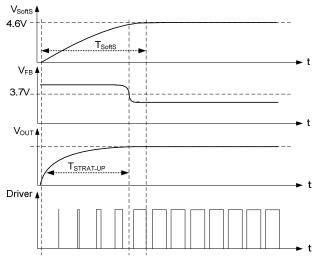


Fig.3 Soft-start phase

(2) Switching Frequency Set

The maximum switching frequency is set to 65kHz. Switching frequency is modulated by output power P_{OUT} during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower Switching frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, The IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between f_{SW} and $P_{OUT}/P_{OUT(MAX)}$ as followed Fig.4.

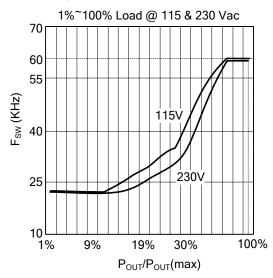


Fig.4 The relation curve between f_{SW} and relative output power POUT/ POUT (MAX)



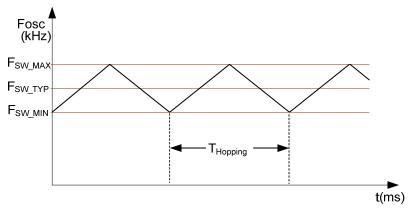
FUNCTIONAL DESCRIPTION (Cont.)

(3) Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation, this greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

(4) Frequency Hopping For EMI Improvement

The Frequency Hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed Fig.5. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.





(5) Constant Output Power Limit

When the primary current, across the primary wind of transformer, reaches the limit current, the output GATE driver will be turned off after a small propagation delay t_D . This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage V_{IN} . Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate for this output power limit variation across a wide AC input range, the threshold voltage is adjusted by adding a positive ramp. This ramp signal rises from $V_{SENSE-L}$ to V_{SENSE_H} , and then flattens out at V_{SENSE_H} . A smaller threshold voltage forces the output GATE drive to terminate earlier. This reduces the total PWM turn-on time and makes the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for a wide AC input voltage range (90VAC to 264VAC).

(6) Protection section

The IC takes on more protection functions such as OLP, OVP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. At the same time, IC enters auto-restart, V_{CC} power on and driver is reset after V_{CC} power on again.

OLP

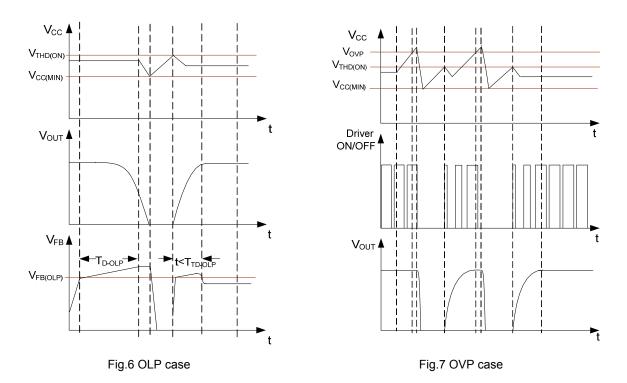
After power on, IC will shutdown driver if over load state occurs for continual T_{D-OLP}. OLP case as followed Fig.6

OVP

OVP will shutdown the switching of the power MOSFET whenever $V_{CC} > V_{OVP}$. The OVP case as followed Fig.7



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ОТР

OTP will shut down driver when junction temperature T_J>T_(THR) for continual a blanking time.

(7) Driver Output Section

The driver-stage drives the gate of the MOSFET and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the MOSFET threshold. This is achieved by a slope control of the rising edge at the driver's output. The output driver is clamped by an internal 16V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage.

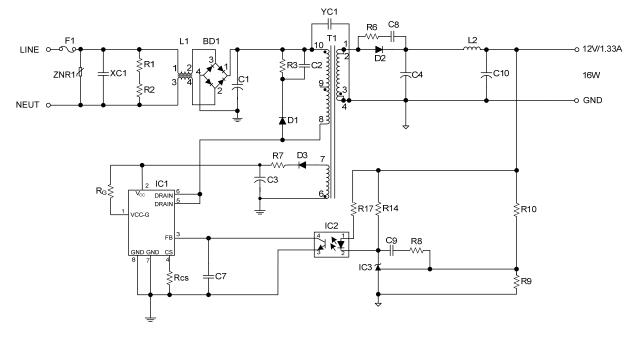
In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between V_{DD} and V_{DDG} , the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

(8) Inside power switch MOS transistor

Specific power MOS transistor parameter is as "POWER MOS TRANSISTOR SECTION" in electrical characteristics table.



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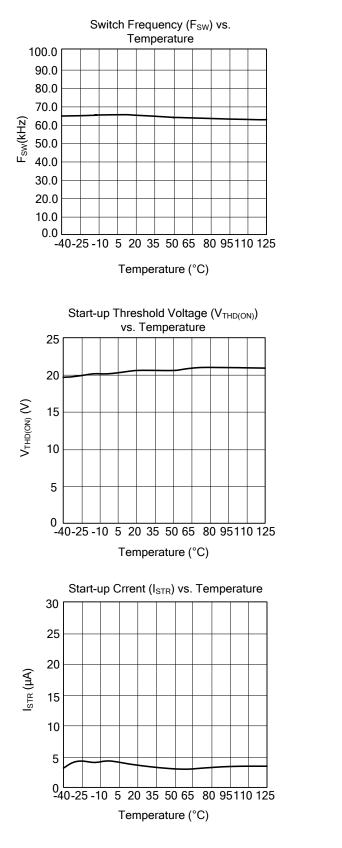
TYPICAL APPLICATION CIRCUIT

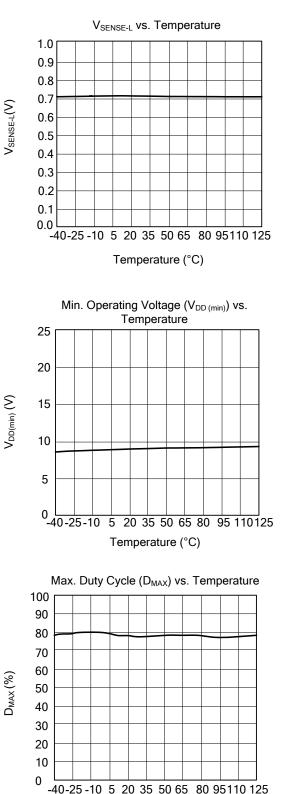
Fig.8 UTC UCS1704S Typical Application Circuit



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TYPICAL CHARACTERISTICS





Temperature (°C)



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

