BITSTREAM CONVERSION

UDA1431T

16-bit, 48 kHz, low-cost stereo current DAC

Rev. 02 — 20 February 2006 Product data sheet

1. General description

The UDA1431T is a 16-bit, 48 kHz, single-chip stereo DAC employing bitstream conversion techniques.

The UDA1431T supports the I^2S-bus data format with word lengths of up to 24 bits, MSB justified and can be operated with a $256f_s$ master clock mode.

The audio outputs meet the IEC 61938 specification.

2. Features

- Low power consumption
- Analog power supply voltage from 10.8 V to 13.2 V
- Digital power supply voltage from 3.1 V to 3.5 V
- Master clock frequencies of $256f_s$
- Supports sampling frequencies up to 48 kHz
- Integrated digital filter
- No analog post filtering required for DAC
- Slave mode only applications
- I^2S-bus input interface: 16-bit, 18-bit, 20-bit and 24-bit format compatible
- CMOS levels compatible digital inputs and outputs
- Very easy application
- Advanced audio configuration:
  - Stereo line output
  - High linearity, wide dynamic range and low distortion
- Small package size (SO14)

3. Applications

- PC audio applications
- Car radio applications
- DVD players
- Digital set-top boxes

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4. Quick reference data

Table 1: Quick reference data

V_{DDA} = 12.0 V; V_{DDD} = 3.3 V; T_{amb} = 25 °C; f_s = 48 kHz; f_i = 1 kHz; all voltages referenced to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DDA}	analog supply voltage (for DAC)			10.8	12.0	13.2	V
V_{DDD}	digital supply voltage			3.1	3.3	3.5	V
I_{DDA}	analog supply current (for DAC)	V_{DDA} = 12.0 V					
		operating	[1]	-	6.6	-	mA
		power-down		-	0.8	-	mA
I_{DDD}	digital supply current	V_{DDD} = 3.3 V					
		operating	[1]	-	7.0	-	mA
		power-down		-	6.8	-	mA
P_{tot}	total power dissipation	operating	[1]	-	102	-	mW
T_{amb}	ambient temperature			5	-	65	°C
Digital-to-analog converter							
$V_{o(rms)}$	output voltage (RMS value)			1.575	1.880	1.925	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB	[2] [3]	–62	–66	-	dB
		at –60 dB	[2] [4]	-	–32.5	-	dB
S/N	signal-to-noise ratio		[3] [5]	89	94	-	dB
α_{cs}	channel separation	at 0 dB; from 1 kHz to 20 kHz		85	98	-	dB

[1] A 1 kHz at 0 dB sine wave input is applied.

[2] (THD + N)/S is the power ratio between the sum of noise and distortion and the output signal.

[3] Measurement is performed with a 22 kHz low-pass filter and is unweighted.

[4] Measurement is performed with a ITU-R-2K filter and is unweighted.

[5] S/N is the power ratio between the output signal and the noise measured with no signal applied.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
UDA1431T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

6. Block diagram

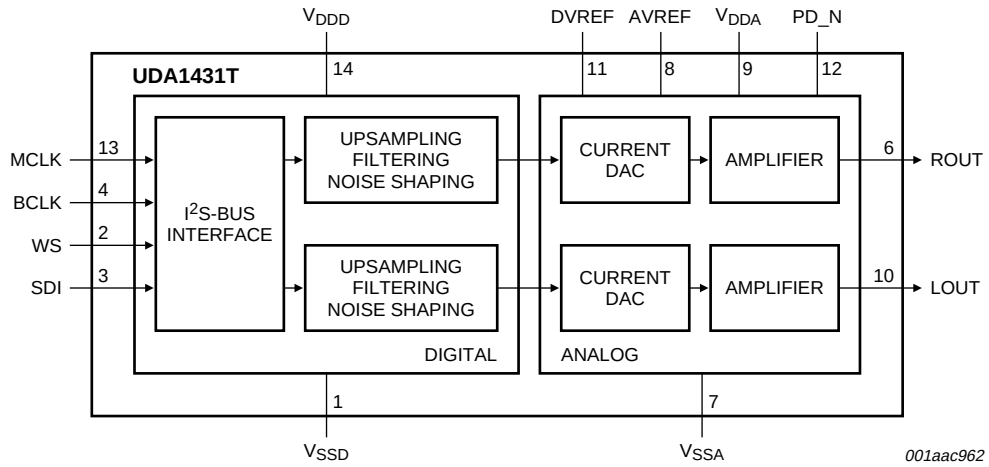


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

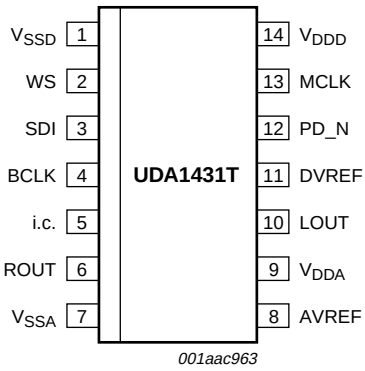


Fig 2. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
V_{SSD}	1	digital ground
WS	2	word select input
SDI	3	serial audio data input
BCLK	4	bit clock input
i.c.	5	internally connected; do not connect or connect to V_{DDD}

Table 3: Pin description *...continued*

Symbol	Pin	Description
ROUT	6	right channel output
V_{SSA}	7	analog ground (for DAC)
AVREF	8	regulator decoupling
V_{DDA}	9	analog supply voltage (for DAC)
LOUT	10	left channel output
DVREF	11	internal reference voltage (digital part)
PD_N	12	power-down input (active LOW)
MCLK	13	master clock input ($256f_s$)
V_{DDD}	14	digital supply voltage

8. Functional description

8.1 Master clock

The UDA1431T operates in slave mode only. Therefore, in all applications the system devices must provide a master clock (pin MCLK) at $256f_s$ for correct operation. The master clock must be locked in frequency to the digital interface input signals.

The UDA1431T supports sampling frequencies up to 48 kHz.

8.2 Data formats

The I^2S-bus formats are shown in Figure 3.

Left and right data channel words are time multiplexed.

The UDA1431T supports I^2S-bus formats with data word length up to 24 bits.

The BCLK clock can be up to $48f_s$, or in other words the BCLK frequency is 48 times or less the word select frequency (pin WS): $f_{BCLK} \leq 48 \times f_{WS}$.

Important: The WS edge MUST fall on the negative edge of the BCLK at all times for proper operation of the digital interface.

8.3 Noise shaper

The 1st-order noise shaper operates at $32f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a current DAC.

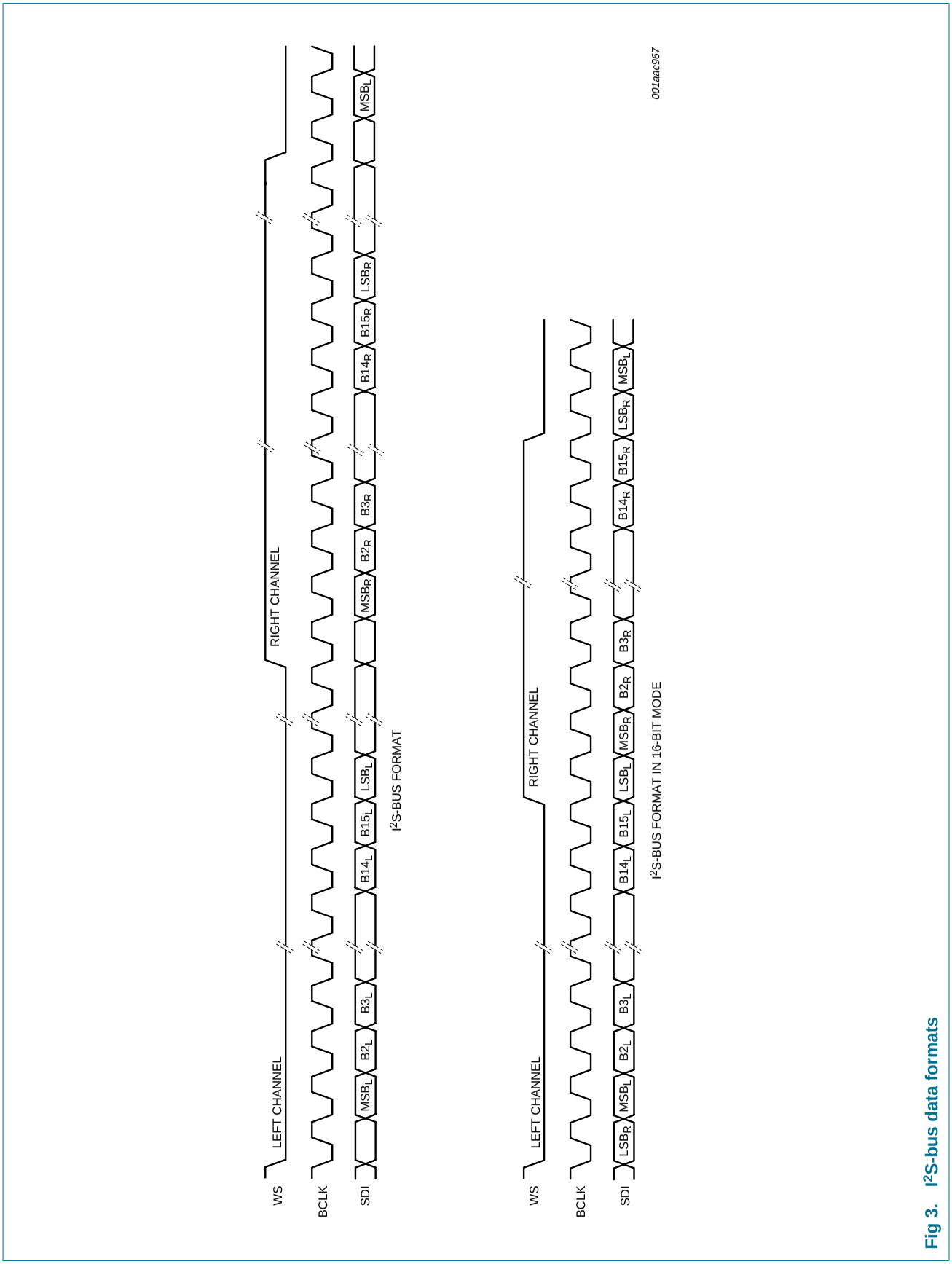


Fig 3. I^{2}S-bus data formats

9. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA}	analog supply voltage (for DAC)		[1]	-	15.2	V
V_{DDD}	digital supply voltage		[1]	-	5.5	V
T_{xtal}	crystal temperature			-	125	°C
T_{stg}	storage temperature			–65	+125	°C

[1] All supply connections must be made to the same power supply.

10. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	115	K/W

11. Static characteristics

Table 6: Static characteristics

V_{DDA} = 12.0 V; V_{DDD} = 3.3 V; T_{amb} = 25 °C; all voltages referenced to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DDA}	analog supply voltage (for DAC)			10.8	12.0	13.2	V
V_{DDD}	digital supply voltage			3.1	3.3	3.5	V
I_{DDA}	analog supply current (for DAC)	V_{DDA} = 12.0 V					
		operating	[1]	-	6.6	-	mA
		power-down		-	0.8	-	mA
I_{DDD}	digital supply current	V_{DDD} = 3.3 V					
		operating	[1]	-	7.0	-	mA
		power-down		-	6.8	-	mA
P_{tot}	total power dissipation	operating	[1]	-	102	-	mW
T_{amb}	ambient temperature			5	-	65	°C
Digital inputs: pins BCLK, WS, SDI, PD_N and MCLK							
V_{IL}	LOW-level input voltage			0	-	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DDD}$	-	V_{DDD}	V
$\|I_{LI}\|$	input leakage current (absolute value)			-	-	1	µA
C_i	input capacitance			-	-	2.5	pF
Digital-to-analog converter							
$V_{O(DC)}$	channel DC output voltage	with respect to pin V_{SSA}		-	4.9	-	V

[1] A 1 kHz at 0 dB sine wave input is applied.

12. Dynamic characteristics

Table 7: Dynamic characteristics

V_{DDA} = 12.0 V; V_{DDD} = 3.3 V; T_{amb} = 25 °C; f_s = 48 kHz; f_i = 1 kHz; all voltages referenced to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Digital-to-analog converter							
$V_{o(rms)}$	output voltage (RMS value)			1.575	1.880	1.925	V
ΔV_o	unbalance between channels	at –20 dB on both channels		-	-	0.5	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB	[1] [2]	–62	–66	-	dB
		at –60 dB	[1] [3]	-	–32.5	-	dB
DNR	dynamic range	at –60 dB	[3] [4]	89	92.5	-	dB
S/N	signal-to-noise ratio		[2] [5]	89	94	-	dB
G_{pb}	pass-band gain	at –20 dB; over the band 20 Hz to 20 kHz		–1.0	-	+0.5	dB
B	bandwidth	at –3 dB cut-off frequency		-	22	-	kHz
φ_{mis}	phase mismatch	at –20 dB; over the band 20 Hz to 20 kHz		-	0.2	1.5	deg
α_{cs}	channel separation	at 0 dB; from 1 kHz to 20 kHz		85	98	-	dB

[1] (THD + N)/S is the power ratio between the sum of noise and distortion, and the output signal.

[2] Measurement is performed with a 22 kHz low-pass filter and is unweighted.

[3] Measurement is performed with a ITU-R-2K filter and is unweighted.

[4] DNR is the result of (THD + N)/S corrected with the full-scale ratio (60 dB in this case).

[5] S/N is the power ratio between the output signal and the noise measured with no signal applied.

Table 8: Timing characteristics

V_{DDA} = 12.0 V; V_{DDD} = 3.3 V; T_{amb} = 5 °C to 65 °C; f_s = 48 kHz; all voltages referenced to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(po-so)}$	delay time from power on to stable output	MCLK active	-	-	500	ms
Master clock (see Figure 4)						
Master clock input: pin MCLK						
$T_{cy(MCLK)}$	master clock cycle time		-	81.4	-	ns
t_{WL}	pulse width LOW		28	-	53	ns
t_{WH}	pulse width HIGH		28	-	53	ns
Digital interface (see Figure 5)						
Bit clock input: pin BCLK						
$T_{cy(BCLK)}$	bit clock cycle time		20.83	-	-	µs
t_{WL}	pulse width LOW		7.29	-	-	µs

Table 8: Timing characteristics *...continued*

V_{DDA} = 12.0 V; V_{DDD} = 3.3 V; T_{amb} = 5 °C to 65 °C; f_s = 48 kHz; all voltages referenced to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WH}	pulse width HIGH		7.29	-	-	µs
t_r	rise time		-	-	3.12	µs
t_f	fall time		-	-	3.12	µs
Data input: pin SDI						
$t_{su(SDI)}$	data input set-up time		4.16	-	-	µs
$t_{h(SDI)}$	data input hold time		0	-	-	µs
Word select input: pin WS						
$t_{su(WS)}$	word select set-up time		4.16	-	-	µs
$t_{h(WS)}$	word select hold time		0	-	-	µs

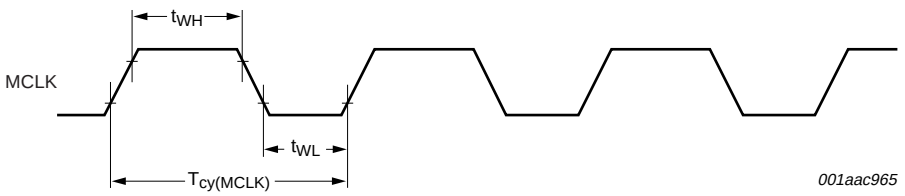


Fig 4. System clock timing

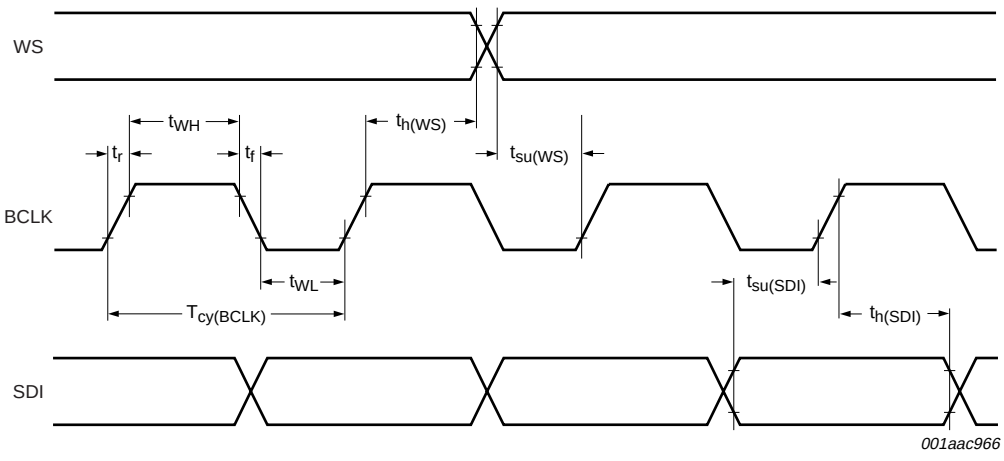
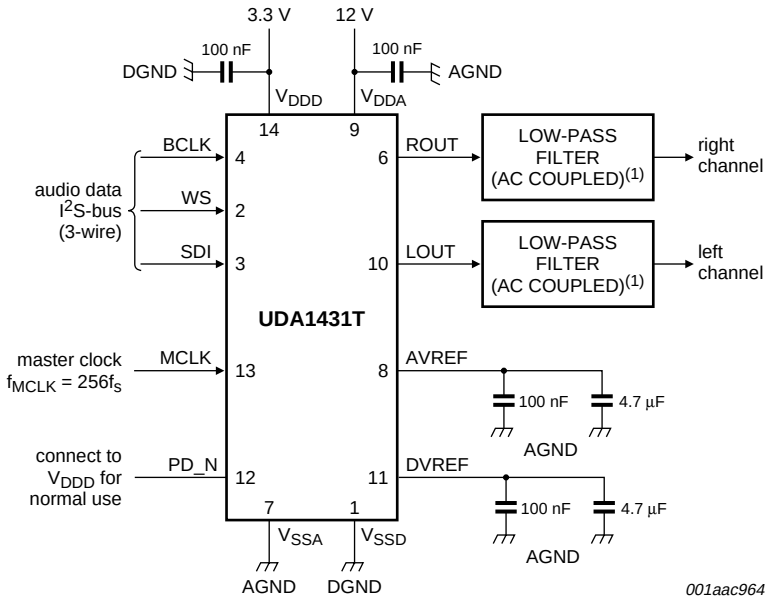


Fig 5. Serial interface timing

13. Application information



(1) At low frequencies, optimum performances will be reached using a Tantalum or a Niobium capacitor rather than with a ceramic capacitor.

Fig 6. Application diagram

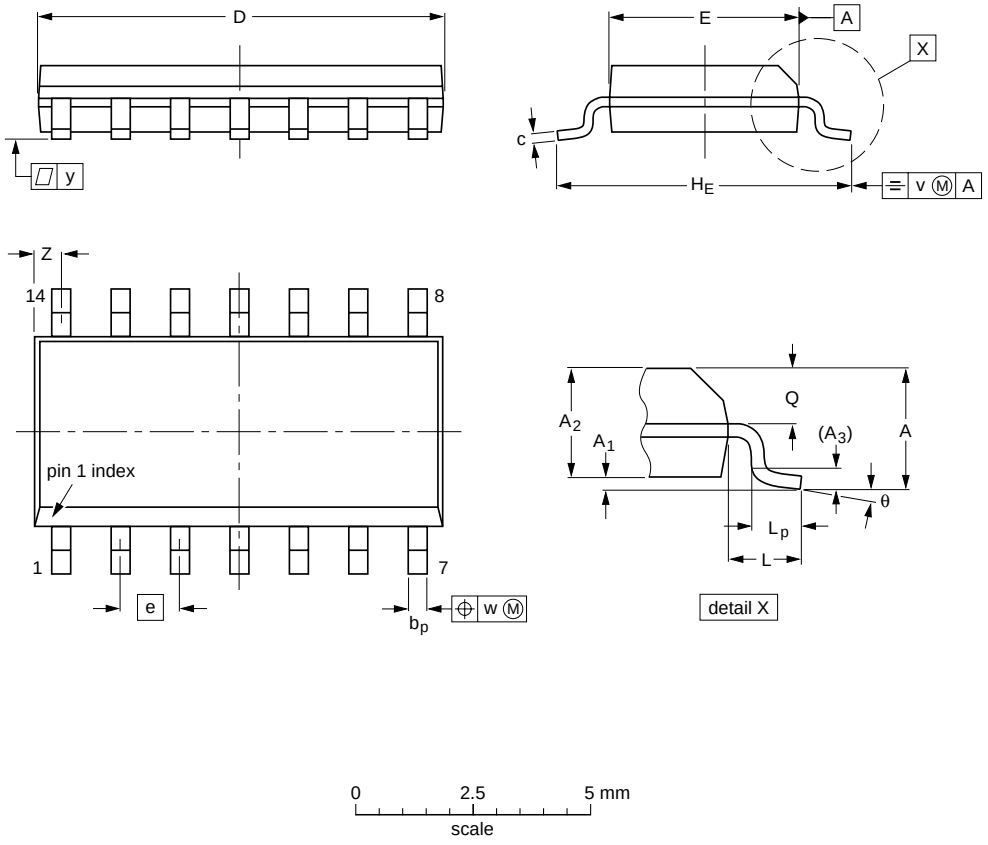
14. Test information

14.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

15. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT108-1 (SO14)

16. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

17. Soldering

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

17.5 Package related soldering information

Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

18. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
UDA1431T_2	20060220	Product data sheet	-	-	UDA1431T_1
Modifications:	• Note added to Figure 6 • In Table 8; 'MCLK active' moved to conditions column				
UDA1431T_1	20060206	Product data sheet	-	9397 750 14957	-

19. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

20. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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24. Contents

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