Low Capacitance Single Line ESD Protection Diode Array

UESD6V8L1F DFN2 1.0×0.6

General Description

The UESD6V8L1F ESD protection diode is designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and PDA's. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, lower operating voltage, lower clamping voltage and no device degradation when compared to MLVs.
The UESD6V8L1F ESD protection diode protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. The UESD6V8L1F is available in a DFN2 1.0×0.6 (Compatible with SOD882) package with working voltages of 5 volt.
It gives designer the flexibility to protect one unidirectional line in applications where arrays are not practical. Additionally, it may be "sprinkled" around the board in applications where board space is at a premium. It may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).
UESD6V8L1F is fabricated using dual diffusion technology offer low junction capacitance (20pF), which is required in high speed signal protection application.

Applications

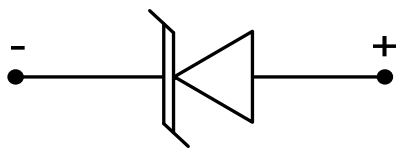
- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDA's)
- Notebooks, Desktops and Servers
- Portable Instrumentation
- Cordless Phones
- Digital Cameras
- Peripherals
- MP3 Players

Features

- Transient Protection for Data Lines to IEC 61000-4-2 (ESD) ±15kV (Air), ±8kV (Contact)
- Small Package for Use in Portable Electronics
- Suitable Replacement for MLV's in ESD Protection Applications
- Protect One I/O or Power Line
- Low Clamping Voltage
- Stand-off Voltages: 5V
- Low Leakage Current
- Solid-State Silicon-Avalanche Technology
- Small Body Outline Dimensions: 1.0mm×0.6mm

Pin Configurations

Top View



UESD6V8L1F
DFN2 1.0×0.6
(Compatible with SOD882)

Ordering Information

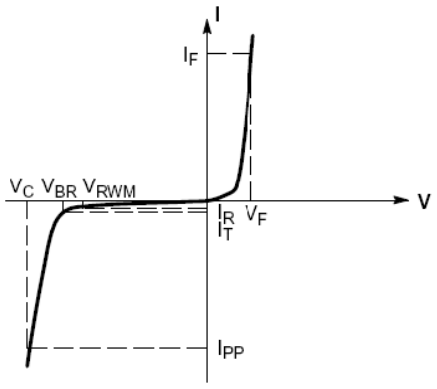
Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UESD6V8L1F	5.0V	DFN2 1.0×0.6	1	E2	5000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

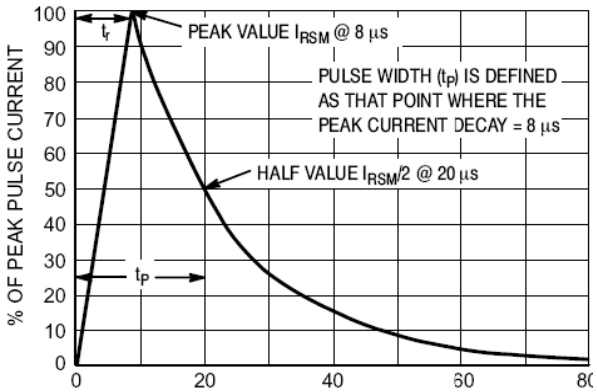
Rating	Symbol	Value	Unit
Peak Pulse Power (t_P=8/20μs)	P_{PK}	55	Watts
Maximum Peak Pulse Current (t_P=8/20μs)	I_{PP}	10.8	Amps
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{PP}	±15 ±8	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Symbol Definition

Parameter	Symbol
Maximum Reverse Peak Pulse Current	I_{PP}
Clamping Voltage @ I_{pp}	V_C
Working Peak Reverse Voltage	V_{RWM}
Maximum Reverse Leakage Current @ V_{RWM}	I_R
Breakdown Voltage @ I_T	V_{BR}
Test Current	I_t
Forward Current	I_F
Forward Voltage @ I_F	V_F
Peak Power Dissipation	P_{PK}
Max. Capacitance @ V_R=0V, f=1MHz	C



Uni−Directional TVS



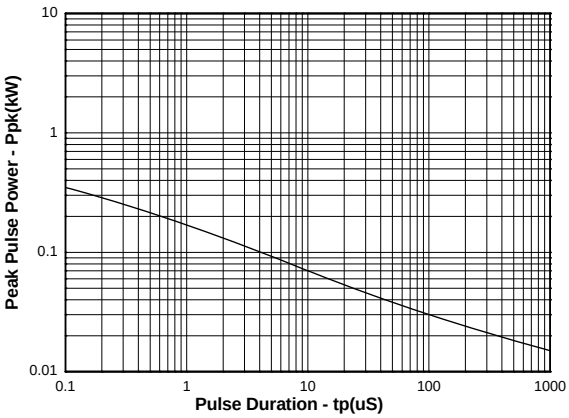
Electrical Characteristics

(T=25°C, Device for 5.0V Reverse Stand-off Voltage)

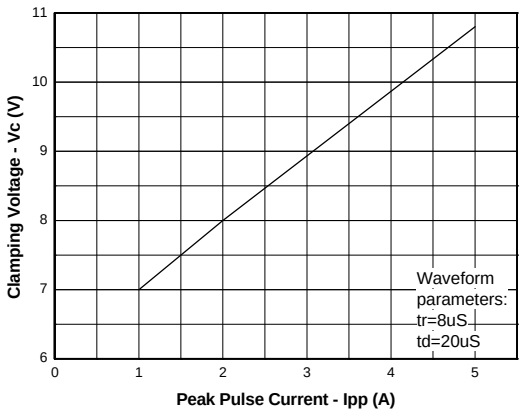
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	6	6.8	7.2	V
Reverse Leakage Current	I_R	V_{RWM}=5V, T=25°C			0.1	μA
Clamping Voltage	V_C	I_{PP}=1A, t_p=8/20μs			7	V
		I_{PP}=2A, t_p=8/20μs			8	
		I_{PP}=5A, t_p=8/20μs			10.8	
Forward Voltage	V_F	I_F=10mA		0.8		V
Junction Capacitance	C_J	V_R=0V, f=1MHz		17	20	pF
Junction Capacitance	C_J	V_R=2.5V, f=1MHz		8	10	pF

Typical Operating Characteristics

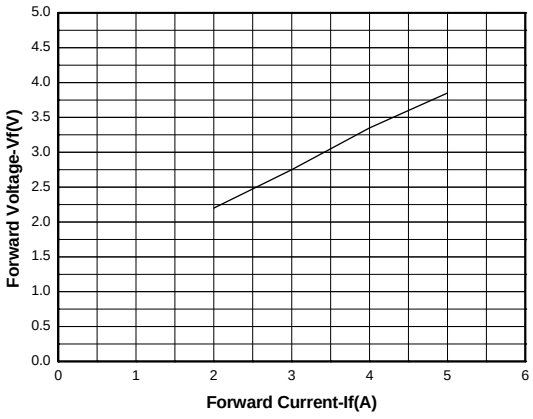
Non-Repetitive Peak Pulse Power vs. Pulse Time



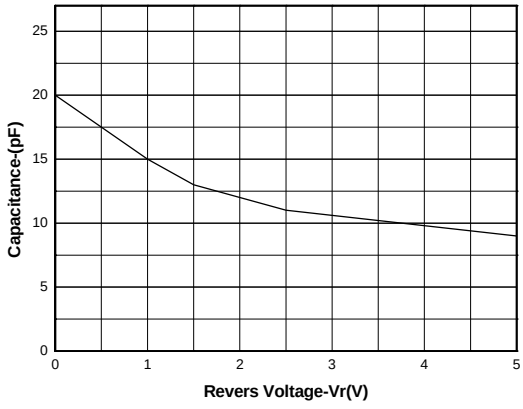
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage



Application Information

Device Connection Options

UESD6V8L1F ESD protection diode is designed to protect one data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode dot should be placed towards the line that is to be protected.

Circuit Board Layout Recommendations for Suppression of ESD

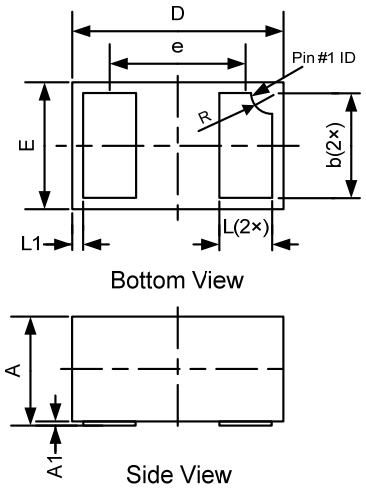
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
7. Keep parallel signal paths to a minimum.
8. Avoid running protection conductors in parallel with unprotected conductor.
9. Minimize all printed-circuit board conductive loops including power and ground loops.
10. Avoid using shared transient return paths to a common ground point.

Package Information

UESD6V8L1F DFN2 1.0×0.6

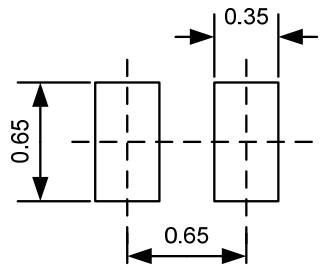
Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.40	-	0.53	0.016	-	0.021
A1	0.00	-	0.05	0.000	-	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
D	0.95	1.00	1.075	0.037	0.039	0.042
E	0.55	0.60	0.675	0.022	0.024	0.027
e	0.65TYP			0.026TYP		
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.00	0.05	0.10	0.000	0.002	0.004
R	0.05	0.10	0.15	0.002	0.004	0.006

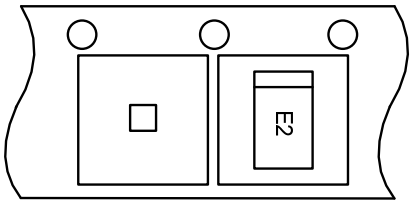
Note: R is optional.

Land Pattern



NOTES:
1. Compound dimension: 1.00×0.60;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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