Dual Line ESD Protection Diode Array

UESD6V8S2B *SOT523*

General Description

The UESD6V8S2B of TVS diode array is designed to protect sensitive electronics from damage or latch-up due to ESD and is for use in applications where board space is at a premium. It is unidirectional device and may be used on lines where the signal polarities are above ground, each device will protect up to two lines.
TVS diodes are solid-state devices feature large cross-sectional area junctions for conducting high transient currents, specifically for transient suppression. It offers desirable characteristics for board level protection including fast response time, low operating, low clamping voltage, and no device degradation.
The UESD6V8S2B may be used to meet the immunity requirements of IEC 61000-4-2, ±15kV air, ±8kV contact discharge and MIL-STD-883 METHOD 3015, ±8 kV HBM. The small package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

Applications

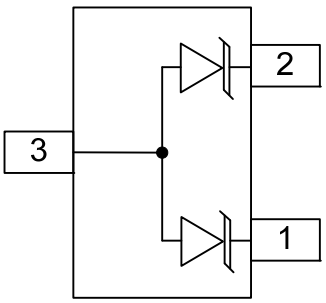
- Cellular Handsets & Accessories
- Cordless Phones
- Personal Digital Assistants (PDA's)
- Notebooks & Handhelds
- Portable Instrumentation
- Digital Cameras
- Peripherals
- MP3 Players

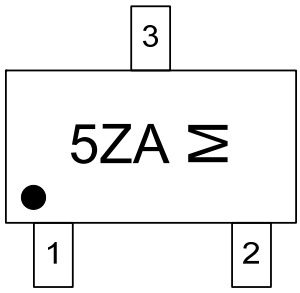
Features

- Transient Protection for Data & Power Lines to IEC 61000-4-2 (ESD) ±15kV (Air), ±8kV (Contact)
- MIL-STD-883 3015 (HBM) ±8kV
- Protect Two I/O Lines
- Working Voltages: 5V
- Low Leakage Current
- Low Operating and Clamping Voltage
- Solid-State Silicon Avalanche Technology

Pin Configurations

Top View





M: Month Code
UESD6V8S2B
SOT523

Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UESD6V8S2B	5.0V	SOT523	2	5ZA	3000pcs/7Inch Tape & Reel

Absolute Maximum Ratings

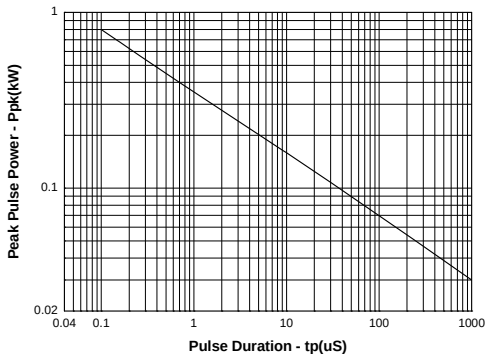
Rating	Symbol	Value	Unit
Peak Pulse Power (t_P=8/20μs)	P_{PK}	140	Watts
Peak Pulse Current (t_P=8/20μs)	I_{PP}	11	A
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Electrical Characteristics

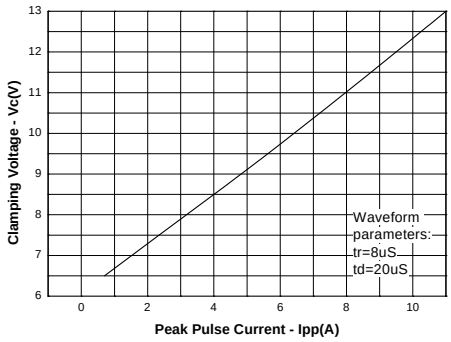
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	6	6.8	7.2	V
Reverse Leakage Current	I_R	V_{RWM}=5V, T=25°C			0.1	μA
Clamping Voltage	V_C	I_{PP}=5A, t_P=8/20μs			9.1	V
		I_{PP}=11A, t_P=8/20μs			13	
Junction Capacitance	C_J	Pin 1, 2 to 3 V_R=0V, f=1MHz		40	50	pF
Junction Capacitance	C_J	Pin 1, 2 to 3 V_R=2.5V, f=1MHz		30	40	pF
Reverse Dynamic Resistance	$R_{dyn,rev}$	I_{PP}=1A~5A		0.6		Ω
Forward Dynamic Resistance	$R_{dyn,fwd}$			0.5		Ω

Typical Operating Characteristics

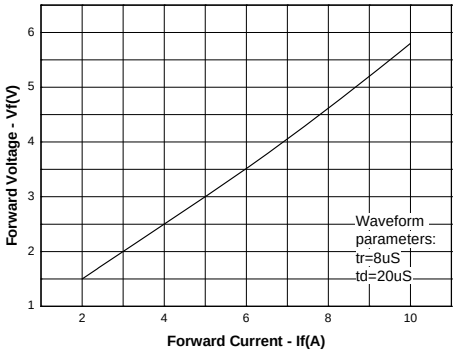
Non-Repetitive Peak Pulse Power vs. Pulse Time



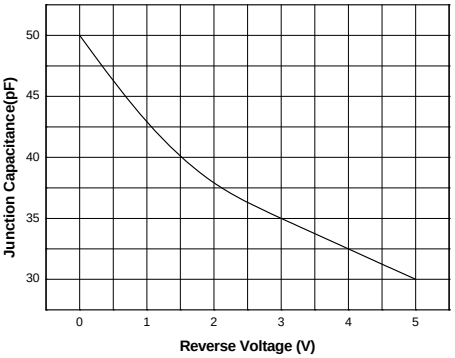
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage

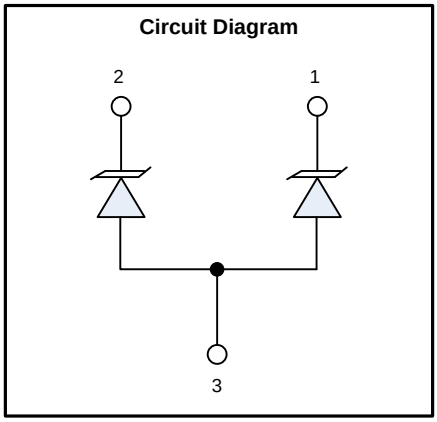


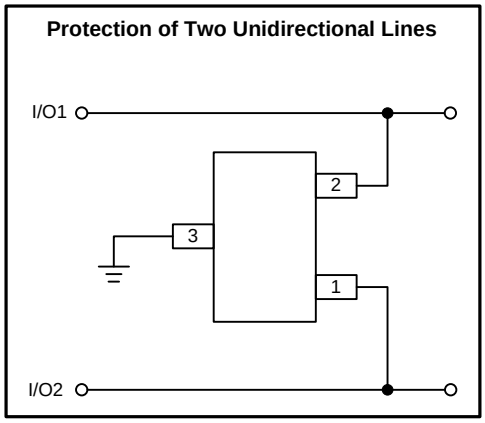
Applications Information

UESD6V8S2B ESD protection diode is designed to protect dual data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode should be placed towards the line that is to be protected.

Device Connection for Protection of Dual Data Lines

The Dual TVS Diode Array is designed to protect up to two unidirectional data lines. The device is connected as follows:
Unidirectional protection of two I/O lines is achieved by connecting pins 1 and 2 to the data lines. Pin 3 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.





Circuit Board Layout Recommendations for Suppression of ESD

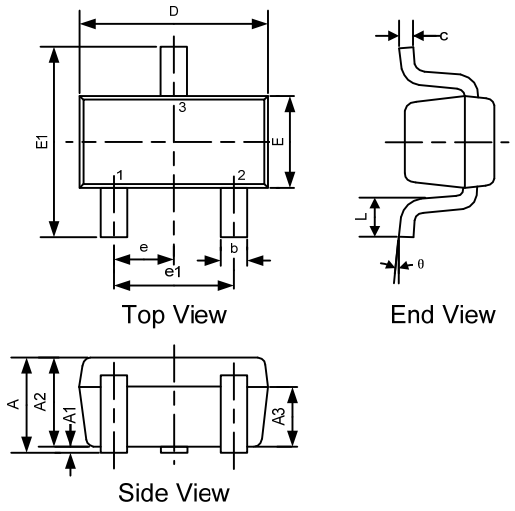
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

Place the TVS near the input terminals or connectors to restrict transient coupling.
Minimize the path length between the TVS and the protected line.
Minimize all conductive loops including power and ground loops.
The ESD transient return path to ground should be kept as short as possible.
Never run critical signals near board edges.
Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
Keep parallel signal paths to a minimum.
Avoid running protection conductors in parallel with unprotected conductor.
Minimize all printed-circuit board conductive loops including power and ground loops.
Avoid using shared transient return paths to a common ground point.

Package Information

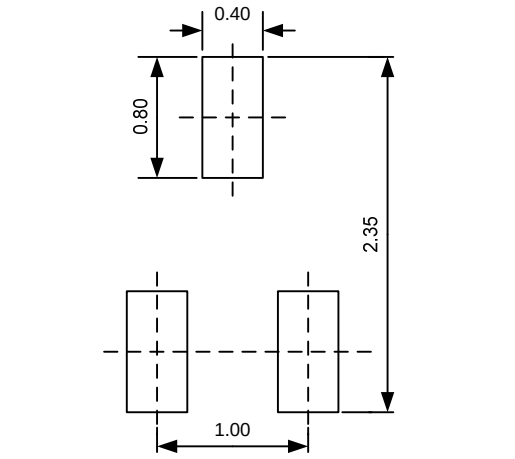
UESD6V8S2B SOT523

Outline Drawing



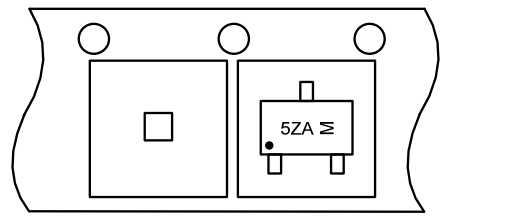
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.60	0.80	0.90	0.024	0.031	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.60	0.75	0.80	0.024	0.030	0.031
A3	0.45	0.50	0.65	0.018	0.020	0.026
b	0.15	0.22	0.30	0.006	0.009	0.012
c	0.10	0.12	0.20	0.004	0.005	0.008
D	1.50	1.60	1.70	0.059	0.063	0.067
E	0.75	0.80	0.85	0.030	0.031	0.033
E1	1.45	1.60	1.75	0.057	0.063	0.069
e	0.50TYP			0.020TYP		
e1	0.90	1.00	1.10	0.035	0.039	0.043
L	0.20	0.33	0.40	0.008	0.013	0.016
θ	0°	-	8°	0°	-	8°

Land Pattern



NOTES:
1. Compound dimension: 1.60×0.80 ;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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