

Silicon Carbide (SiC) JFET - EliteSiC, Power N-Channel, D2PAK-7L, 1700 V, 400 mohm

Rev. C, January 2025

DATASHEET

UF3N170400B7S

Description

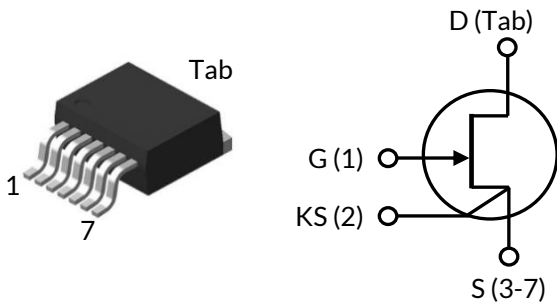
UnitedSiC offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at $V_{GS} = 0\text{ V}$ is also ideal for current protection circuits without the need for active control, as well as for cascode operation.

Features

- ◆ Typical on-resistance $R_{DS(on),typ}$ of 400mΩ
- ◆ Voltage controlled
- ◆ Maximum operating temperature of 175°C
- ◆ Extremely fast switching not dependent on temperature
- ◆ Low gate charge
- ◆ Low intrinsic capacitance
- ◆ RoHS compliant

Typical applications

- ◆ Over Current Protection Circuits
- ◆ DC-AC Inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating



Part Number	Package	Marking
UF3N170400B7S	D ² PAK-7L	UF3N170400B7S



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1700	V
Gate-source voltage	V_{GS}	DC	-20 to +3	V
		AC ¹	-30 to +20	V
Continuous drain current ²	I_D	$T_C = 25^\circ\text{C}$	6.8	A
		$T_C = 100^\circ\text{C}$	5.1	A
Pulsed drain current ³	I_{DM}	$T_C = 25^\circ\text{C}$	16	A
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	68	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	T_{solder}	reflow MSL 1	245	$^\circ\text{C}$

1. +20V AC rating applies for turn-on pulses <200ns applied with external $R_G > 1\Omega$.

2. Limited by $T_{J,max}$

3. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			1.7	2.2	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS} = -20\text{V}, I_D = 0.3\text{mA}$	1700			V
Total drain leakage current	I_{DSS}	$V_{DS} = 1700\text{V}, V_{GS} = -20\text{V}, T_J = 25^\circ\text{C}$		2.2	60	μA
		$V_{DS} = 1700\text{V}, V_{GS} = -20\text{V}, T_J = 175^\circ\text{C}$		9		
Total gate leakage current	I_{GSS}	$V_{GS} = -20\text{V}, T_J = 25^\circ\text{C}$		0.15	6	μA
		$V_{GS} = -20\text{V}, T_J = 175^\circ\text{C}$		0.8		μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 2\text{V}, I_D = 5\text{A}, T_J = 25^\circ\text{C}$		350		m Ω
		$V_{GS} = 0\text{V}, I_D = 5\text{A}, T_J = 25^\circ\text{C}$		400	500	
		$V_{GS} = 2\text{V}, I_D = 5\text{A}, T_J = 175^\circ\text{C}$		928		
		$V_{GS} = 0\text{V}, I_D = 5\text{A}, T_J = 175^\circ\text{C}$		1040		
Gate threshold voltage	$V_{G(th)}$	$V_{DS} = 5\text{V}, I_D = 4.5\text{mA}$	-11.3	-9	-6.7	V
Gate resistance	R_G	$f = 1\text{MHz}, \text{open drain}$		5		Ω

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=-20V$ $f=100kHz$		225		pF
Output capacitance	C_{oss}			22		
Reverse transfer capacitance	C_{rss}			18		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 1200V, $V_{GS}=-20V$		11.4		pF
C_{OSS} stored energy	E_{oss}	$V_{DS}=1200V, V_{GS}=-20V$		8.2		μJ
Total gate charge	Q_G	$V_{DS}=1200V, I_D=5A,$ $V_{GS} = -18V$ to 0V		30		nC
Gate-drain charge	Q_{GD}			17		
Gate-source charge	Q_{GS}			5		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=1200V, I_D=5A,$ Gate Driver = -18V to 0V, $R_G=1\Omega,$ Inductive Load, FWD: 2x UJ3D1210TS in series $T_J=25^\circ C$		5		ns
Rise time	t_r			19		
Turn-off delay time	$t_{d(off)}$			9		
Fall time	t_f			37		
Turn-on energy	E_{ON}			125		
Turn-off energy	E_{OFF}		38		μJ	
Total switching energy	E_{TOTAL}		163			
Turn-on delay time	$t_{d(on)}$	$V_{DS}=1200V, I_D=5A,$ Gate Driver = -18V to 0V, $R_G=1\Omega,$ Inductive Load, FWD: 2x UJ3D1210TS in series, $T_J=150^\circ C$		5		ns
Rise time	t_r			16		
Turn-off delay time	$t_{d(off)}$			8		
Fall time	t_f			34		
Turn-on energy	E_{ON}			114		
Turn-off energy	E_{OFF}		31		μJ	
Total switching energy	E_{TOTAL}		145			

Typical Performance Diagrams

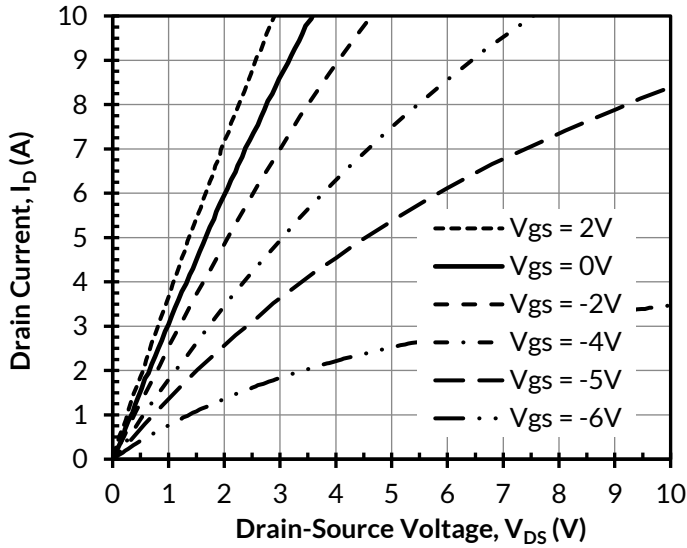


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

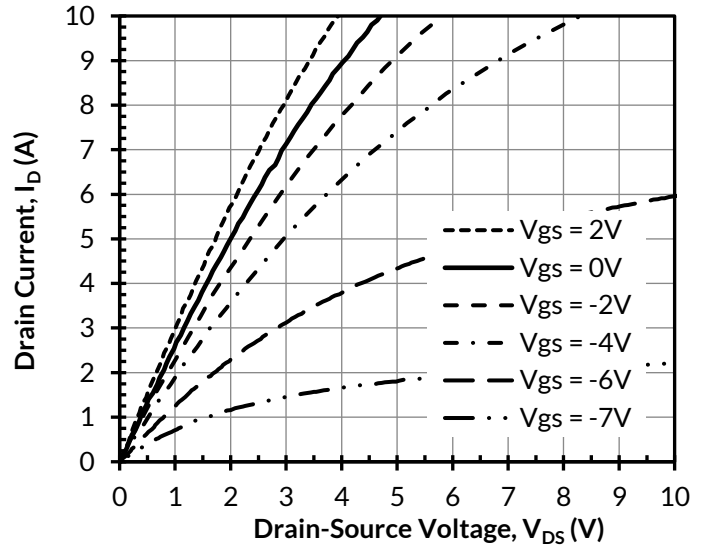


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

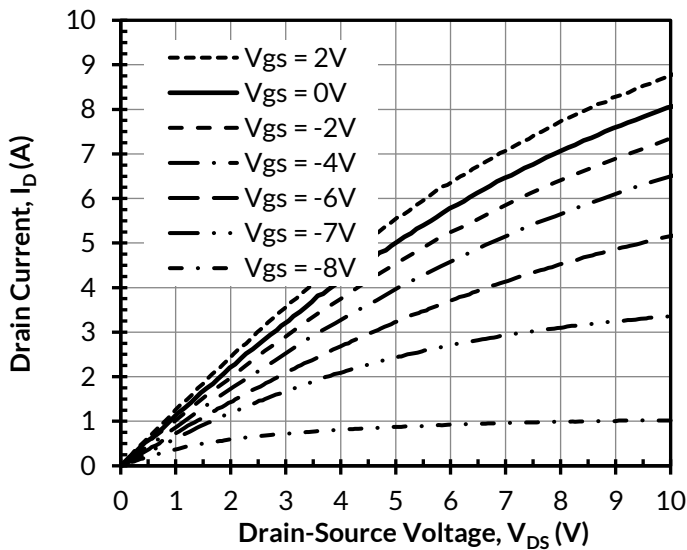


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

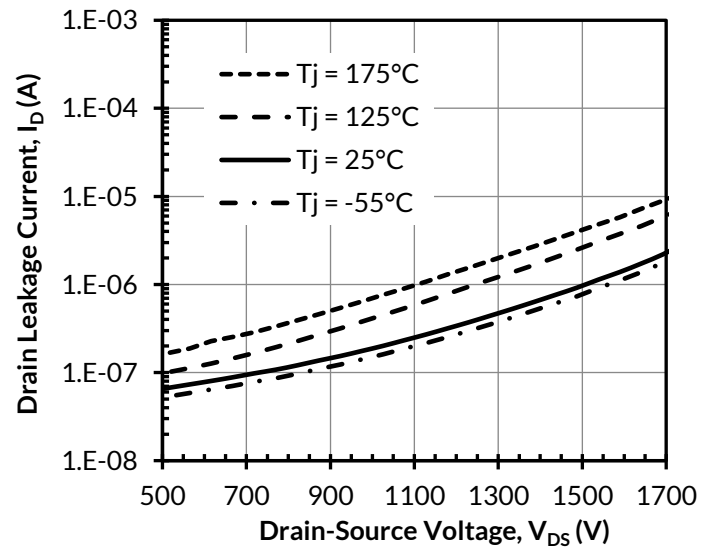


Figure 4. Typical drain-source leakage at $V_{GS} = -20\text{V}$

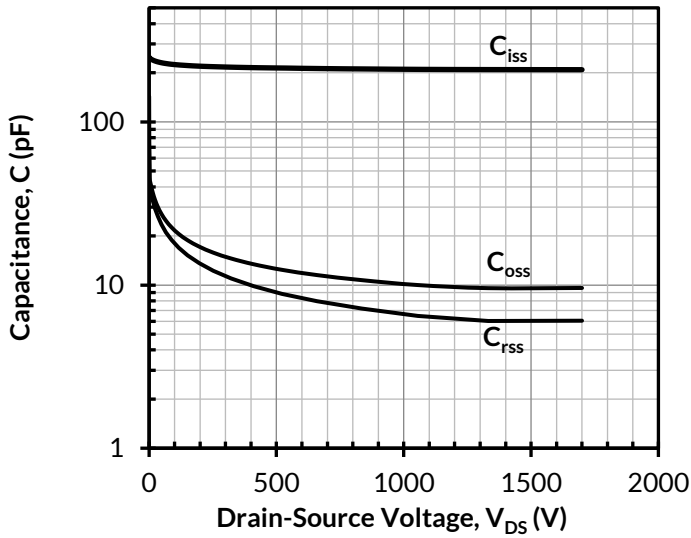


Figure 5. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = -20\text{V}$

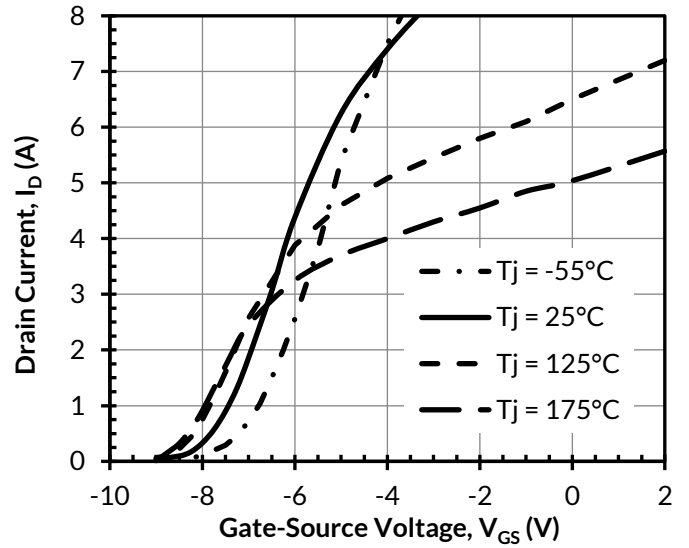


Figure 6. Typical transfer characteristics at $V_{DS} = 5\text{V}$

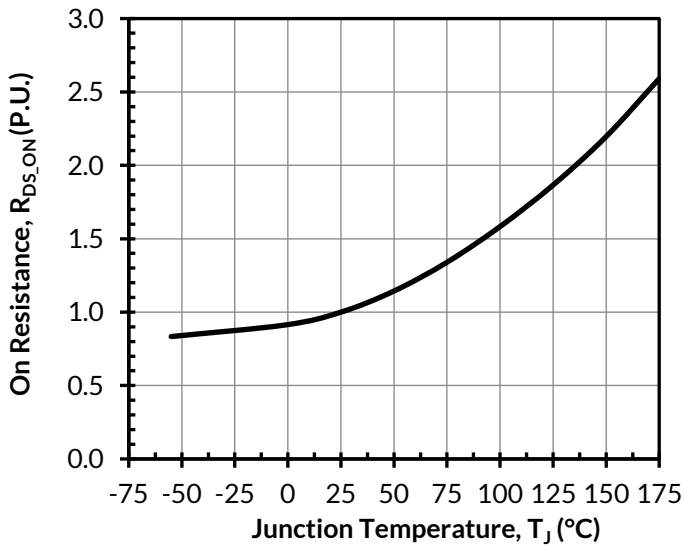


Figure 7. Normalized on-resistance vs. temperature at $V_{GS} = 0\text{V}$ and $I_D = 5\text{A}$

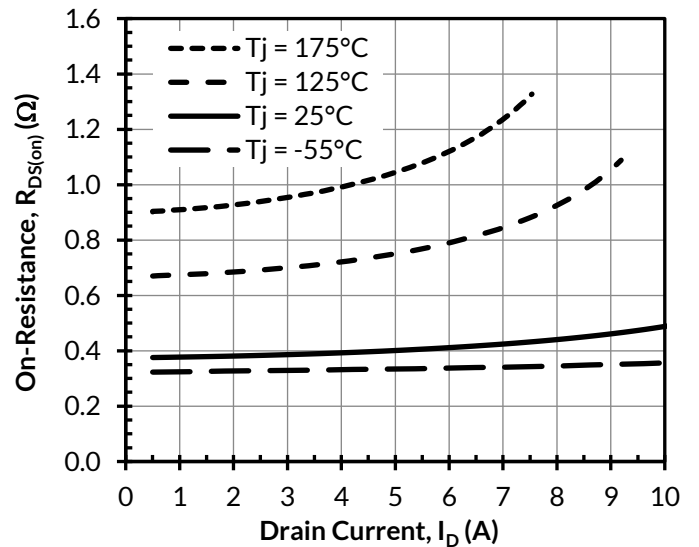


Figure 8. Typical drain-source on-resistances at $V_{GS} = 0\text{V}$

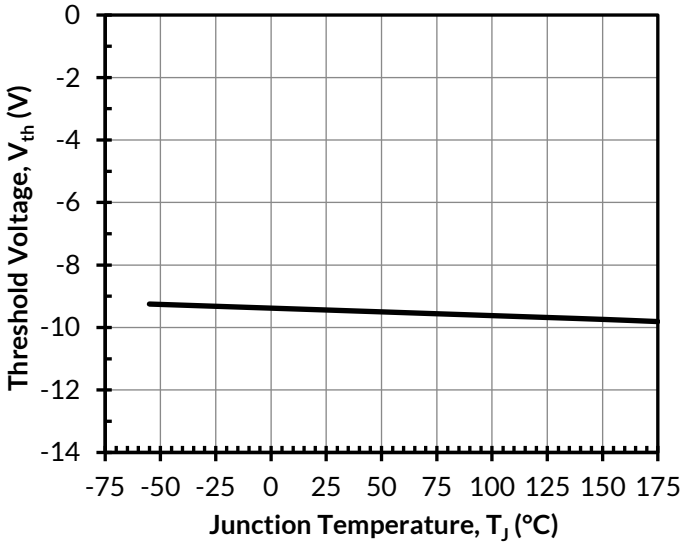


Figure 9. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 4.5mA$

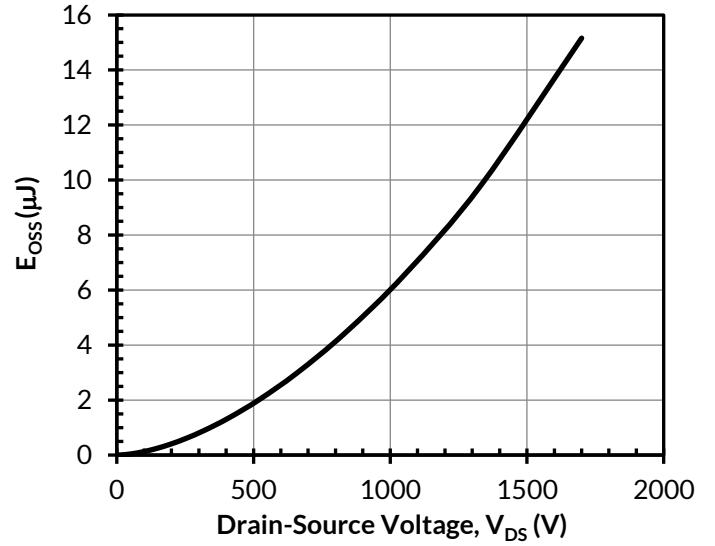


Figure 10. Typical stored energy in C_{OSS} at $V_{GS} = -20V$

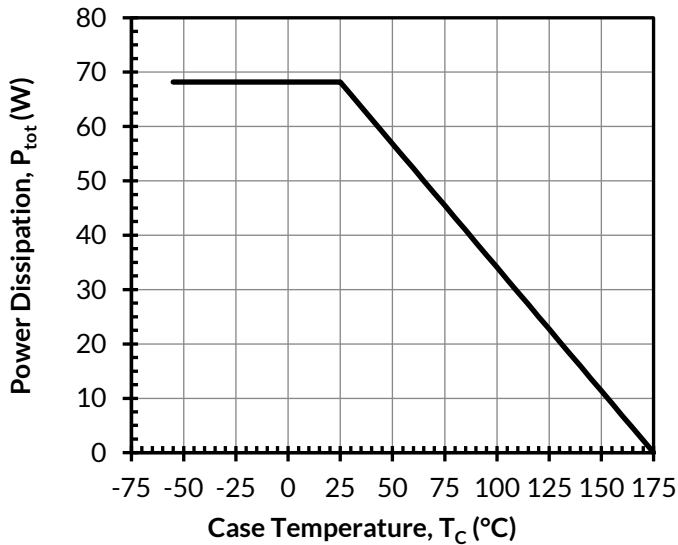


Figure 11. Total power Dissipation

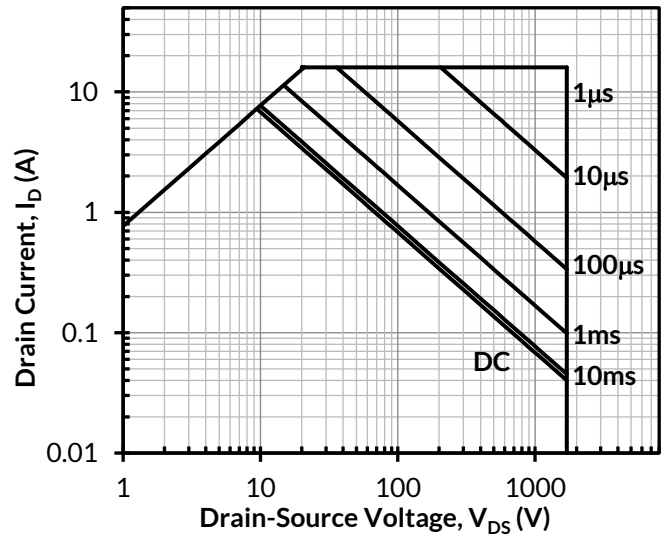


Figure 12. Safe operation area at $T_c = 25^\circ C$, Parameter t_p

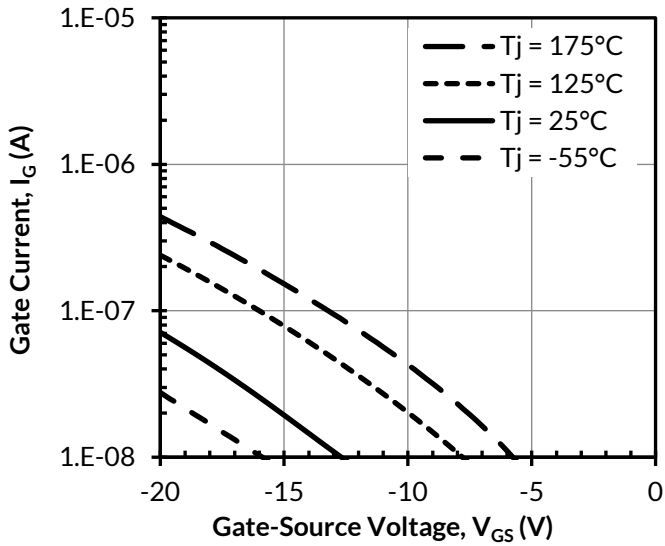


Figure 13. Typical gate leakage at $V_{DS} = 0V$

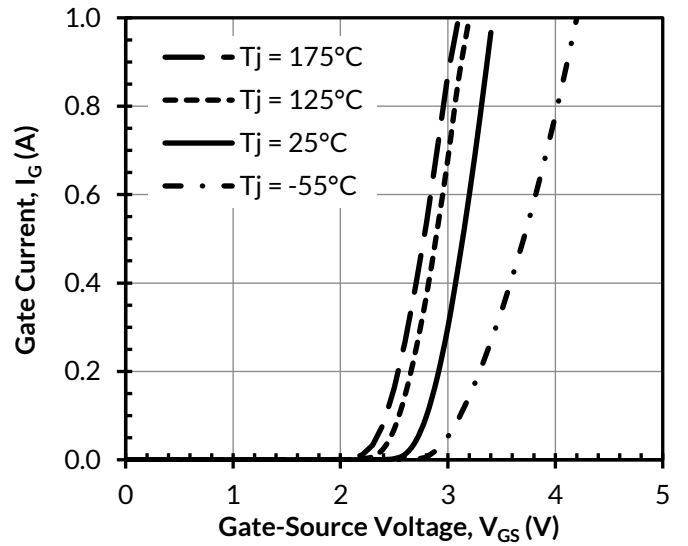


Figure 14. Typical gate forward current at $V_{DS} = 0V$

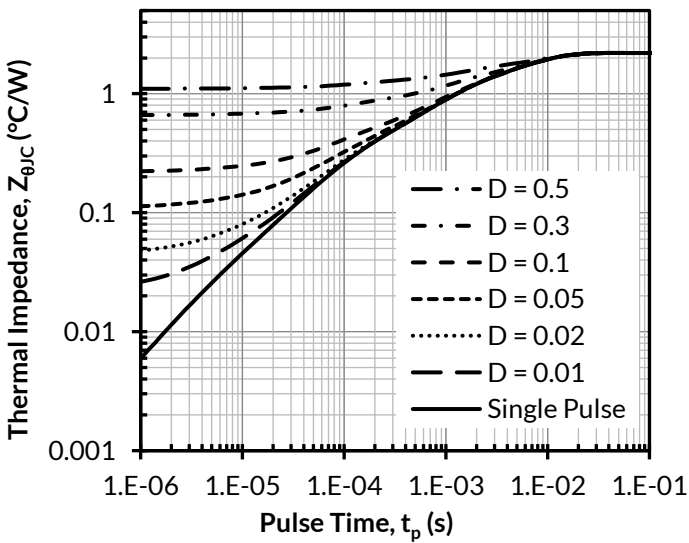


Figure 15. Maximum transient thermal impedance

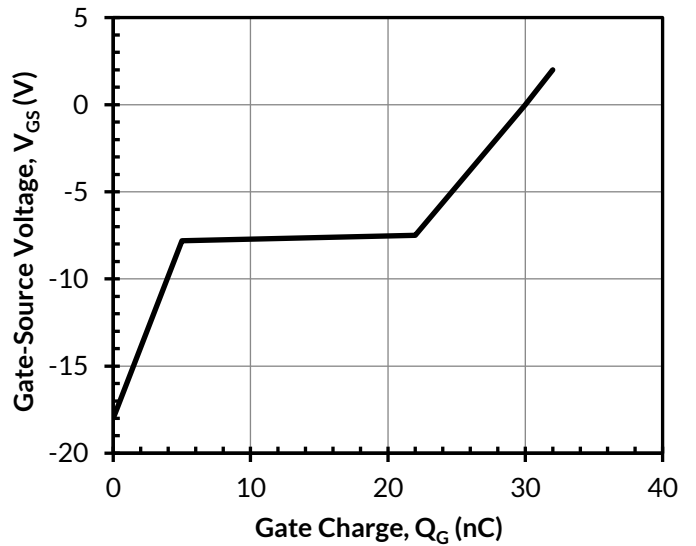


Figure 16. Typical gate charge at $V_{DS} = 1200V$ and $I_D = 5A$

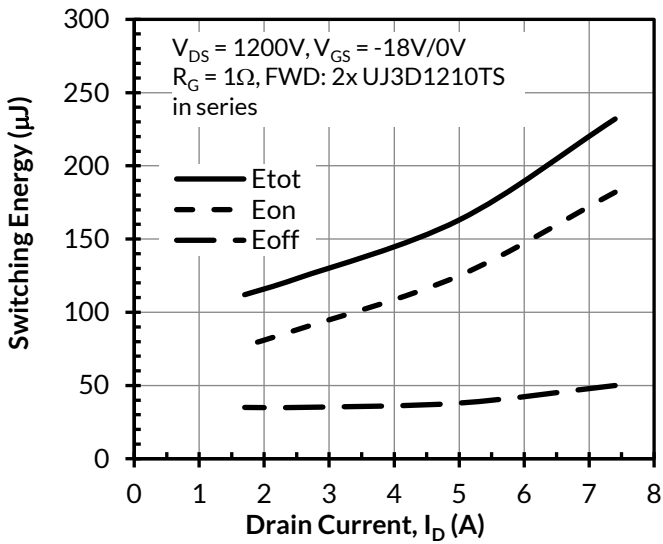


Figure 17. Clamped inductive switching energy vs. drain current at $T_J = 25^\circ C$

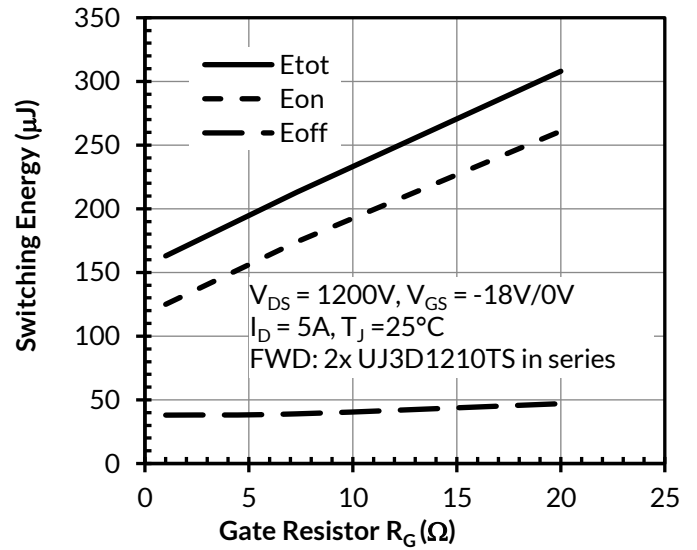


Figure 18. Clamped inductive switching energy vs. gate resistor R_G

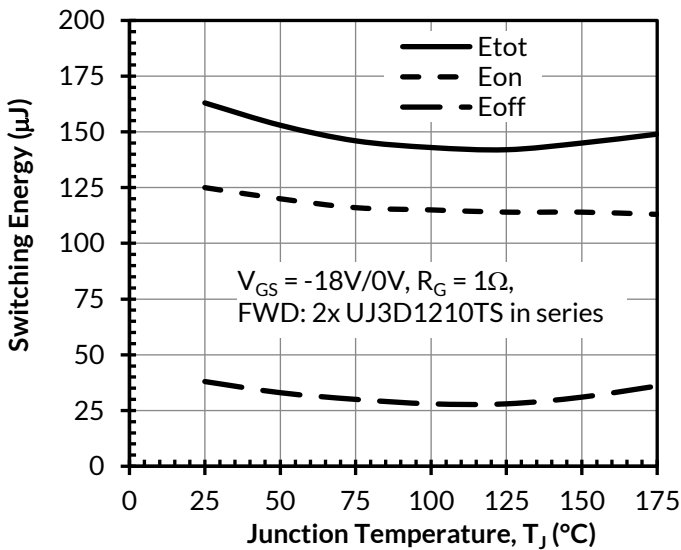


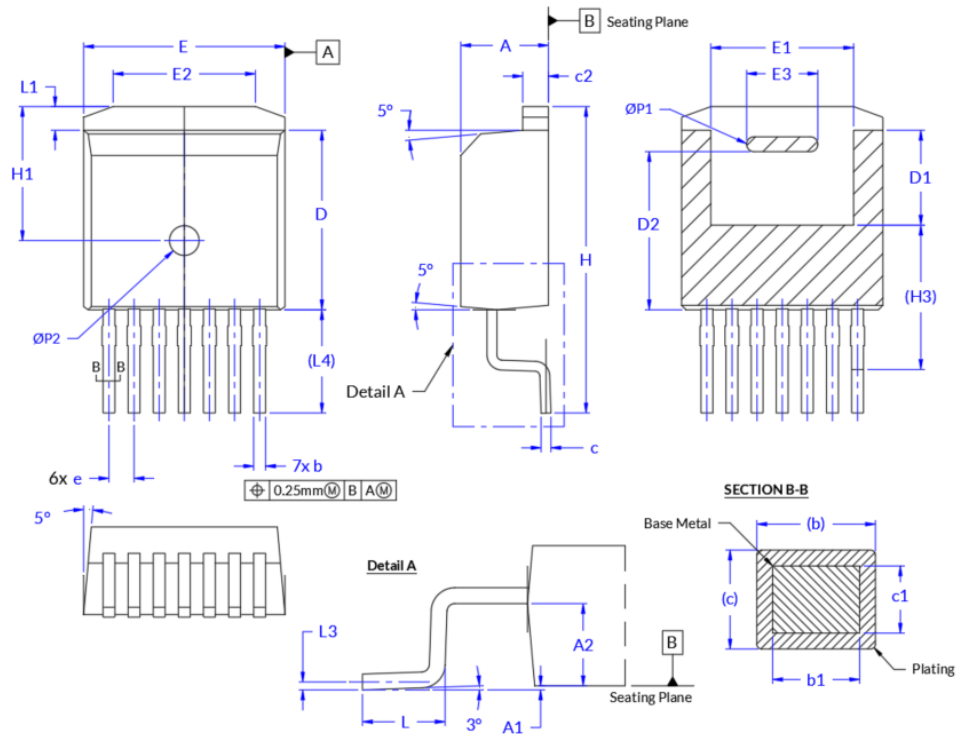
Figure 19. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 1200V$ and $I_D = 5A$

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PACKAGE OUTLINE


SYM	7L-D2PAK			
	MM		MIN	MAX
A	4.30	4.56	.169	.180
A1	0.00	0.25	.000	.010
A2	2.45	2.75	.096	.108
b	0.50	0.70	.020	.028
b1	0.50	-	.020	-
c	0.40	0.60	.016	.024
c1	0.40	-	.016	-
c2	1.20	1.40	.047	.055
D	8.93	9.23	.352	.363
D1	4.65	4.95	.183	.195
D2	7.90	8.10	.311	.319
e	1.27 BSC		.050 BSC	
E	10.08	10.28	.397	.405
E1	6.82	7.62	.269	.300
E2	6.50	8.60	.256	.339
E3	3.50	3.70	.138	.146
H	15.00	16.00	.591	.630
H1	6.68	6.88	.263	.271
H3	7.3 REF.		.287 REF	
L	1.90	2.50	.075	.098
L1	0.98	1.42	.039	.056
L3	0.25 BSC		.0098 BSC	
L4	5.22 REF		.205 REF	
ØP1	0.65	0.85	.026	.033
ØP2	1.40	1.60	.055	.063

Notes:

1. GENERAL TOLERANCE: ± 0.1 unless otherwise specified
2. CONTROLLING DIMENSION: **MILLIMETERS**
3. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
4. DIMENSION L IS MEASURED IN GAUGE LINE.
5. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
6. DIMENSION c1 AND b1 APPLIES TO BASE METAL ONLY

PART MARKING

G3, 650V / 1200V variant

UF3C: > 40 mOhm

UF3SC: ≤ 40 mOhm

G3, 1700V variant

UF3N: 400 mOhm

G4, 750V variant

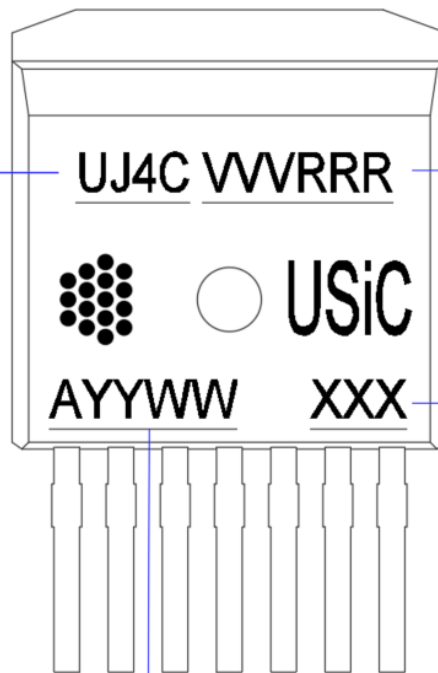
UJ4C: ≥ 23 mOhm

UJ4SC: < 23 mOhm

G4, 1200V variant

UF4C: > 30 mOhm

UF4SC: ≤ 30 mOhm



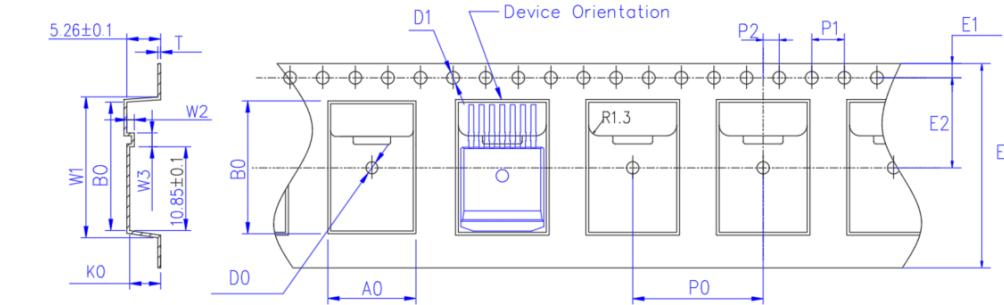
VVV : Voltage Rating
 RRR : Resistance Rating

Lot Code

A: Assembly Site
 YY: Year Code
 WW: Week code

PACKING TYPE

Carrier Tape

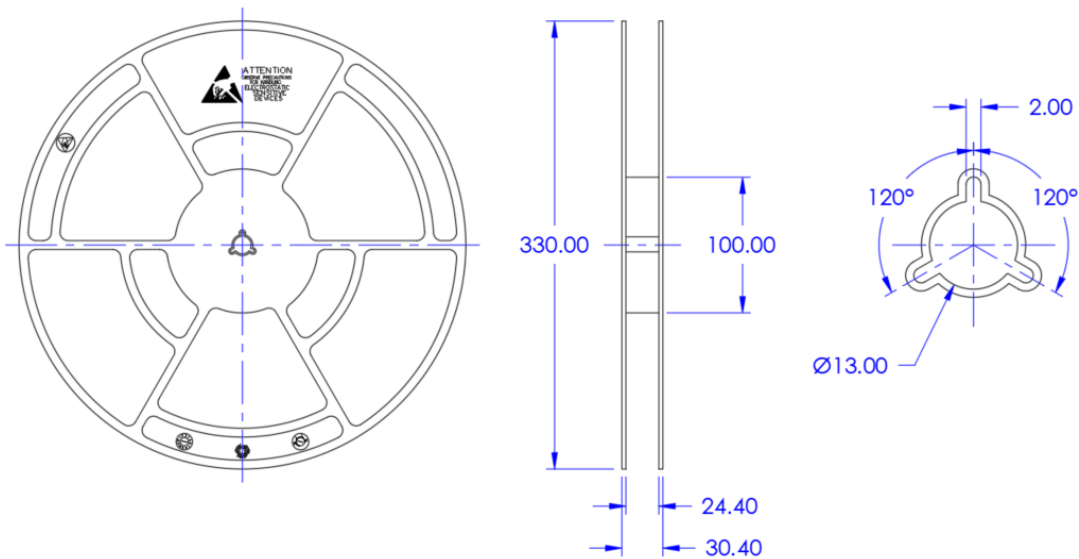


UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
D2PAK (24 mm)	10.80 ±0.10	16.30 ±0.10	4.70 ±0.10	1.50 ±0.10	1.50 $\begin{smallmatrix} +0.1 \\ -0 \end{smallmatrix}$	24.00 ±0.30	1.75 ±0.10	11.50 ±0.10	16.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.35 ±0.10

Exterior size	
Spec 1	W1 16.9±0.1
	W2 1.3±0.1
	W3 1.0±0.1
Spec 2	W1 17.2±0.1 (a)
	W2 1.8±0.1 (b)
	W3 0.85±0.1 (c)

Reel



All dimensions in millimeters
 Anti-Static Tape and Reel (T&R)
 Quantity per Reel: 800 units



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REVISION HISTORY

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
C	11/06/2023	Updated to Qorvo template Updated Package outline drawing based latest drawing revision	Glenn Galang
D	05/21/2024	Added illustration of device orientation on carrier tape (page 3)	Glenn Galang

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