Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO-263-7, 650 V, 42 mohm

UF3SC065040B7S

TAB

TO-263-7
CASE 418BA

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-263-7 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.

Features

- On-resistance $R_{DS(on)}$: 42 mΩ (Typ)
- Operating Temperature: 175 °C (Max)
- Excellent Reverse Recovery: Q_{rr} = 185 nC
- Low Body Diode V_{FSD}: 1.5 V
- Low Gate Charge: Q_G = 43 nC
- Threshold Voltage $V_{G(th)}$: 5 V (Typ) Allowing 0 to 15 V Drive
- Package Creepage and Clearance Distance > 6.1 mm
- Kelvin Source Pin for Optimized Switching Performance
- ESD Protected, HBM Class 2
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

Any controlled environment such as

- Telecom and Server Power
- Industrial Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

MARKING DIAGRAM

Tab
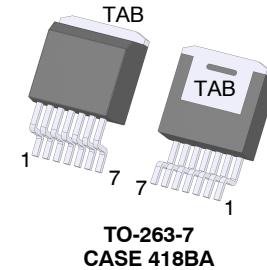
UF3SC065040B7S
AYYWW   ZZZ
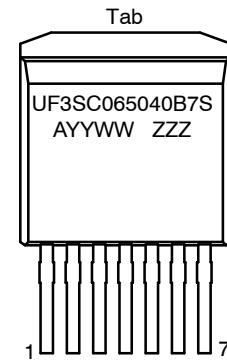
UF3SC065040B7S = Specific Device Code
A   = Assembly Location
YY   = Year
WW   = Work Week
ZZZ   = Lot ID

PIN CONNECTIONS
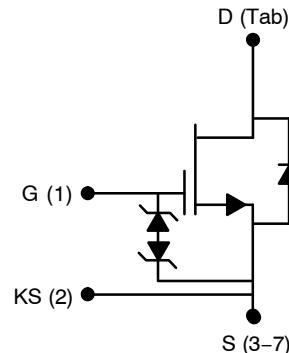
D (Tab)

G (1)

KS (2)

S (3–7)

ORDERING INFORMATION

April, 2025 – Rev. 3

1

Publication Order Number:
UF3SC065040B7S/D

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		650	V
Gate-source Voltage	V_{GS}	DC	−25 to +25	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25\ °C$	43	A
		$T_C = 100\ °C$	31.5	A
Pulsed Drain Current (Note 2)	I_{DM}	$T_C = 25\ °C$	125	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	L = 15 mH, I_{AS} = 3.19 A	76	mJ
Power Dissipation	P_{tot}	$T_C = 25\ °C$	195	W
Maximum Junction Temperature	$T_{J, max}$		175	°C
Operating and Storage Temperature	T_J, T_{STG}		−55 to 175	°C
Reflow Soldering Temperature	T_{solder}	Reflow MSL 3	245	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Limited by $T_{J, max}$.
2. Pulse width t_p limited by $T_{J, max}$.
3. Starting $T_J = 25\ °C$.

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		–	0.59	0.77	°C/W

UF3SC065040B7S

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
Drain-source Breakdown Voltage	BV_{DS}	V_{GS} = 0 V, I_D = 1 mA	650	–	–	V
Total Drain Leakage Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25 °C	–	0.7	150	µA
		V_{DS} = 650 V, V_{GS} = 0 V, T_J = 175°C	–	10	–	
Total Gate Leakage Current	I_{GSS}	V_{DS} = 0 V, T_J = 25 °C, V_{GS} = −20 V / +20 V	–	6	±20	µA
Drain-source On-resistance	$R_{DS(on)}$	V_{GS} = 12 V, I_D = 30 A, T_J = 25°C	–	42	52	mΩ
		V_{GS} = 12 V, I_D = 30 A, T_J = 125°C	–	59	–	
		V_{GS} = 12 V, I_D = 30 A, T_J = 175°C	–	78	–	
Gate Threshold Voltage	$V_{G(th)}$	V_{DS} = 5 V, I_D = 10 mA	4	5	6	V
Gate Resistance	R_G	f = 1 MHz, open drain	–	4.5	–	Ω
TYPICAL PERFORMANCE – REVERSE DIODE						
Diode Continuous Forward Current (Note 1)	I_S	T_C = 25 °C	–	–	43	A
Diode Pulse Current (Note 2)	$I_{S, pulse}$	T_C = 25 °C	–	–	125	A
Forward Voltage	V_{FSD}	V_{GS} = 0 V, I_S = 20 A, T_J = 25 °C	–	1.5	1.75	V
		V_{GS} = 0 V, I_S = 20 A, T_J = 175 °C	–	1.8	–	
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 30 A, V_{GS} = −5 V, R_{G_EXT} = 10 Ω, di/dt = 1500 A/µs, T_J = 25 °C	–	185	–	nC
Reverse Recovery Time	t_{rr}		–	31	–	ns
Reverse Recovery Charge	Q_{rr}	V_{DS} = 400 V, I_S = 30 A, V_{GS} = −5 V, R_{G_EXT} = 10 Ω, di/dt = 1500 A/µs, T_J = 150 °C	–	155	–	nC
Reverse Recovery Time	t_{rr}		–	30	–	ns
TYPICAL PERFORMANCE – DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = 0 V, f = 100 kHz	–	1500	–	pF
Output Capacitance	C_{oss}		–	200	–	
Reverse Transfer Capacitance	C_{rss}		–	2.2	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	146	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	325	–	
C_{OSS} Stored Energy	E_{oss}	V_{DS} = 400 V, V_{GS} = 0 V	–	11.7	–	µJ
Total Gate Charge	Q_G	V_{DS} = 400 V, I_D = 30 A, V_{GS} = −5 V to 12 V	–	43	–	nC
Gate-drain Charge	Q_{GD}		–	11	–	
Gate-source Charge	Q_{GS}		–	19	–	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 30 A, Gate Driver = −5 V to +12 V, Turn-on $R_{G, EXT}$ = 8.5 Ω, Turn-off $R_{G, EXT}$ = 22 Ω, Inductive Load, FWD: same device with V_{GS} = −5 V, R_G = 10 Ω, T_J = 25 °C	–	25	–	ns
Rise Time	t_r		–	27	–	
Turn-off Delay Time	$t_{d(off)}$		–	45	–	
Fall Time	t_f		–	12	–	
Turn-on Energy	E_{ON}		–	249	–	µJ
Turn-off Energy	E_{OFF}		–	28	–	
Total Switching Energy	E_{TOTAL}		–	277	–	

UF3SC065040B7S

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 30 A, Gate Driver = −5 V to +12 V, Turn-on $R_{G, EXT}$ = 8.5 Ω, Turn-off $R_{G, EXT}$ = 22 Ω, Inductive Load, FWD: same device with V_{GS} = −5 V, R_G = 10 Ω, T_J = 150 °C	–	22	–	ns
Rise Time	t_r		–	24	–	
Turn-off Delay Time	$t_{d(off)}$		–	47	–	
Fall Time	t_f		–	9	–	
Turn-on Energy	E_{ON}		–	227	–	µJ
Turn-off Energy	E_{OFF}		–	13	–	
Total Switching Energy	E_{TOTAL}		–	240	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS
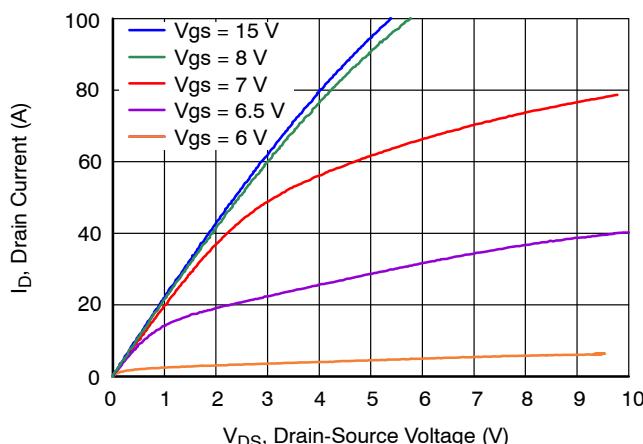
**Figure 1. Typical Output Characteristics
at T$_J$ = −55 °C, t$_p$ < 250 μs**
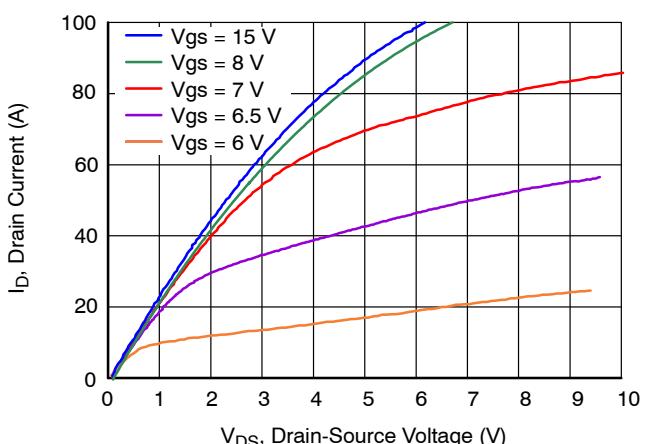
**Figure 2. Typical Output Characteristics
at T$_J$ = 25 °C, t$_p$ < 250 μs**
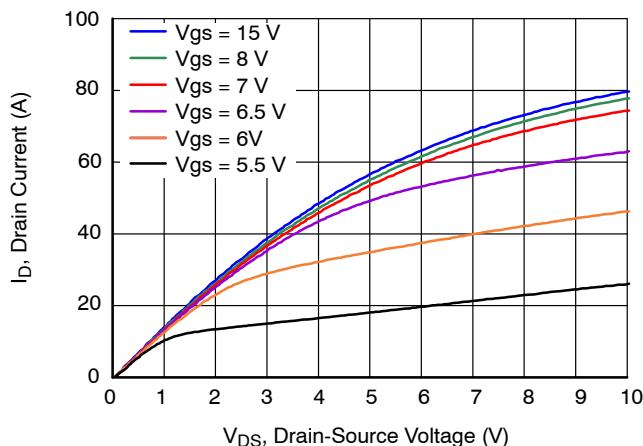
**Figure 3. Typical Output Characteristics
at T$_J$ = 175 °C, t$_p$ < 250 μs**
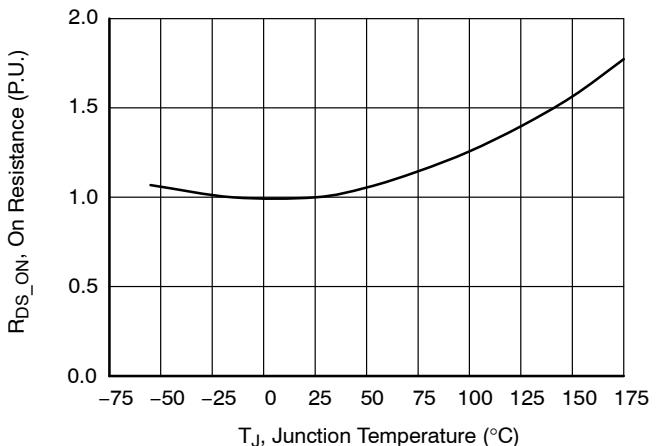
**Figure 4. Normalized On-Resistance
vs. Temperature at V$_{GS}$ = 12 V and I$_D$ =30 A**
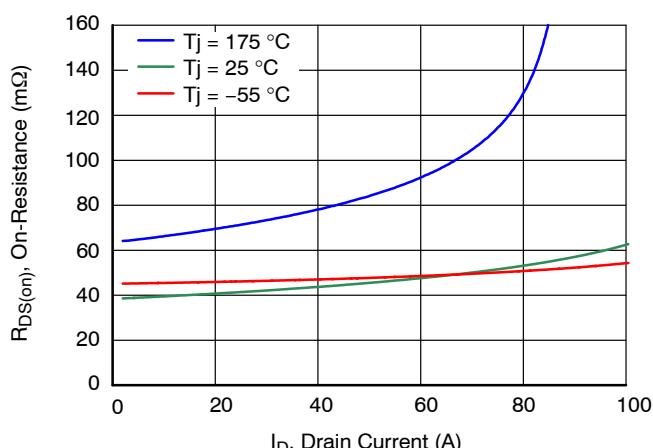
**Figure 5. Typical Drain-Source On-Resistances
at V$_{GS}$ = 12 V**
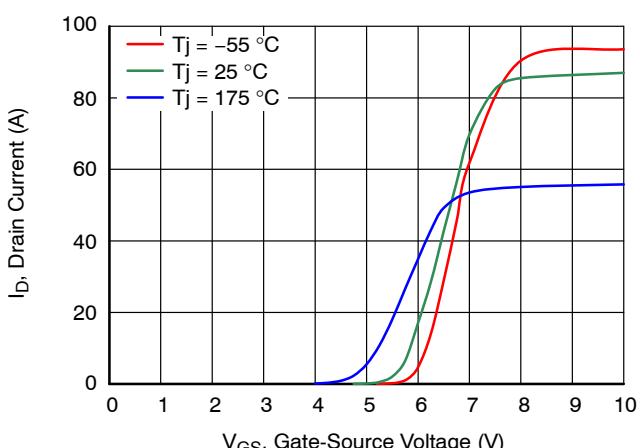
**Figure 6. Typical Transfer Characteristics
at V$_{DS}$ = 5 V**

TYPICAL PERFORMANCE DIAGRAMS (continued)
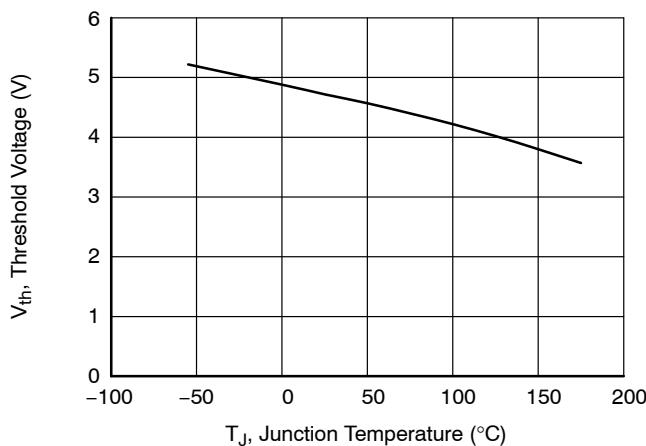
Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 10 mA
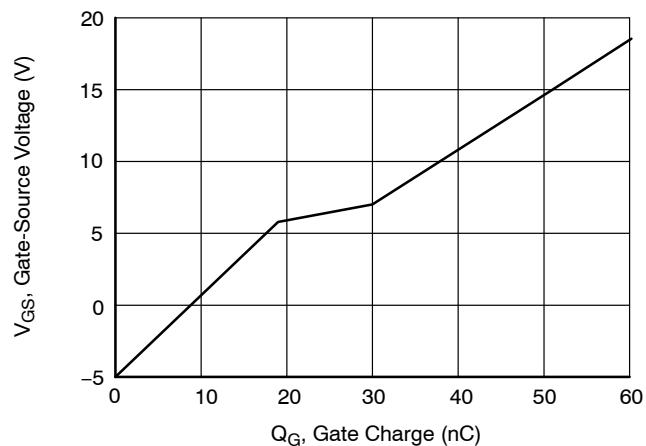
Figure 8. Typical Gate Charge at V_{DS} = 400 V and I_D = 30 A
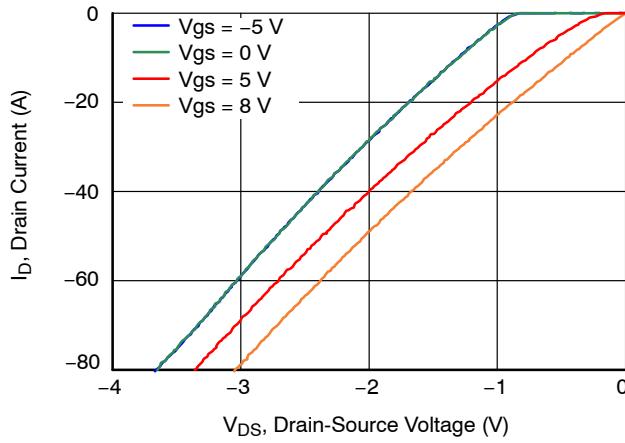
Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C
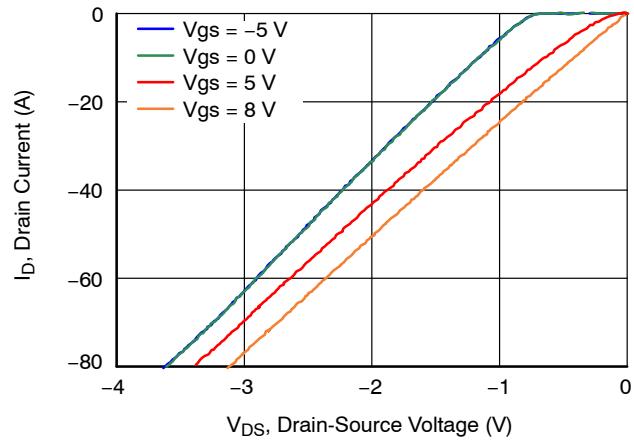
Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C
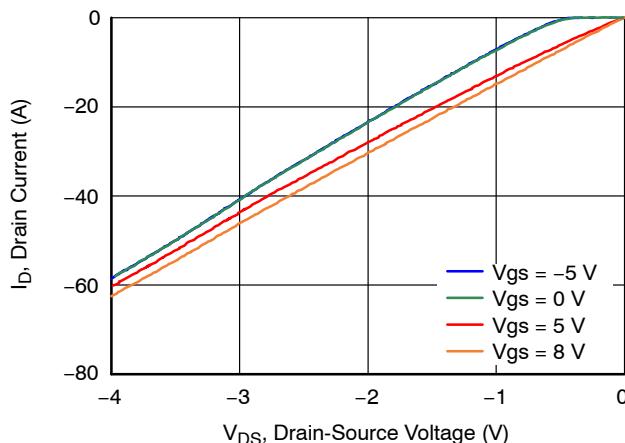
Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C
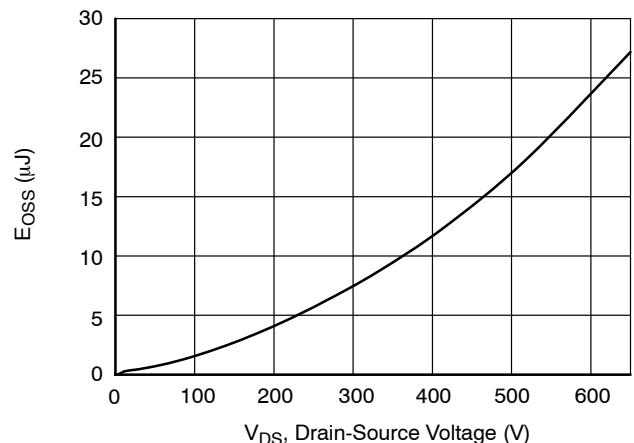
Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS (continued)
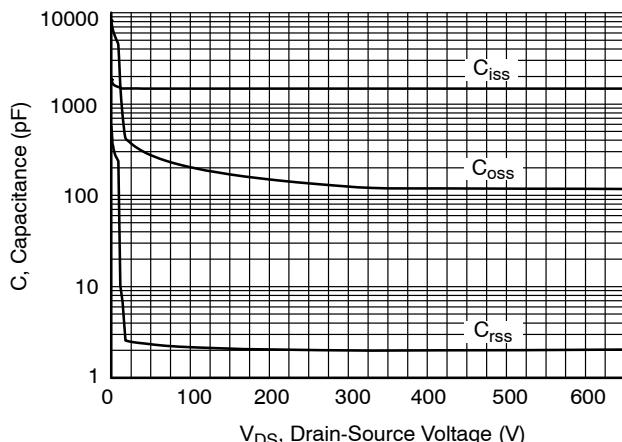
Figure 13. Typical Capacitances at f = 100 kHz and V$_{GS}$ = 0 V
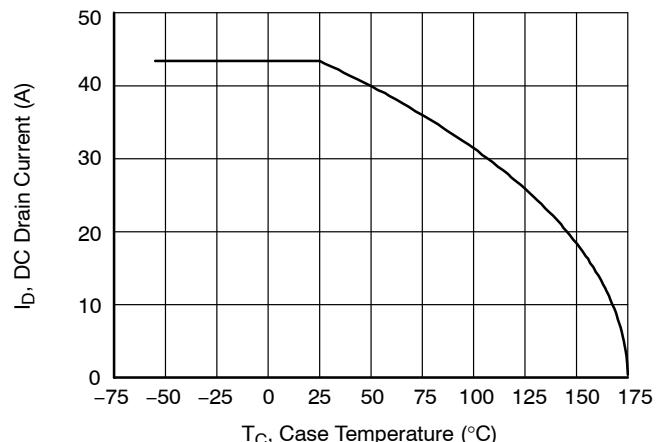
Figure 14. DC Drain Current Derating
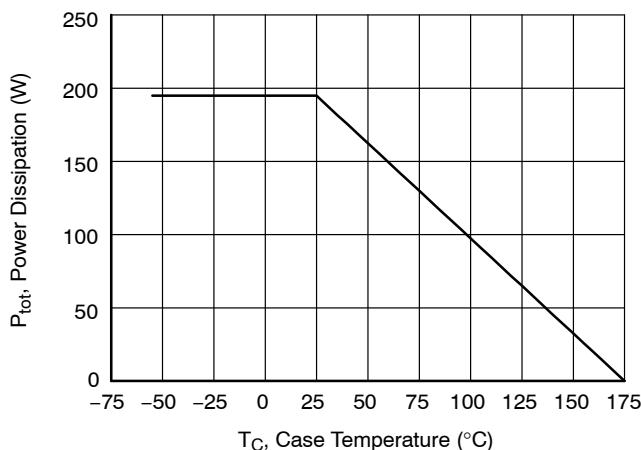
Figure 15. Total Power Dissipation
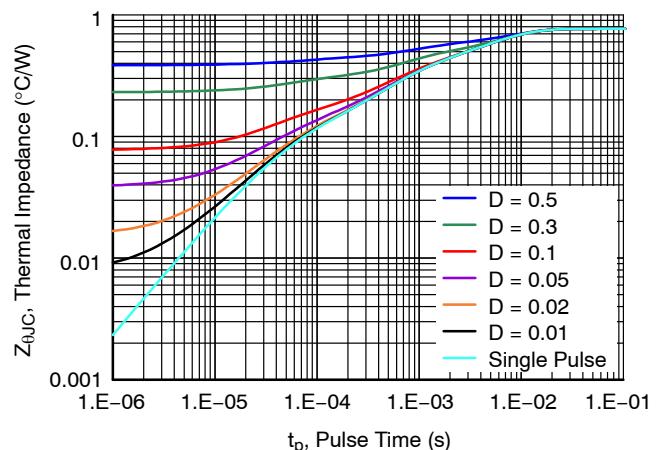
Figure 16. Maximum Transient Thermal Impedance
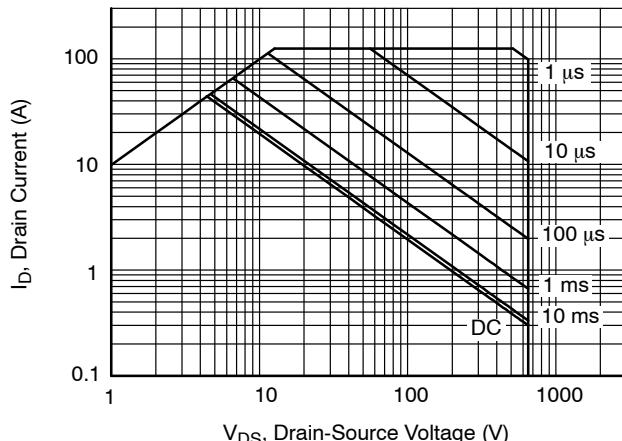
Figure 17. Safe Operation Area at T$_C$ = 25 °C, D = 0, Parameter t$_p$
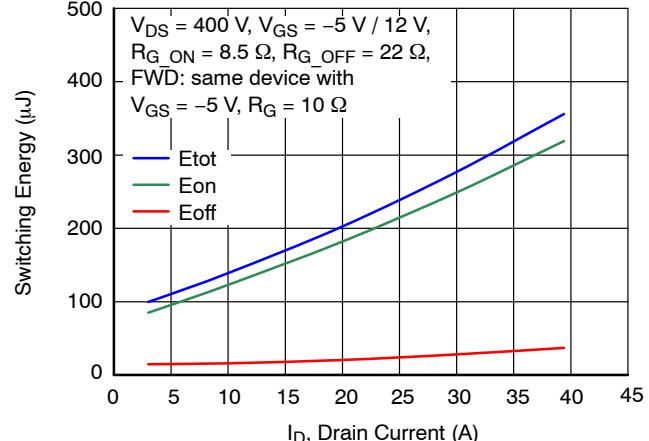
Figure 18. Clamped Inductive Switching Energy vs. Drain Current at T$_J$ = 25 °C

TYPICAL PERFORMANCE DIAGRAMS (continued)
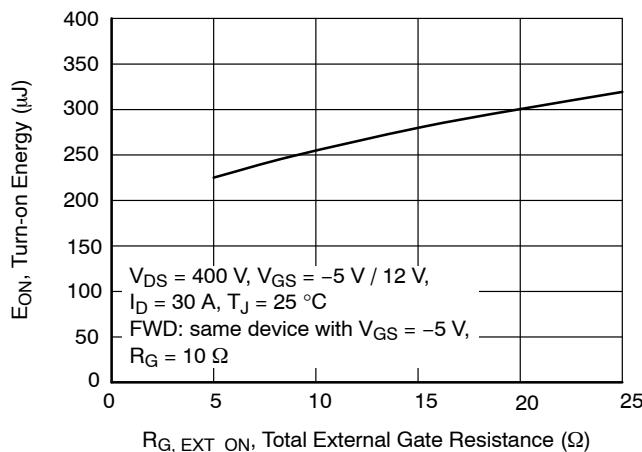
Figure 19. Clamped Inductive Switching Turn-on Energy vs. R_{G, EXT_ON}
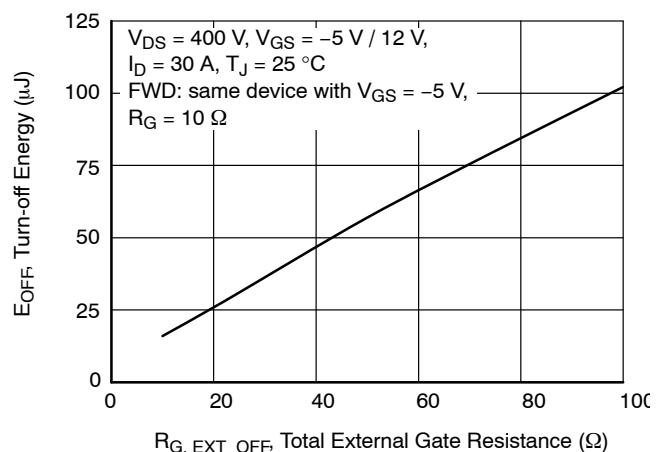
Figure 20. Clamped Inductive Switching Turn-off Energy vs. R_{G, EXT_OFF}
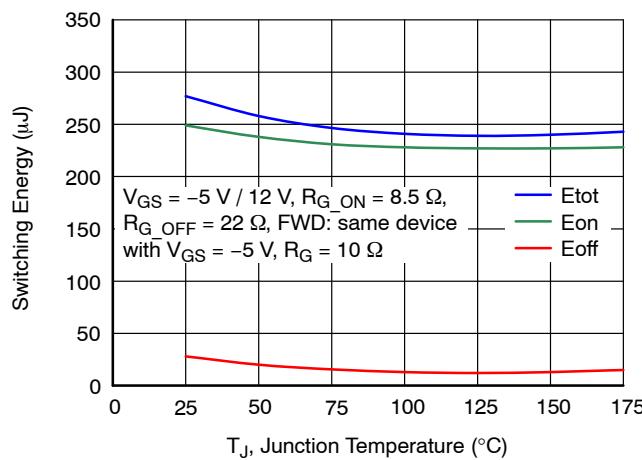
Figure 21. Clamped Inductive Switching Energy vs. Junction Temperature at V_{DS} = 400 V and I_D = 30 A
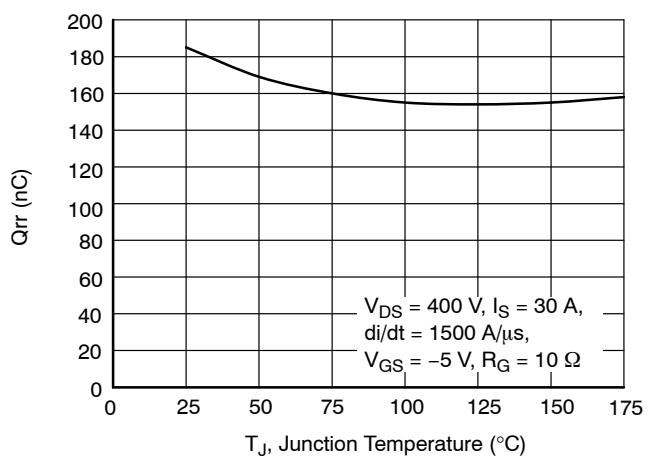
Figure 22. Reverse Recovery Charge Qrr vs. Junction Temperature

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com

ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
UF3SC065040B7S	UF3SC065040B7S	TO-263-7	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
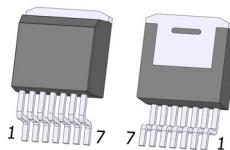
TO−263−7 10.18x9.08x4.43, 1.27P
CASE 418BA
ISSUE B

DATE 17 APR 2025

Section B-B

Detail A

Gauge Plane

SYM	MILLIMETERS		
	Min	Nom	Max
A	4.30	4.43	4.56
A1	0.00	0.13	0.25
A2	2.45	2.60	2.75
b	0.50	0.60	0.70
b1	0.50	-	-
c	0.40	0.50	0.60
c1	0.40	-	-
c2	1.20	1.30	1.40
D	8.93	9.08	9.23
D1	5.85	6.00	6.15
D2	7.90	8.00	8.10
e	1.27 BSC		
E	10.08	10.18	10.28
E1	6.82	7.22	7.62
E2	6.50	7.55	8.60
E3	3.50	3.60	3.70
H	15.00	15.50	16.00
H1	6.78 REF		
H3	7.30 REF.		
L	1.90	2.20	2.50
L1	0.98	1.20	1.42
L3	0.25 BSC		
L4	5.22 REF		
ØP1	0.65	0.75	0.85
ØP2	1.50 REF		
θ	5°		
θ1	3°		
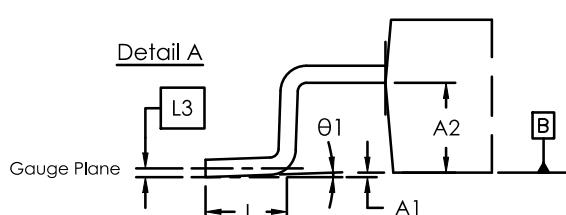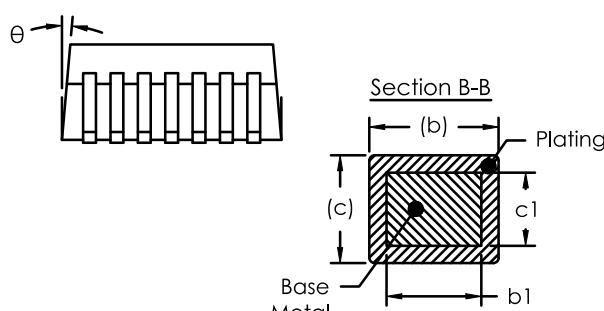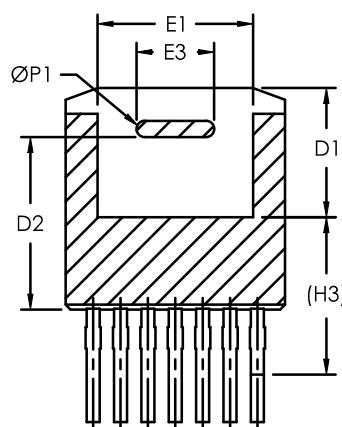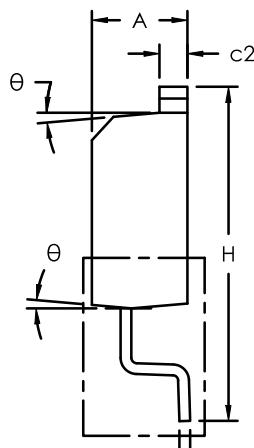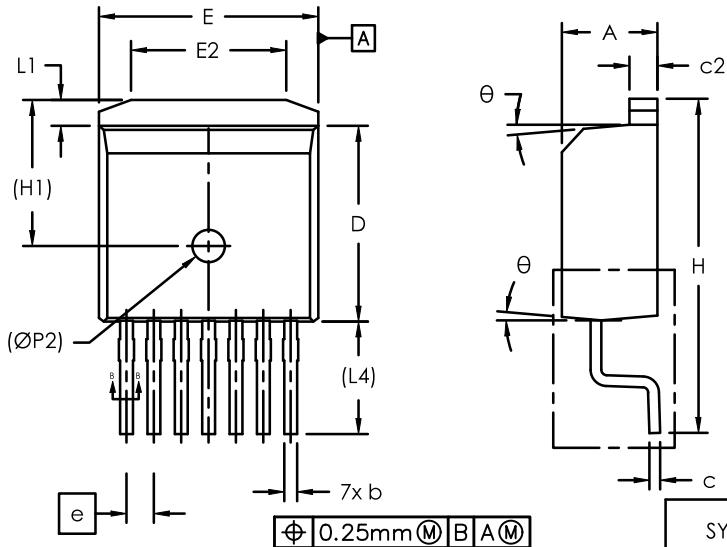
Notes:
1. Dimensioning and Tolerancing as per ASME Y14.5M, 2018.
2. Controlling Dimension : Millimeters
3. Package body sides exclude mold flash and gate burrs.
4. Dimension L is measured on gauge plane.
5. Dimension c1 and b1 applies to base metal only.

DOCUMENT NUMBER:	98AON13800G		
DESCRIPTION:	TO−263−7 10.18x9.08x4.43, 1.27P		PAGE 1 OF 2

RECOMMENDED PCB FOOTPRINT

10.48
4.00
2.68
6.30
(7.90)
16.40
6.20
8.52
3.90
1.27
6x
.90
7x
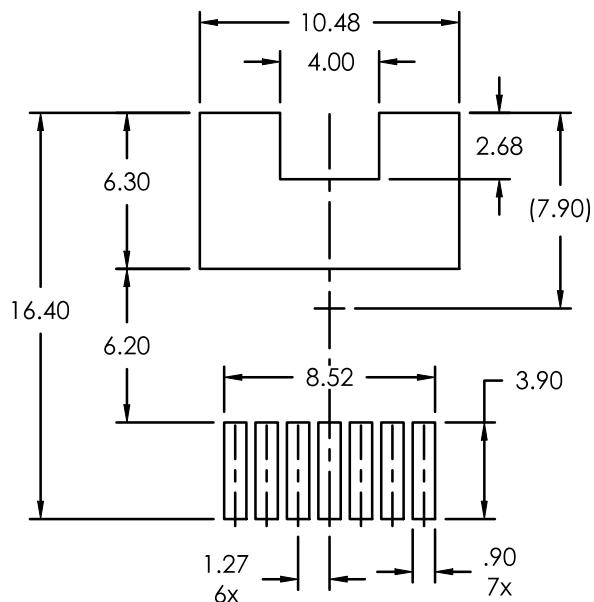
RECOMMENDED STENCIL APERTURE

10.28
4.20
2.53
3.27
6.10
16.25
4.65
1.70
8.42
3.80
1.27
6x
.80
7x
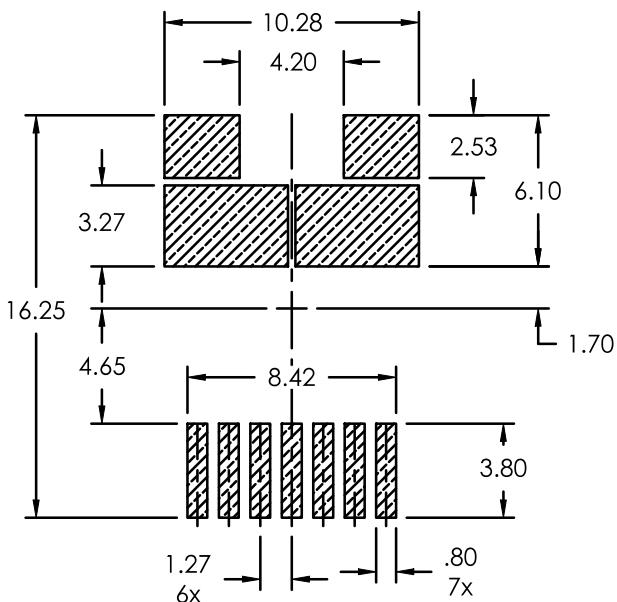
NOTE: LAND PATTERN AND STENCIL APERTURE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE. END-USER PCB DESIGN RULES
AND TOLERANCES SHOULD ALWAYS PREVAIL.

PCB FOOTPRINT with PACKAGE OVERLAY
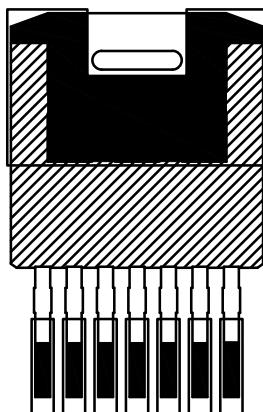
■ AREA IN CONTACT WITH
THE PACKAGE

▨ MOLD COMPOUND

DOCUMENT NUMBER:	98AON13800G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**TO−263−7 10.18x9.08x4.43, 1.27P**		**PAGE 2 OF 2**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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