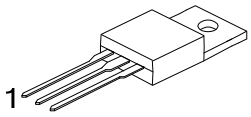
9.2A, 100V N-CHANNEL POWER MOSFET



TO-220

■ DESCRIPTION

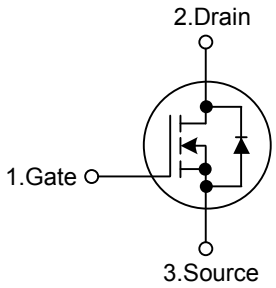
The UTC **UF520** is an N-channel enhancement power MOSFET using UTC's advanced technology to provide the customers with high Input Impedance and high switching speed.

This UTC **UF520** is suitable for motor drivers, switching convertors, switching regulators, relay drivers and drivers for high power bipolar switching transistors.

■ FEATURES

* $R_{DS(ON)}$=0.25Ω @ V_{GS}=10V,I_D=5.6A
* High Input Impedance
* High Switching Speed

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF520L-TA3-T	UF520G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UF520L-TA3-T (1)Packing Type (2)Package Type (3)Lead Free	(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS (T_J=25°C, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	100	V
Gate-Source Voltage			V_{GSS}	±20	V
Drain Current	Continuous	T_C=25°C	I_D	9.2	A
		T_C=100°C		6.5	A
	Pulsed (Note 2)		I_{DM}	37	A
Single Pulsed Avalanche Energy (Note 3)			E_{AS}	36	mJ
Power Dissipation			P_D	50	W
Junction Temperature			T_J	+150	°C
Storage Temperature			T_{STG}	-55~+175	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve
3. V_{DD}=25V, starting T_J=25°C, L=640mH, R_G=25Ω, peak I_{AS}=9.2A

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	80	°C/W
Junction to Case	θ_{JC}	2.5	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=95V, V_{GS}=0V			250	μA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.6A (Note 1)		0.25	0.27	Ω
On State Drain Current (Note 1)	$I_{D(ON)}$	V_{GS}=10V, V_{DS}>$I_{D(ON)}$×$R_{DS(ON)}$MAX	9.2			A
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		350		pF
Output Capacitance	C_{OSS}			130		pF
Reverse Transfer Capacitance	C_{RSS}			25		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	V_{GS}=10V, I_D=9.2A, V_{DS}=0.8*Rated BV_{DSS}, $I_{G(REF)}$=1.5mA (Note 2)		10	30	nC
Gate to Source Charge	Q_{GS}			2.5		nC
Gate to Drain Charge	Q_{GD}			2.5		nC
Turn-ON Delay Time	$t_{D(ON)}$	V_{DD}=50V, I_D≈9.2A, R_G=18Ω, R_L=5.5 Ω (Note 3)		9	13	ns
Rise Time	t_R			30	63	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			18	70	ns
Fall-Time	t_F			20	59	ns

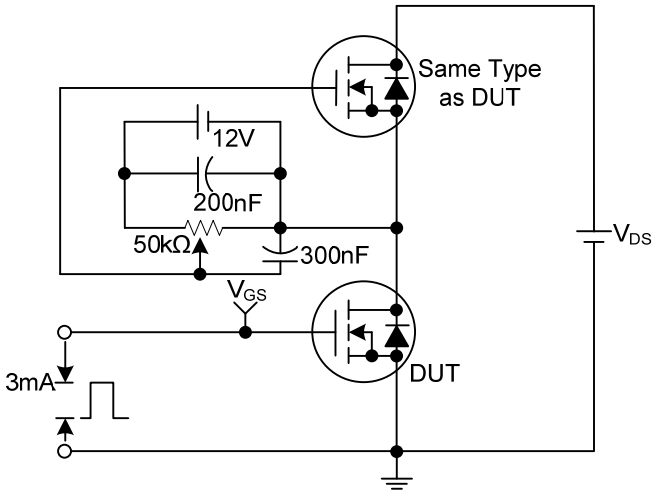
Notes: 1. Pulse test: pulse width≤300μs, duty cycle≤2%
2. Gate Charge is Essentially Independent of Operating Temperature
3. MOSFET Switching Times are Essentially Independent of Operating Temperature

■ SOURCE TO DRAIN DIODE SPECIFICATIONS

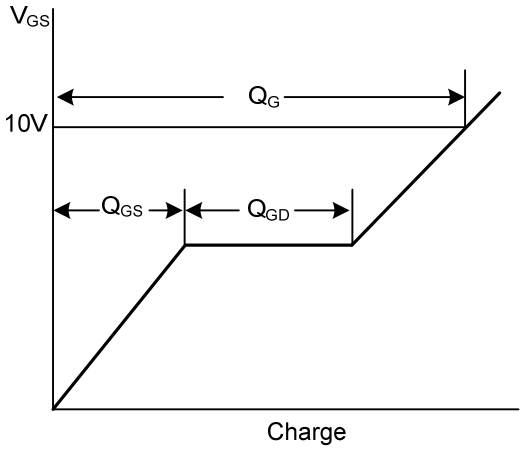
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage	V_{SD}	T_J=25°C,I_{SD}=9.2A,V_{GS}=0V (Note 1)			2.5	V
Continuous Source to Drain Current	I_{SD}	Note 3			9.2	A
Pulse Source to Drain Current (Note 2)	I_{SDM}				37	A

Note : 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.
2. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve
3. Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode.

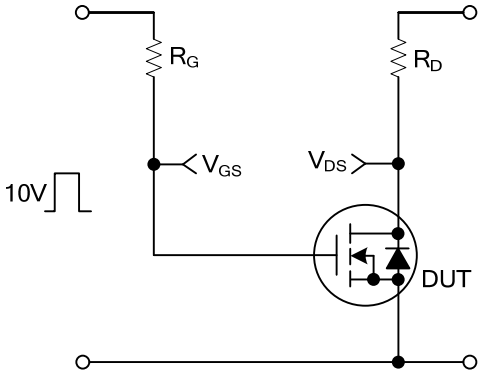
■ TEST CIRCUITS AND WAVEFORMS



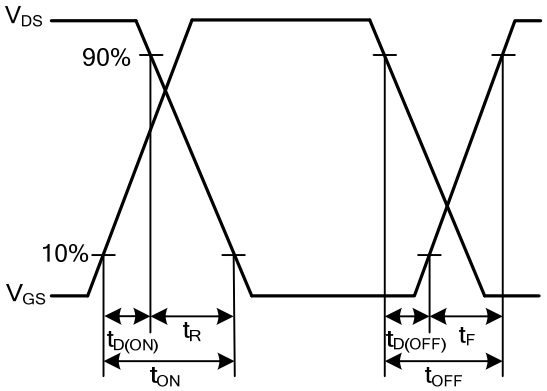
Gate Charge Test Circuit



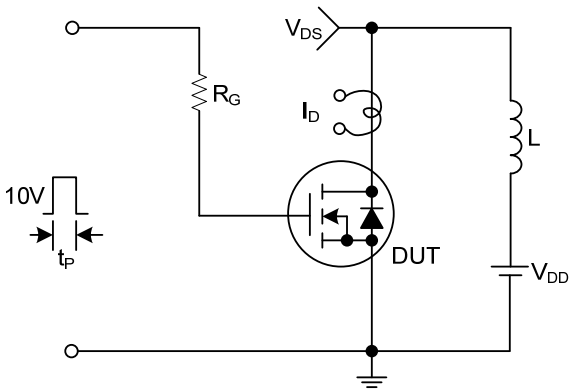
Gate Charge Waveforms



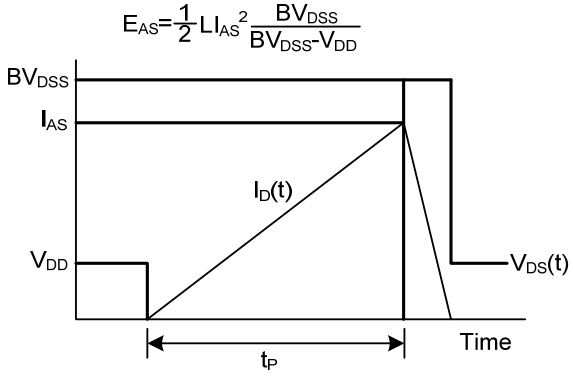
Resistive Switching Test Circuit



Resistive Switching Waveforms

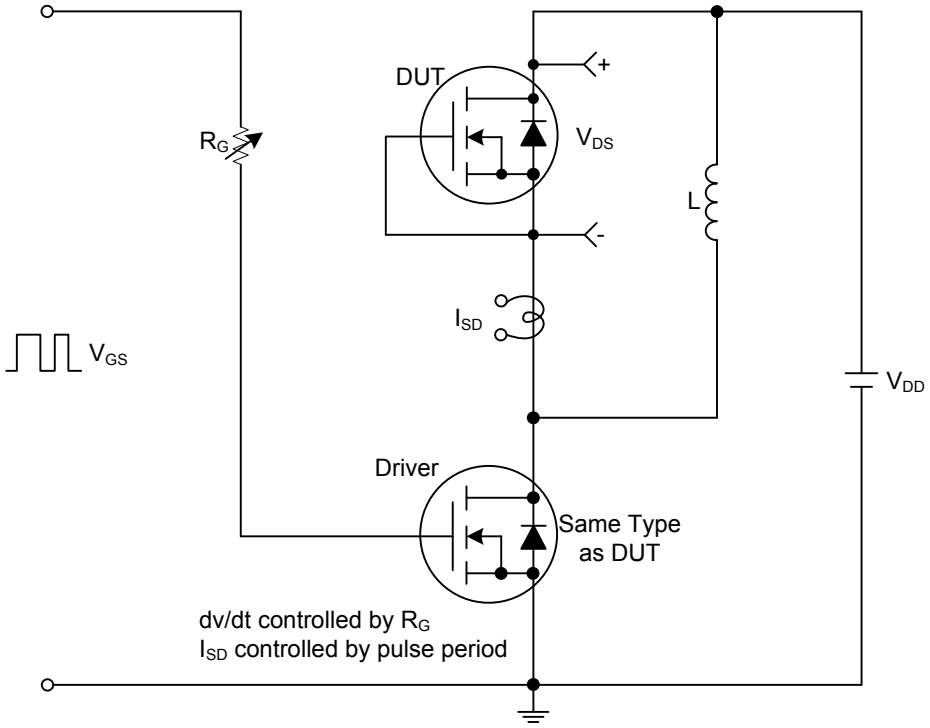


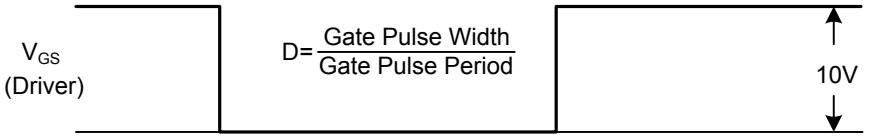
Unclamped Inductive Switching Test Circuit

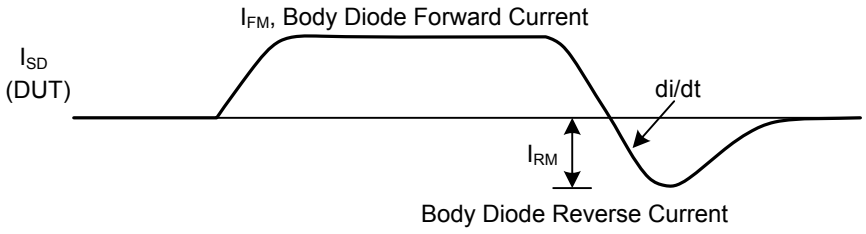


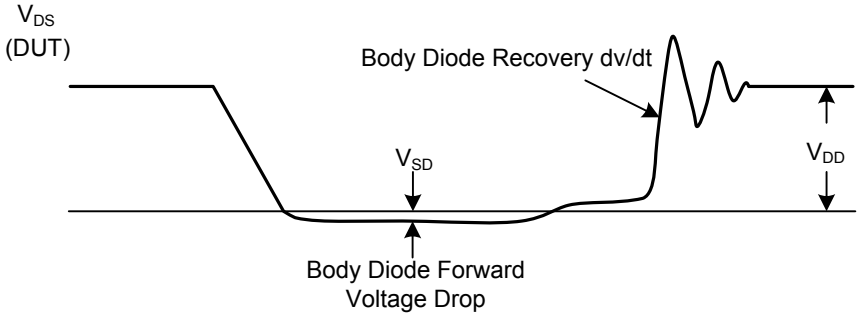
Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)









Peak Diode Recovery dv/dt Test Circuit and Waveforms