

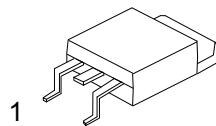
UF740-V

Power MOSFET

10A, 400V N-CHANNEL POWER MOSFET

■ DESCRIPTION

The UTC **UF740-V** is a N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

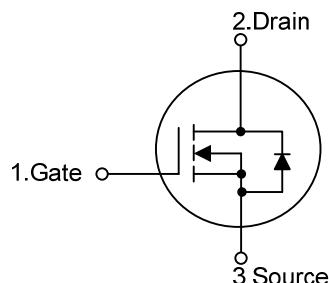


TO-263

■ FEATURES

- * $R_{DS(ON)} < 0.44\Omega$ @ $V_{GS} = 10V$, $I_D = 5.0A$
- * Single Pulse Avalanche Energy Rated
- * Rugged - SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

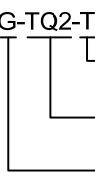
■ SYMBOL



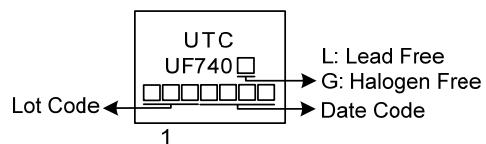
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen-Free		1	2	3	
UF740L-TQ2-T	UF740G-TQ2-T	TO-263	G	D	S	Tube
UF740L-TQ2-R	UF740G-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UF740G-TQ2-T  <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package 	<ul style="list-style-type: none"> (1) T: Tube, R: Tape Reel (2) TQ2: TO-263 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



UF740-V

Power MOSFET

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	400	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	10	A
	Pulsed (Note 2)	I_{DM}	20	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	442	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.6	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)		P_D	125	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10 \text{ mH}$, $I_{AS} = 9.4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 10\text{A}$, $dI/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C/W}$
Junction to Case	θ_{JC}	1	$^\circ\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

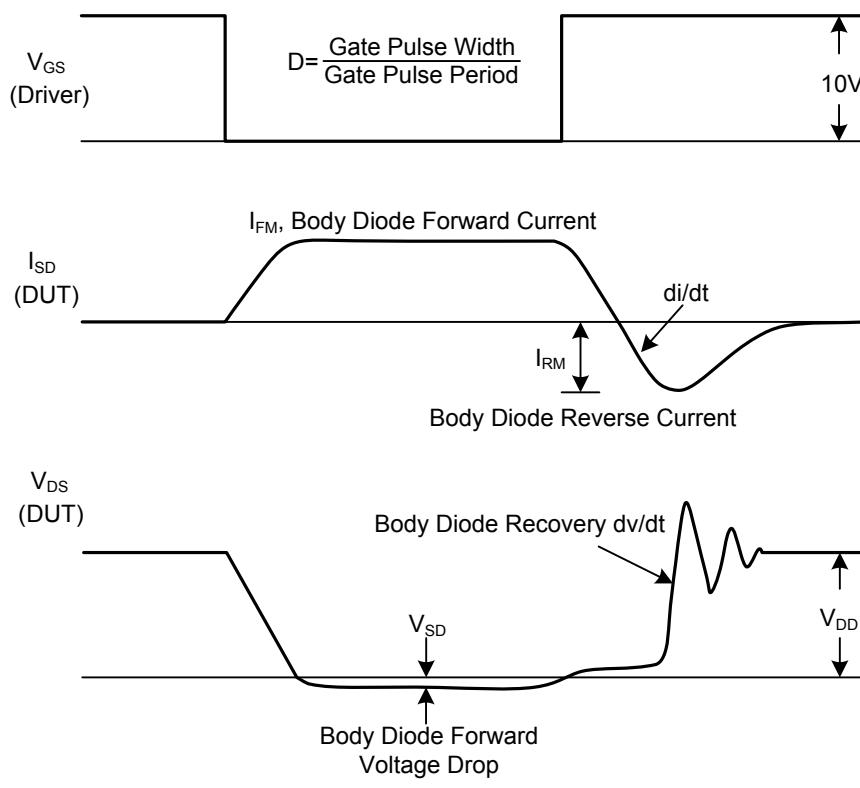
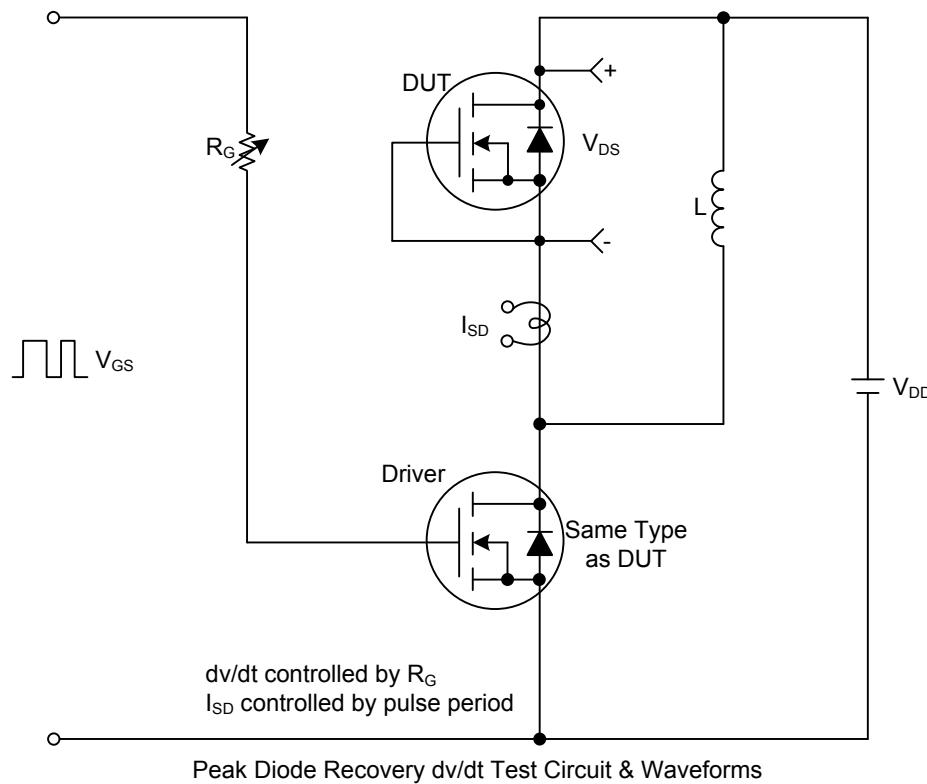
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	400			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=400\text{V}$, $V_{GS}=0\text{V}$		25	μA	
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$		+100	nA
	Reverse		$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$		-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=5.0\text{A}$			0.44	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		1065		pF
Output Capacitance	C_{OSS}			172		pF
Reverse Transfer Capacitance	C_{RSS}			32		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=200\text{V}$, $V_{GS}=10\text{V}$, $I_D=10\text{A}$, $I_G=1\text{mA}$ (Note 1, 2)		36		nC
Gate to Source Charge	Q_{GS}			8		nC
Gate to Drain Charge	Q_{GD}			10		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		30		ns
Rise Time	t_R			72		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			380		ns
Fall-Time	t_F			130		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				10	A
Maximum Body-Diode Pulsed Current	I_{SM}				20	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=10\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=10\text{A}$, $V_{GS}=0\text{V}$,		270		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$dI_{rr}/dt=100\text{A}/\mu\text{s}$		2.6		μC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

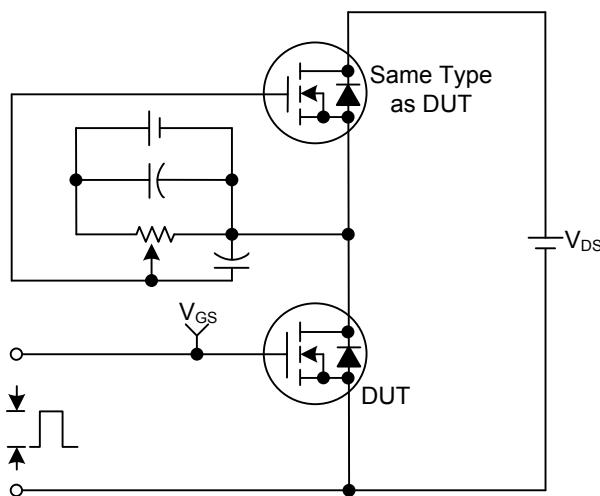


■ TEST CIRCUITS AND WAVEFORMS

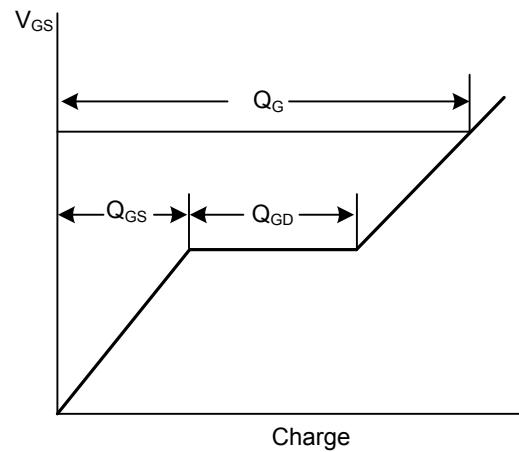


Peak Diode Recovery dv/dt Waveforms

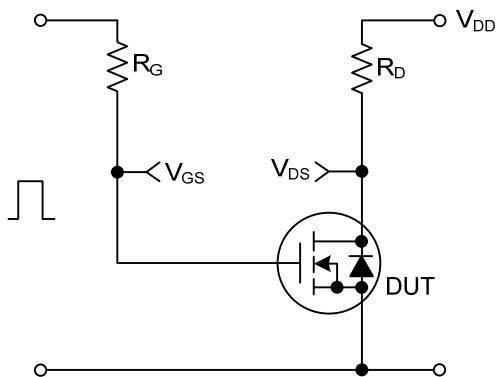
■ TEST CIRCUITS AND WAVEFORMS



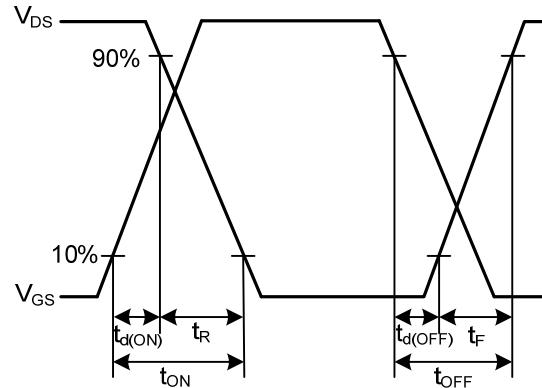
Gate Charge Test Circuit



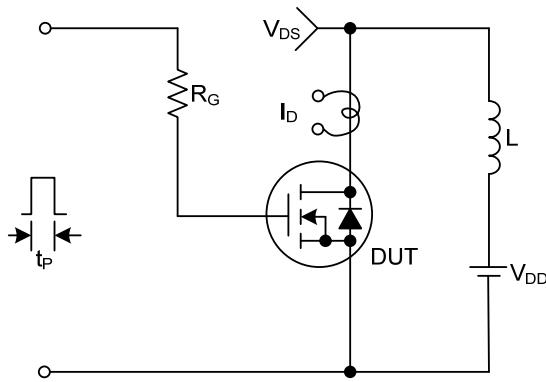
Gate Charge Waveforms



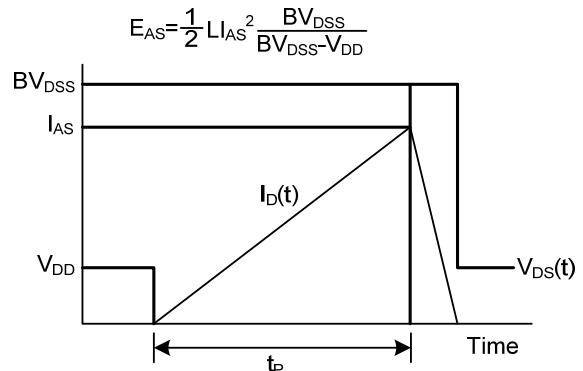
Resistive Switching Test Circuit



Resistive Switching Waveforms

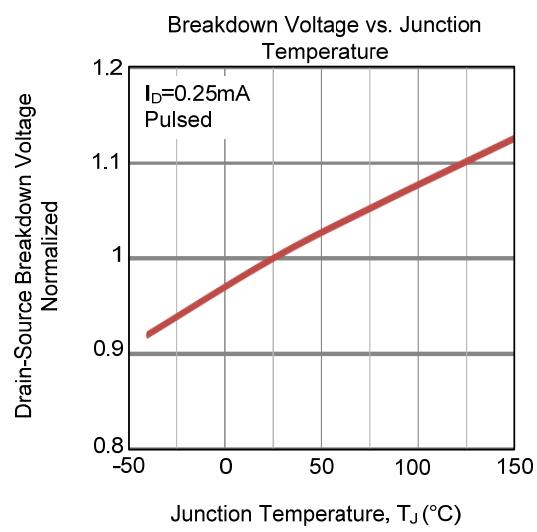
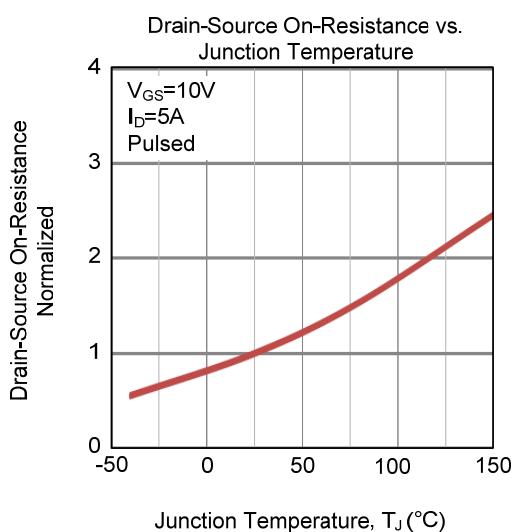
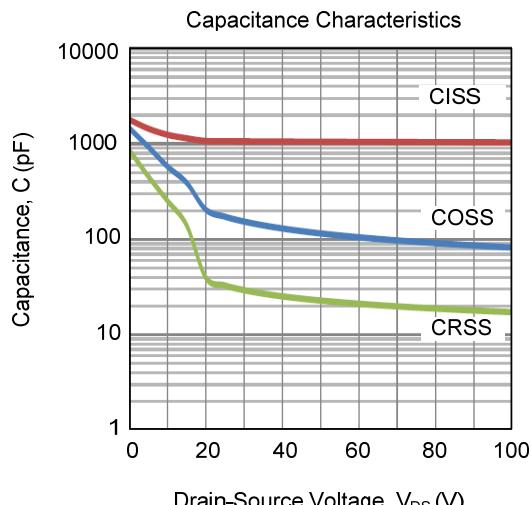
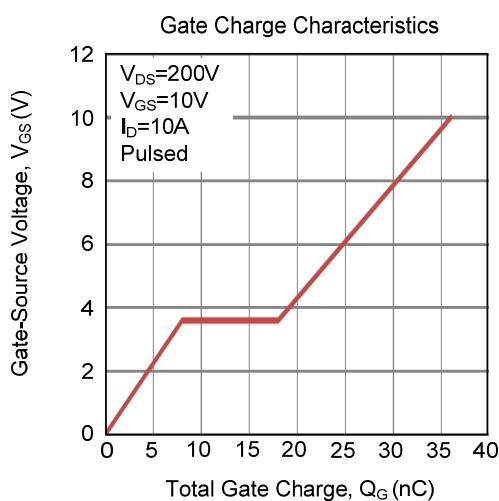
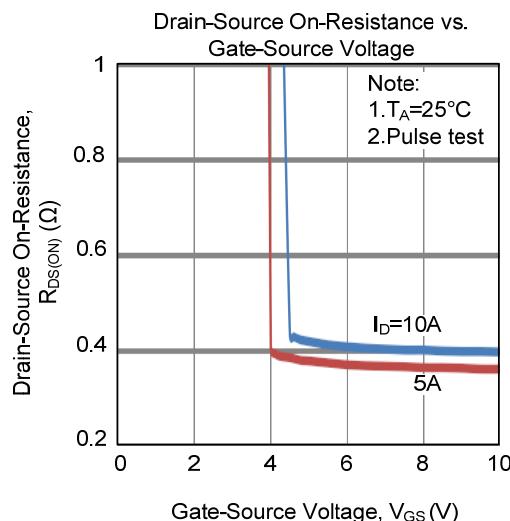
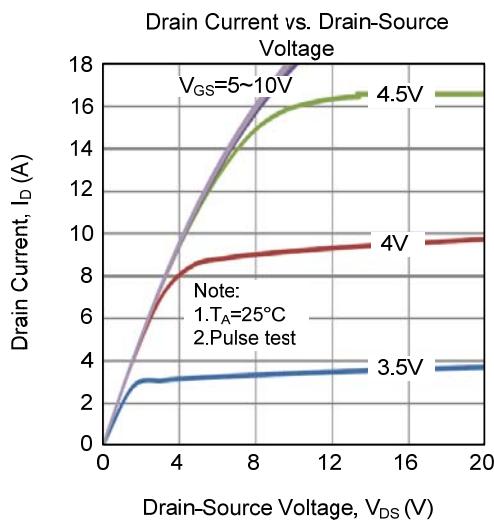


Unclamped Inductive Switching Test Circuit

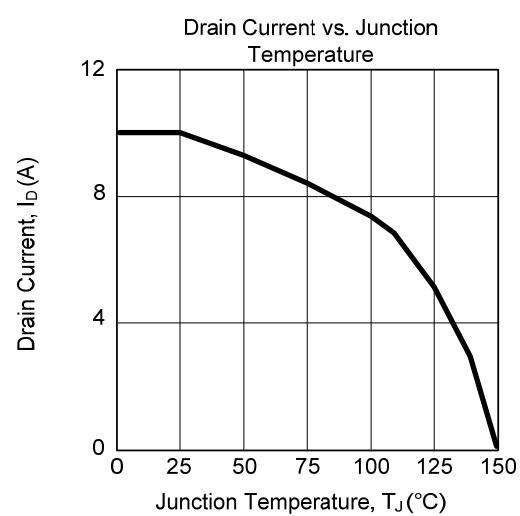
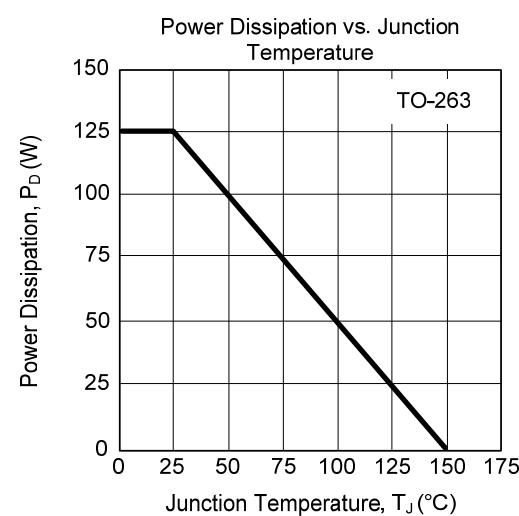
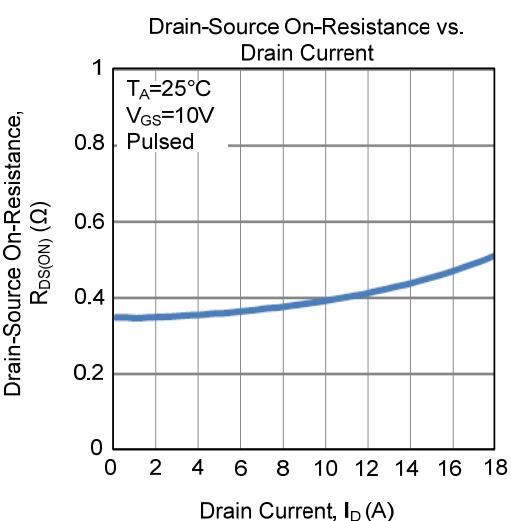
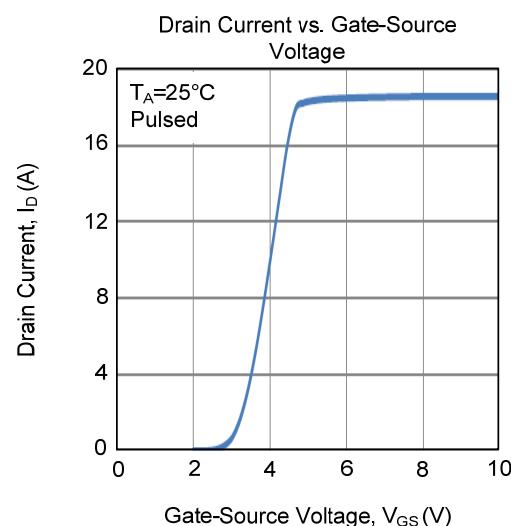
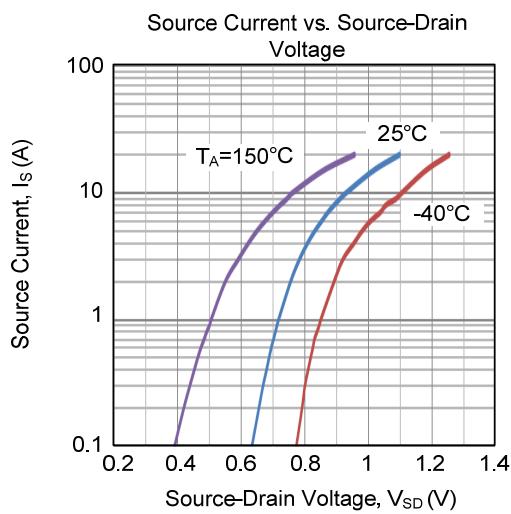
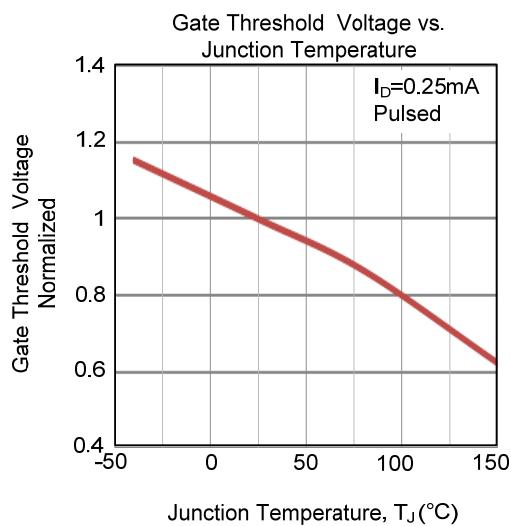


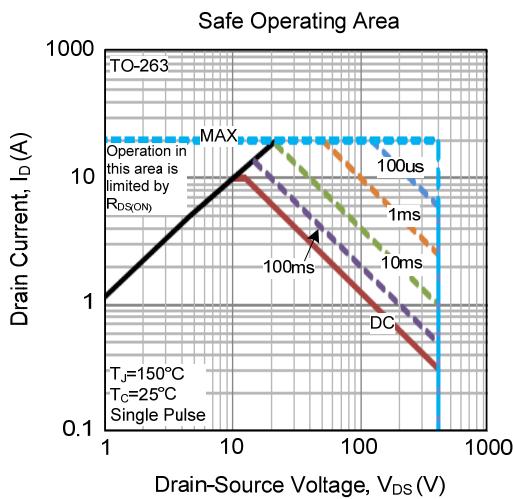
Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)

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