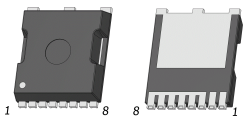
Silicon Carbide (SiC) Combo JFET – EliteSiC, Power N-Channel, H-PDSO-F8, 750 V, 5.4 mohm

UG4SC075005L8S



H-PDSO-F8
CASE 740AA

Description

onsemi's UG4SC075005L8S "Combo-FET" integrates both a 750 V SiC JFET and a Low Voltage Si MOSFET into a single H-PDSO-F8 package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

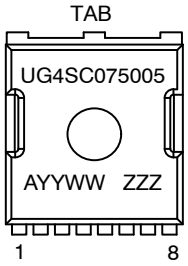
Features

- Single Digit $R_{DS(on)}$
- Normally-off Capability
- Improved Speed Control
- Improved Parallel Device Operation (3+ FETs)
- Operating Temperature: 175 °C (Max)
- High Pulse Current Capability
- Excellent Device Robustness
- Silver-Sintered Die Attach for Excellent Thermal Resistance
- Short Circuit Rated
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

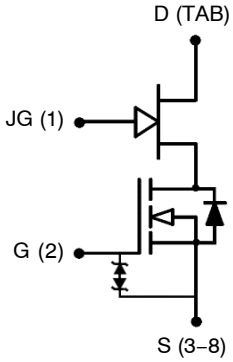
- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High Power Switch Mode Converters (>25 kW)

MARKING DIAGRAM



UG4SC075005	= Specific Device Number
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Value	Unit
V_{DS}	Drain-Source Voltage		750	V
V_{JGS}	JFET Gate (JG) to Source Voltage	DC	–30 to +3	V
		AC (Note 1)	–30 to +30	V
V_{GS}	MOSFET Gate (G) to Source Voltage	DC	–20 to + 20	V
		AC (f > 1 Hz)	–25 to + 25	V
I_D	Continuous Drain Current (Note 2)	T_C < 144 °C	120	A
I_{DM}	Pulsed Drain Current (Note 3)	T_C = 25 °C	588	A
E_{AS}	Single Pulsed Avalanche Energy (Note 4)	L = 15 mH, I_{AS} = 6.5 A	316	mJ
t_{SC}	Short Circuit Withstand Time	V_{DS} = 400 V, $T_{J(START)}$ = 175 °C	5	μS
dv/dt	SiC FET dv/dt Ruggedness	V_{DS} < 500 V	100	V/ns
P_{tot}	Power Dissipation	T_C = 25 °C	1153	W
$T_{J,max}$	Maximum Junction Temperature		175	°C
T_J, T_{STG}	Operating and Storage Temperature		–55 to 175	°C
T_{solder}	Reflow Soldering Temperature	Reflow MSL 1	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. +30 V AC rating applies for turn-on pulses < 200 ns applied with external R_G > 1 Ω.
2. Limited by Bondwires
3. Pulse width t_p limited by $T_{J,max}$.
4. Starting T_J = 25 °C

THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		–	0.10	0.13	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C and V_{JGS} = 0 V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE - STATIC						
BV_{DS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	750	–	–	V
I_{DSS}	Total Drain Leakage Current	V_{DS} = 750 V, V_{GS} = 0 V, T_J = 25 °C	–	6	130	μA
		V_{DS} = 750 V, V_{GS} = 0 V, T_J = 175 °C	–	45	–	
I_{JGSS}	Total JFET Gate Leakage Current	V_{GS} = –20 V, V_{GS} = 12 V	–	0.1	100	μA
I_{GSS}	Total MOSFET Gate Leakage Current	V_{GS} = –20 V / +20 V	–	6	20	μA
$R_{DS(on)}$	Drain-Source On-resistance	V_{GS} = 15 V, V_{JGS} = 2 V, I_D = 80 A, T_J = 25 °C	–	5.0	–	mΩ
		V_{GS} = 15 V, V_{JGS} = 0 V, I_D = 80 A, T_J = 25 °C	–	5.4	7.2	
		V_{GS} = 15 V, V_{JGS} = 0 V, I_D = 80 A, T_J = 125 °C	–	9.3	–	
		V_{GS} = 15 V, V_{JGS} = 0 V, I_D = 80 A, T_J = 175 °C	–	12.2	–	
$V_{JG(th)}$	JFET Gate Threshold Voltage	V_{DS} = 5 V, V_{GS} = 12 V, I_D = 180 mA	–8.3	–6.0	–3.7	V
$V_{G(th)}$	MOSFET Gate Threshold Voltage	V_{DS} = 5 V, I_D = 10 mA	4	4.7	6	V
R_{JG}	JFET Gate Resistance	f = 1 MHz, open drain	–	0.8	–	Ω
R_G	MOSFET Gate Resistance	f = 1 MHz, open drain	–	0.8	–	Ω

ELECTRICAL CHARACTERISTICS (T_J = +25 °C and V_{JGS} = 0 V unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE - REVERSE DIODE						
I_S	Diode Continuous Forward Current (Note 1)	T_C < 144 °C	–	–	120	A
$I_{S,pulse}$	Diode Pulse Current (Note 2)	T_C = 25 °C	–	–	588	A
V_{FSD}	Forward Voltage	V_{GS} = 0 V, I_S = 50 A, T_J = 25 °C	–	1.03	1.16	V
		V_{GS} = 0 V, I_S = 50 A, T_J = 175 °C	–	1.06	–	
Q_{rr}	Reverse Recovery Charge	V_{DS} = 400 V, I_S = 80 A, V_{GS} = 0 V, V_{JGS} = 0 V, R_{JG} = 0.7 Ω, di/dt = 2400 A/μs, T_J = 25 °C	–	377	–	nC
t_{rr}	Reverse Recovery Time		–	70	–	ns
Q_{rr}	Reverse Recovery Charge	V_{DS} = 400 V, I_S = 80 A, V_{GS} = 0 V, V_{JGS} = 0 V, R_{JG} = 0.7 Ω, di/dt = 2400 A/μs, T_J = 150 °C	–	427	–	nC
t_{rr}	Reverse Recovery Time		–	78	–	ns
TYPICAL PERFORMANCE - DYNAMIC WITH MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V						
C_{iss}	MOSFET Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 100 kHz	–	8374	–	pF
C_{oss}	Output Capacitance		–	362	–	
C_{rss}	Reverse Transfer Capacitance		–	4	–	
$C_{oss(er)}$	Effective Output Capacitance, Energy Related	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	475	–	pF
$C_{oss(tr)}$	Effective Output Capacitance, Time Related		–	950	–	pF
Q_G	Total Gate Charge	V_{DS} = 400 V, I_D = 80 A, V_{GS} = 0 V to 15 V	–	164	–	nC
Q_{GD}	Gate-Drain Charge		–	24	–	
Q_{GS}	Gate-Source Charge		–	46	–	
TYPICAL PERFORMANCE - DYNAMIC WITH JFET GATE AS CONTROL TERMINAL AND V_{GS} = +12 V						
C_{Jiss}	JFET Input Capacitance	V_{DS} = 400 V, V_{JGS} = −20 V, f = 100 kHz	–	3028	–	pF
C_{Joss}	JFET Output Capacitance		–	364	–	
C_{Jrss}	JFET Reverse Transfer Capacitance		–	360	–	
Q_{JG}	JFET Total Gate Charge	V_{DS} = 400 V, I_D = 80 A, V_{JGS} = −18 V to 0 V	–	400	–	nC
Q_{JGD}	JFET Gate-drain Charge		–	270	–	
Q_{JGS}	JFET Gate-source Charge		–	60	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS - MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V

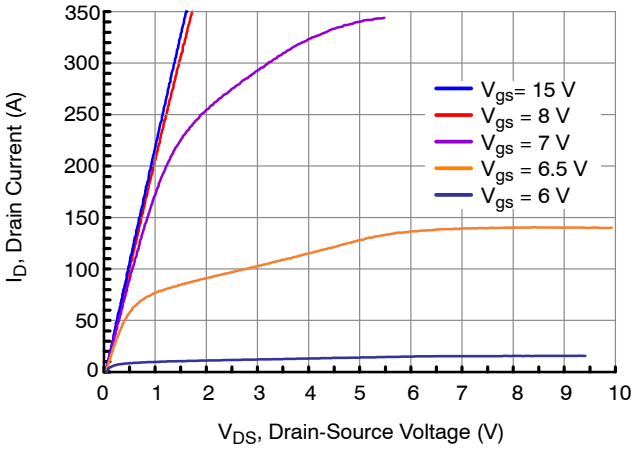


Figure 1. Typical Output Characteristics at T_J = −55 °C, t_p < 250 μs

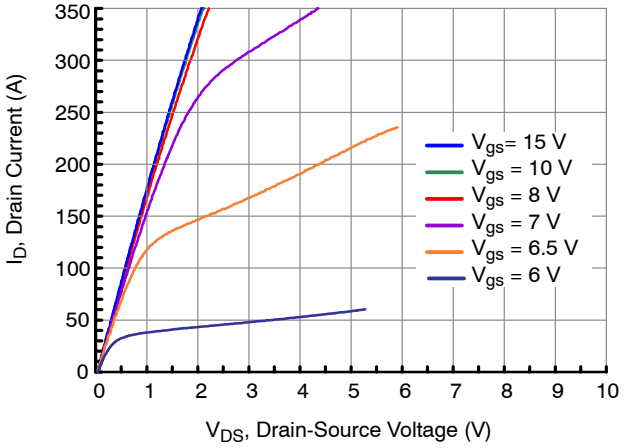


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

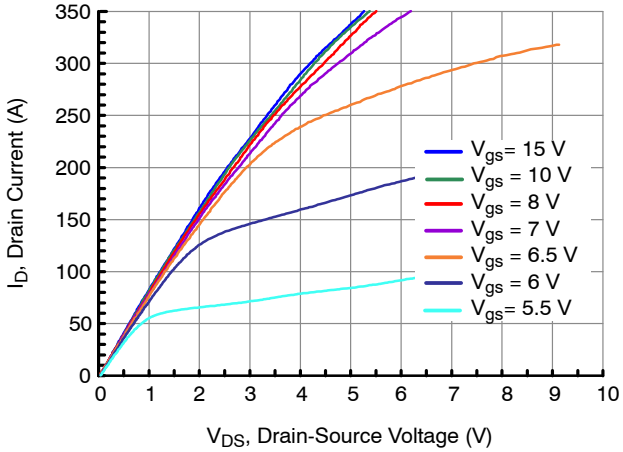


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

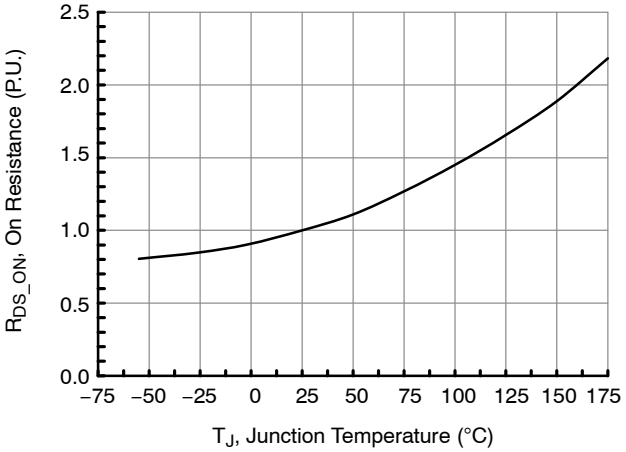


Figure 4. Normalized On-Resistance vs. Temperature at V_{GS} = 12 V and I_D = 80 A

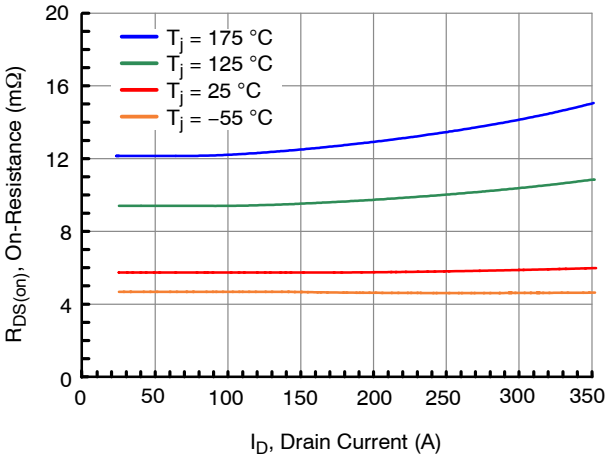


Figure 5. Typical Drain-Source On-Resistances at V_{GS} = 12 V

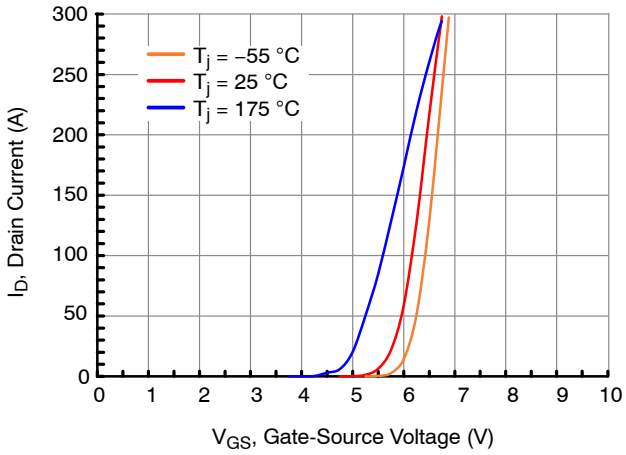


Figure 6. Typical Transfer Characteristics at V_{DS} = 5 V

TYPICAL PERFORMANCE DIAGRAMS - MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V

(continued)

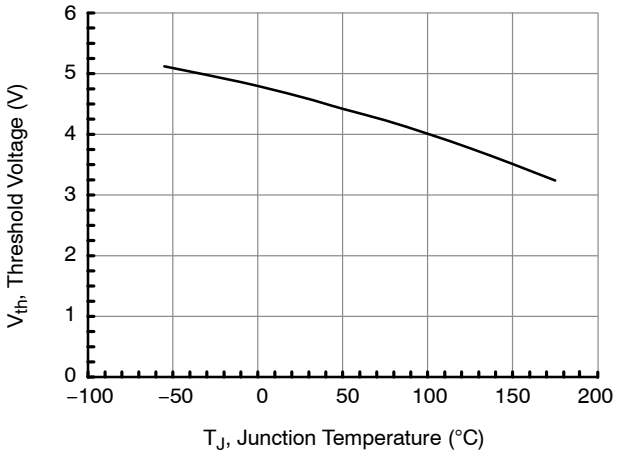


Figure 7. Threshold Voltage vs Junction Temperature at V_{DS} = 5 V and I_D = 10 mA

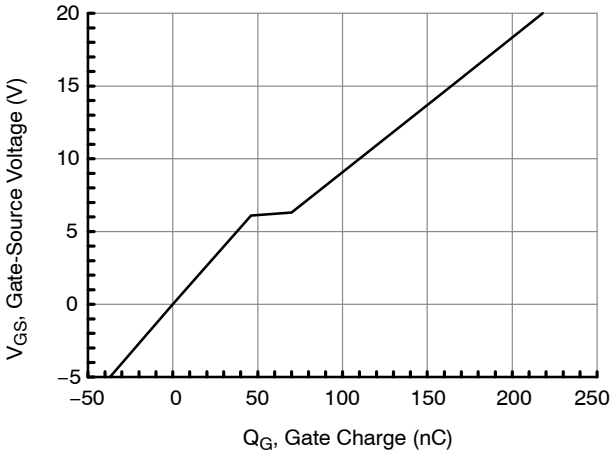


Figure 8. Typical Gate Charge at V_{DS} = 400 V and I_D = 80 A

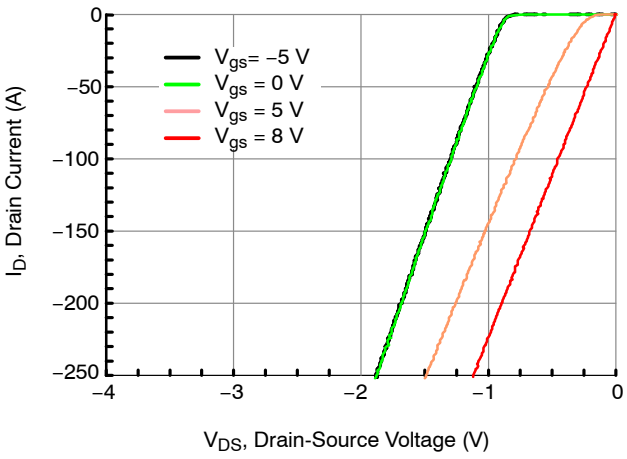


Figure 9. 3rd Quadrant Characteristics at T_J = −55 °C

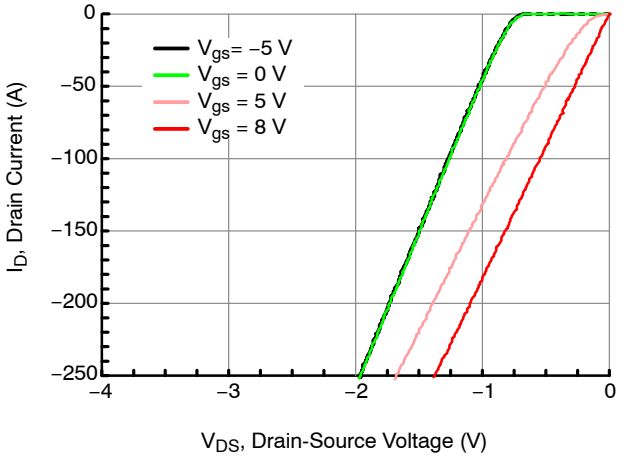


Figure 10. 3rd Quadrant Characteristics at T_J = 25 °C

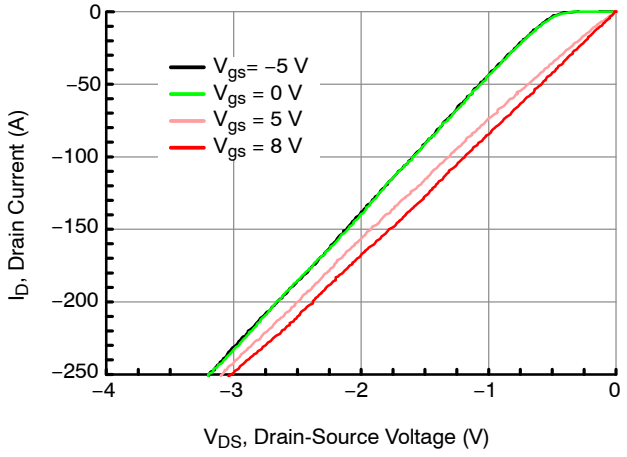


Figure 11. 3rd Quadrant Characteristics at T_J = 175 °C

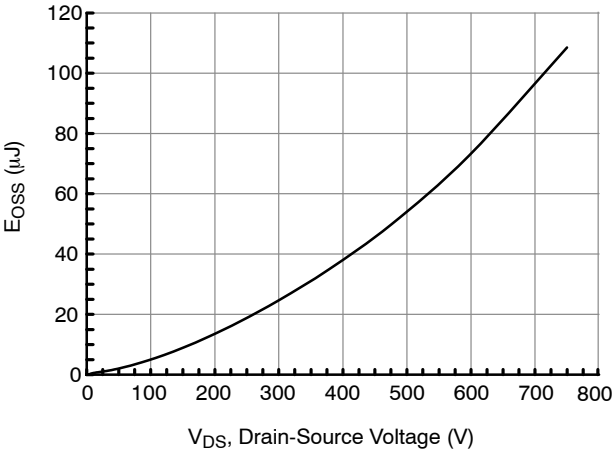


Figure 12. Typical Stored Energy in C_{OSS} at V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS - MOSFET GATE AS CONTROL TERMINAL AND V_{JGS} = 0 V

(continued)

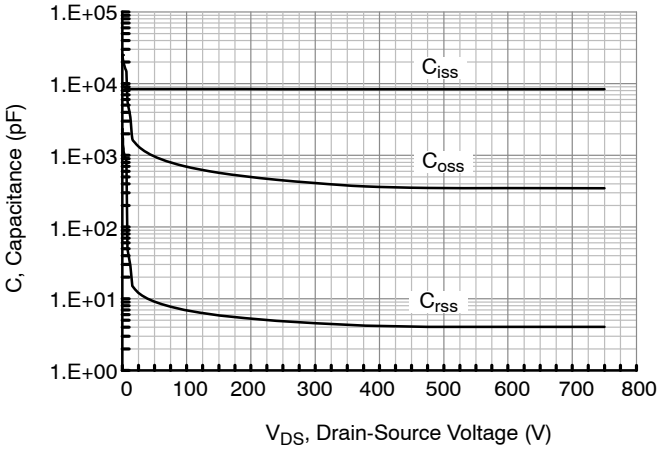


Figure 13. Typical Capacitances at f = 100 kHz and V_{GS} = 0 V

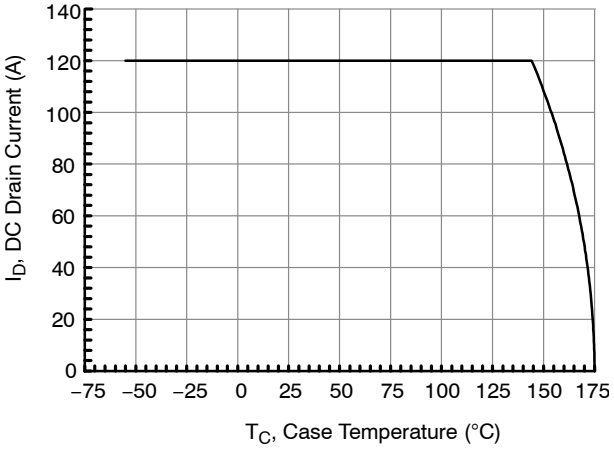


Figure 14. DC Drain Current Derating

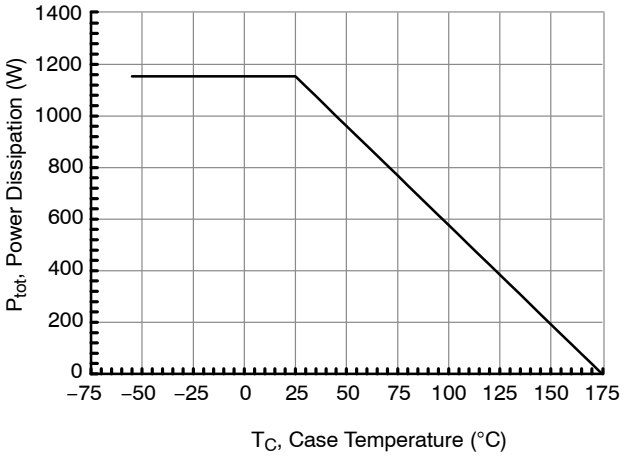


Figure 15. Total Power Dissipation

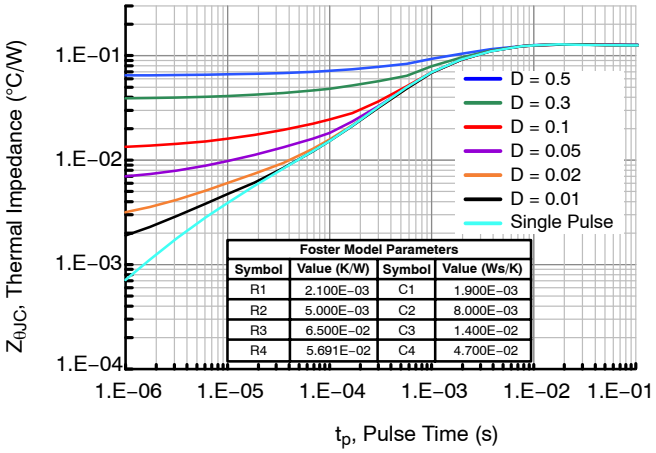


Figure 16. Maximum Transient Thermal Impedance

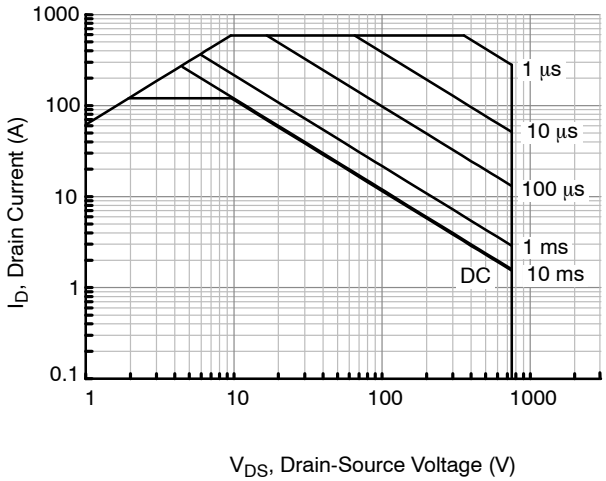


Figure 17. Safe Operation Area at T_C = 25 °C, D = 0, Parameter t_p

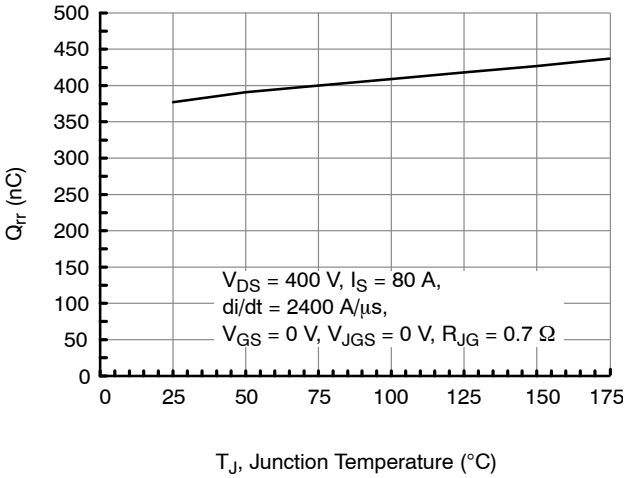


Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature

TYPICAL PERFORMANCE DIAGRAMS - JFET GATE AS CONTROL TERMINAL AND V_{GS} = +12 V

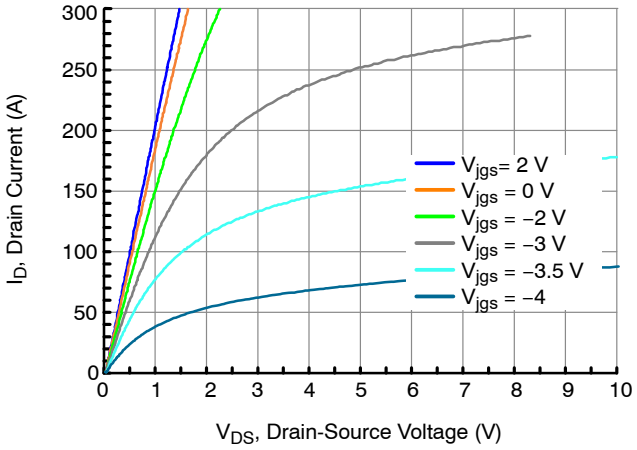


Figure 19. Typical Output Characteristics with JFET Gate as Control at T_J = −55 °C, t_p < 250 μs

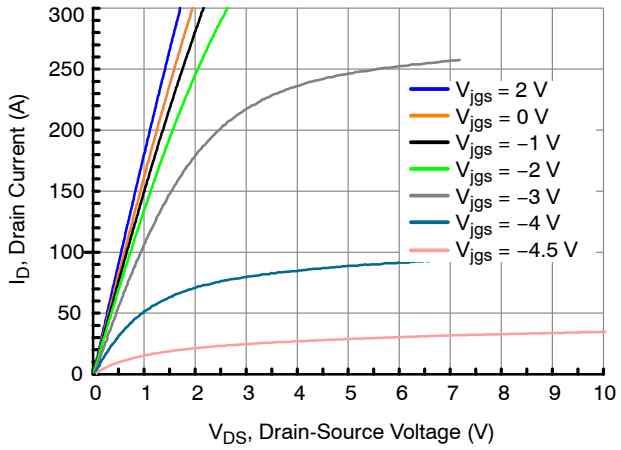


Figure 20. Typical Output Characteristics with JFET Gate as Control at T_J = 25 °C, t_p < 250 μs

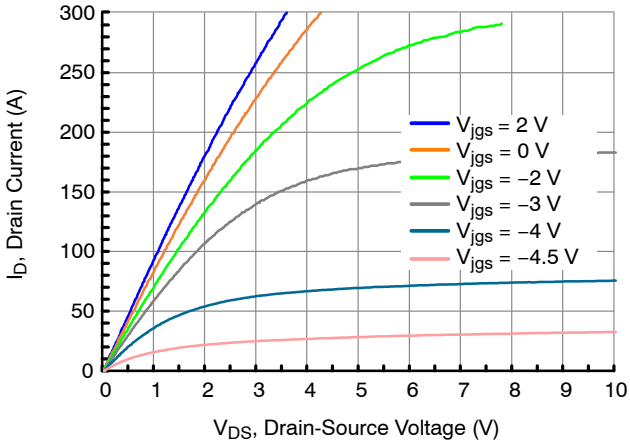


Figure 21. Typical Output Characteristics with JFET Gate as Control at T_J = 175 °C, t_p < 250 μs

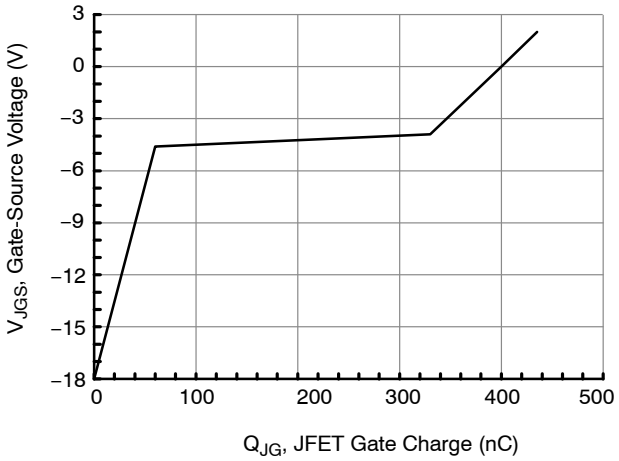


Figure 22. Typical JFET Gate Charge at V_{DS} = 400 V and I_D = 80 A

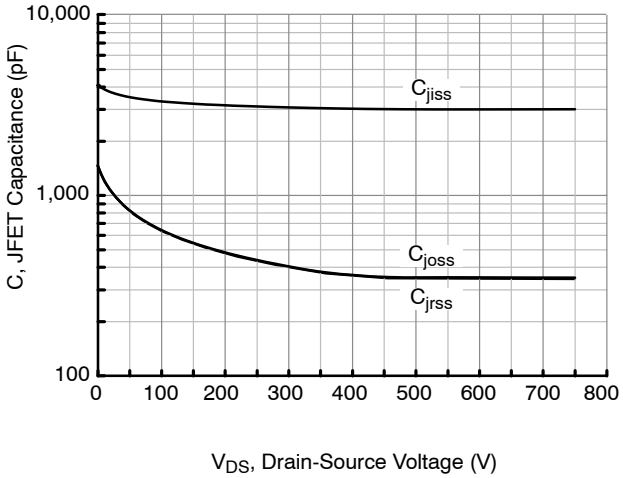


Figure 23. Typical JFET Capacitances at f = 100 kHz and V_{JGS} = −20 V

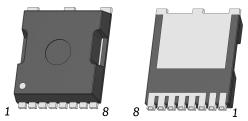
ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
UG4SC075005L8S	UG4SC075005	H-PDSO-F8 (Pb-Free, Halogen Free)	2,000 / Tape and Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

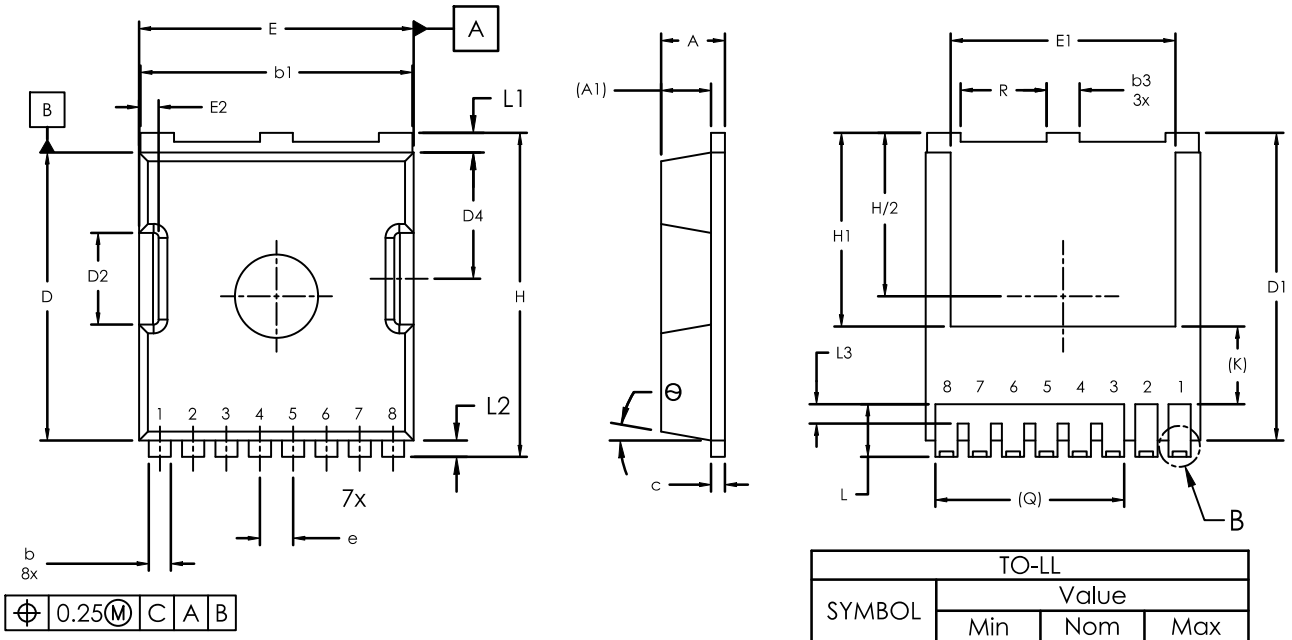
REVISION HISTORY

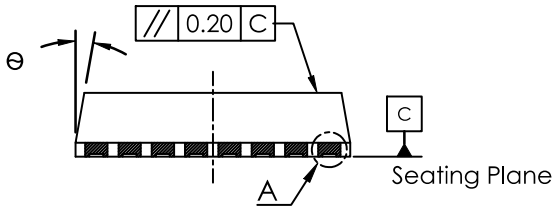
Revision	Description of Changes	Date
B	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with onsemi standards for SiC products.	1/15/2025
2	Converted the Data Sheet to **onsemi** format.	5/26/2025

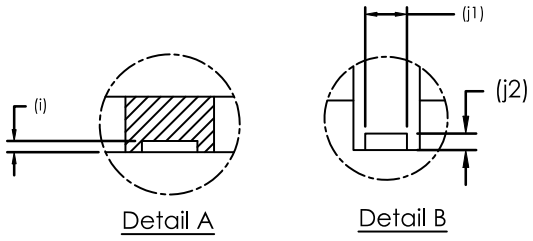


H−PDSO−F8 9.90x10.38x2.30, 1.20P
CASE 740AA
ISSUE B

DATE 24 JUN 2025







TO-LL			
SYMBOL	Value		
	Min	Nom	Max
A	2.15	2.30	2.45
A1		1.80 REF	
b	0.65	0.80	0.90
b1	9.65	9.80	9.95
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	10.88	11.08	11.28
D2	3.15	3.30	3.45
D4	4.40	4.55	4.70
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
E2	0.60	0.70	0.80
e		1.20 BSC	
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
i		0.10 REF	
j1		0.46 REF	
j2		0.20 REF	
K		2.80 REF	
L	1.40	1.90	2.10
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L3	0.30	0.70	0.80
Q		6.80 REF	
R	3.00	3.10	3.20
θ		10°	

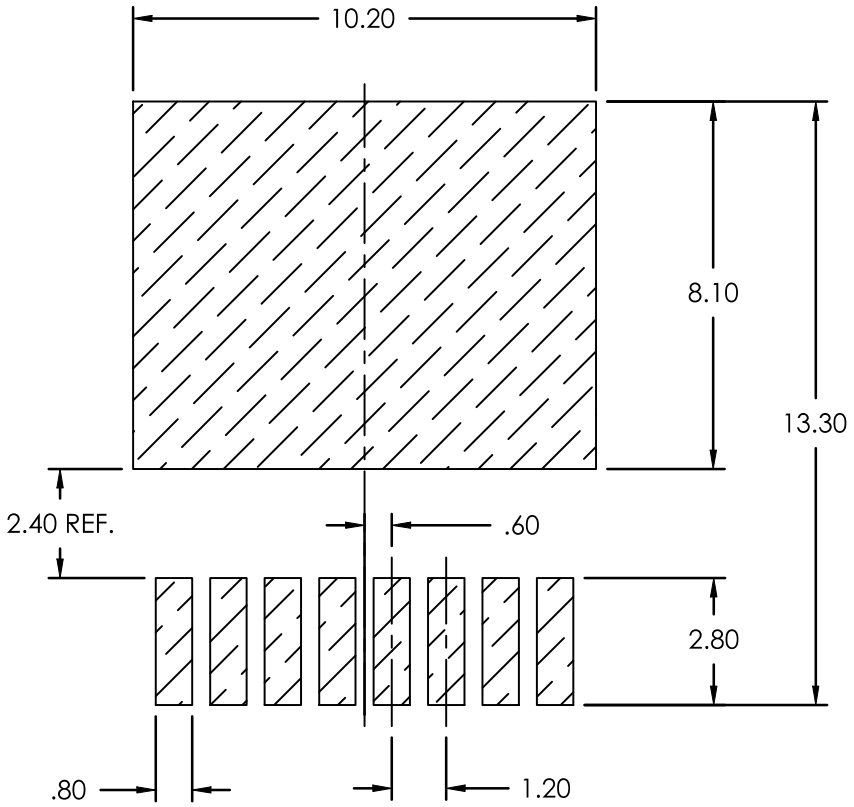
Note:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Dimensions does not include Burrs and Mold Flashes

DOCUMENT NUMBER:	**98AON26704H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**H−PDSO−F8 9.90x10.38x2.30, 1.20P**		**PAGE 1 OF 2**

H−PDSO−F8 9.90x10.38x2.30, 1.20P
CASE 740AA
ISSUE B

DATE 24 JUN 2025

RECOMMENDED PCB LAND PATTERN



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

ADDITIONAL INFORMATION

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