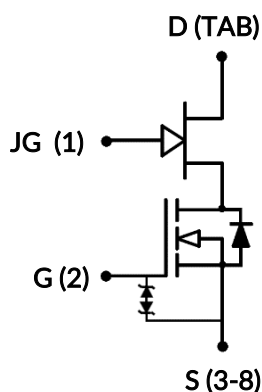
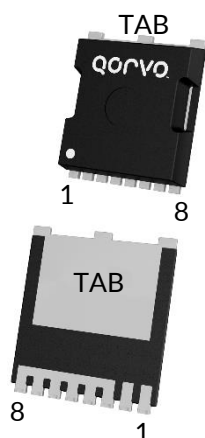


DATASHEET

UG4SC075005L8S



Part Number	Package	Marking
UG4SC075005L8S	MO-229	UG4SC075005



Silicon Carbide (SiC) Combo JFET - EliteSiC, Power N-Channel, TOLL, 750 V, 5 mohm

Preliminary, January 2025

Description

Qorvo's UG4SC075005L8S "Combo-FET" integrates both a 750V SiC JFET and a Low Voltage Si MOSFET into a single TOLL package. This innovative approach allows users to create circuitry that would enable a normally-off switch while leveraging the benefits of a normally-on SiC JFET. These benefits include ultra-low on-resistance ($R_{DS(on)}$) to minimize conduction losses and the exceptional robustness characteristic of a simplified JFET device structure, making it capable of handling the high-energy switching required in circuit protection applications. For switch-mode power conversion application, this device provides separate access to the JFET and MOSFET gates for improved speed control and ease of paralleling multiple devices.

Features

- Single digit $R_{DS(on)}$
- Normally-off capability
- Improved speed control
- Improved parallel device operation (3+ FETs)
- Operating temperature: 175°C (max)
- High pulse current capability
- Excellent device robustness
- Silver-sintered die attach for excellent thermal resistance
- Short circuit rated

Typical applications

- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control
- High power switch mode converters (>25kW)

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
JFET Gate (JG) to source voltage	V_{JGS}	DC	-30 to +3	V
		AC ¹	-30 to +30	V
MOSFET Gate (G) to source voltage	V_{GS}	DC	-20 to +20	V
		AC ($f > 1\text{Hz}$)	-25 to +25	V
Continuous drain current ²	I_D	$T_C < 144^\circ\text{C}$	120	A
Pulsed drain current ³	I_{DM}	$T_C = 25^\circ\text{C}$	588	A
Single pulsed avalanche energy ⁴	E_{AS}	$L=15\text{mH}$, $I_{AS} = 6.5\text{A}$	316	mJ
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	1153	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Reflow soldering temperature	T_{solder}	reflow MSL 1	260	$^\circ\text{C}$

1. +30V AC rating applies for turn-on pulses <200ns applied with external $R_G > 1\Omega$.

2. Limited by bondwires

3. Pulse width t_p limited by $T_{J,max}$

4. Starting $T_J = 25^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.10	0.13	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ and $V_{GS} = 0\text{V}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$	750			V
Total drain leakage current	I_{DSS}	$V_{DS}=750\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$		6	130	μA
		$V_{DS}=750\text{V}$, $V_{GS}=0\text{V}$, $T_J=175^\circ\text{C}$		45		
Total JFET gate leakage current	I_{JGSS}	$V_{GS}=-20\text{V}$, $V_{GS}=12\text{V}$		0.1	100	μA
Total MOSFET gate leakage current	I_{GSS}	$V_{GS}=-20\text{V} / +20\text{V}$		6	20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=15\text{V}$, $V_{JGS}=2\text{V}$, $I_D=80\text{A}$, $T_J=25^\circ\text{C}$		5.0		$\text{m}\Omega$
		$V_{GS}=15\text{V}$, $V_{JGS}=0\text{V}$, $I_D=80\text{A}$, $T_J=25^\circ\text{C}$		5.4	7.2	
		$V_{GS}=15\text{V}$, $V_{JGS}=0\text{V}$, $I_D=80\text{A}$, $T_J=125^\circ\text{C}$		9.3		
		$V_{GS}=15\text{V}$, $V_{JGS}=0\text{V}$, $I_D=80\text{A}$, $T_J=175^\circ\text{C}$		12.2		
JFET gate threshold voltage	$V_{JG(th)}$	$V_{DS}=5\text{V}$, $V_{GS}=12\text{V}$, $I_D=180\text{mA}$	-8.3	-6.0	-3.7	V
MOSFET gate threshold voltage	$V_{G(th)}$	$V_{DS}=5\text{V}$, $I_D=10\text{mA}$	4	4.7	6	V
JFET gate resistance	R_{JG}	$f=1\text{MHz}$, open drain		0.8		Ω
MOSFET gate resistance	R_G	$f=1\text{MHz}$, open drain		0.8		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C < 144^\circ\text{C}$			120	A
Diode pulse current ²	$I_{S,pulse}$	$T_C = 25^\circ\text{C}$			588	A
Forward voltage	V_{FSD}	$V_{GS}=0\text{V}$, $I_S=50\text{A}$, $T_J=25^\circ\text{C}$		1.03	1.16	V
		$V_{GS}=0\text{V}$, $I_S=50\text{A}$, $T_J=175^\circ\text{C}$		1.06		
Reverse recovery charge	Q_{rr}	$V_{DS}=400\text{V}$, $I_S=80\text{A}$, $V_{GS}=0\text{V}$, $V_{JGS}=0\text{V}$, $R_{JG}=0.7\Omega$, $di/dt=2400\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$		377		nC
Reverse recovery time	t_{rr}			70		ns
Reverse recovery charge	Q_{rr}	$V_{DS}=400\text{V}$, $I_S=80\text{A}$, $V_{GS}=0\text{V}$, $V_{JGS}=0\text{V}$, $R_{JG}=0.7\Omega$, $di/dt=2400\text{A}/\mu\text{s}$, $T_J=150^\circ\text{C}$		427		nC
Reverse recovery time	t_{rr}			78		ns

Typical Performance - Dynamic with MOSFET gate as control terminal and $V_{GS}=0V$

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
MOSFET input capacitance	C_{iss}	$V_{DS}=400V, V_{GS}=0V,$ $f=100kHz$		8374		pF
Output capacitance	C_{oss}			362		
Reverse transfer capacitance	C_{rss}			4		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V \text{ to } 400V,$ $V_{GS}=0V$		475		pF
Effective output capacitance, time related	$C_{oss(tr)}$			950		pF
Total Gate charge	Q_G	$V_{DS}=400V, I_D=80A,$ $V_{GS} = 0V \text{ to } 15V$		164		nC
Gate-drain charge	Q_{GD}			24		
Gate-source charge	Q_{GS}			46		

Typical Performance - Dynamic with JFET gate as control terminal and $V_{GS}=+12V$

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
JFET input capacitance	C_{Jiss}	$V_{DS}=400V, V_{JGS}=-20V,$ $f=100kHz$		3028		pF
JFET output capacitance	C_{Joss}			364		
JFET reverse transfer capacitance	C_{Jrss}			360		
JFET total gate charge	Q_{JG}	$V_{DS}=400V, I_D=80A,$ $V_{JGS} = -18V \text{ to } 0V$		400		nC
JFET gate-drain charge	Q_{JGD}			270		
JFET gate-source charge	Q_{JGS}			60		

Typical Performance Diagrams - MOSFET gate as control terminal and $V_{GS}=0V$

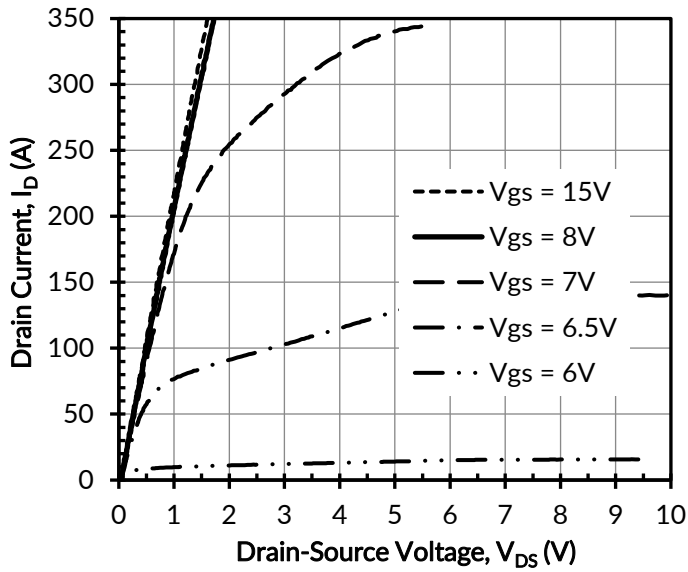


Figure 1. Typical output characteristics at $T_J = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

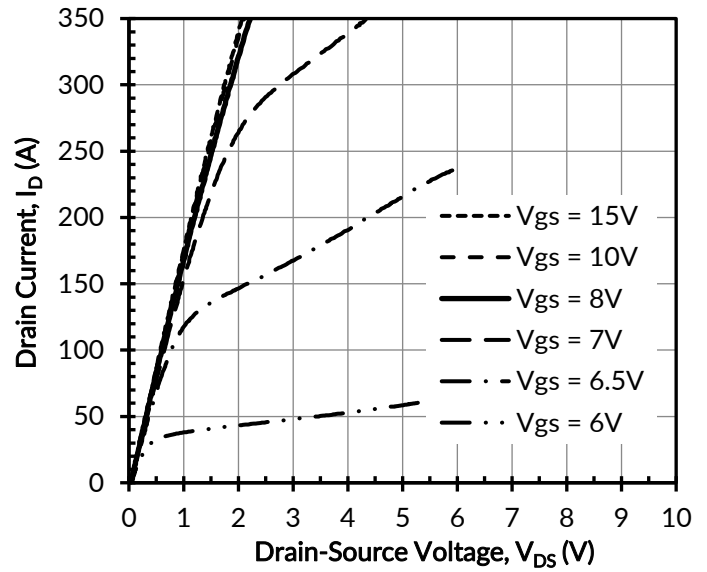


Figure 2. Typical output characteristics at $T_J = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

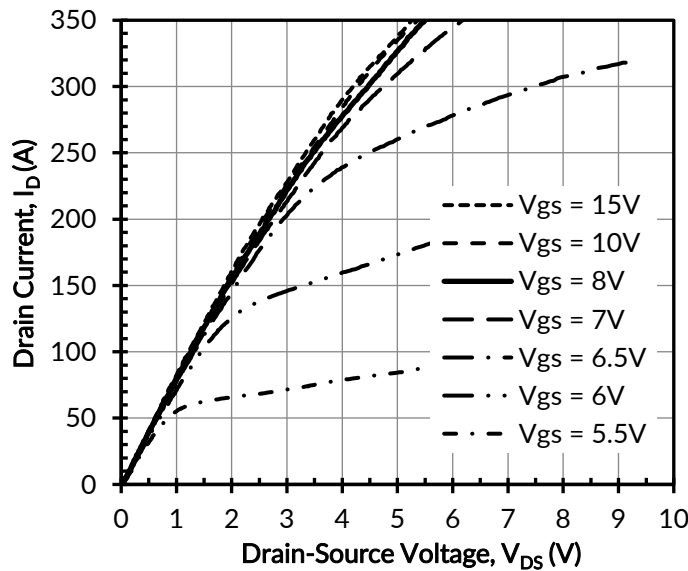


Figure 3. Typical output characteristics at $T_J = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

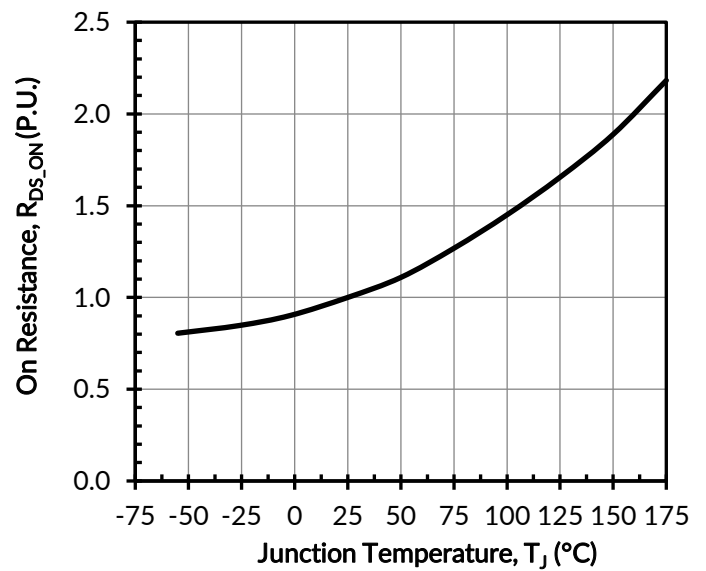


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12V$ and $I_D = 80A$

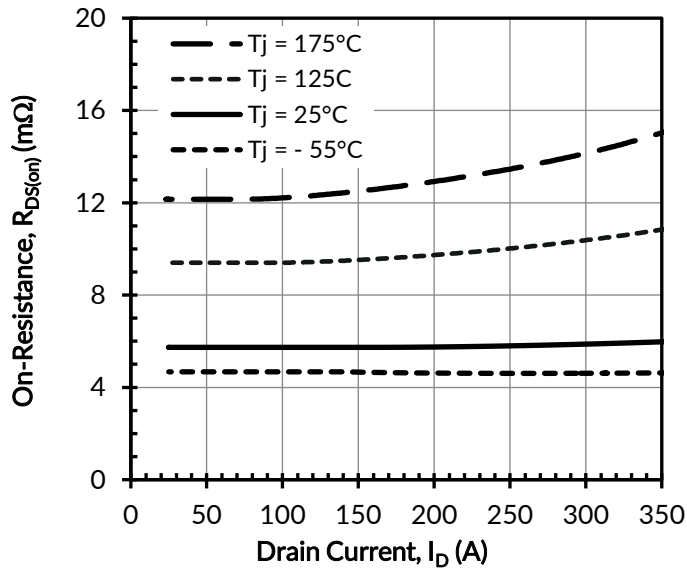


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

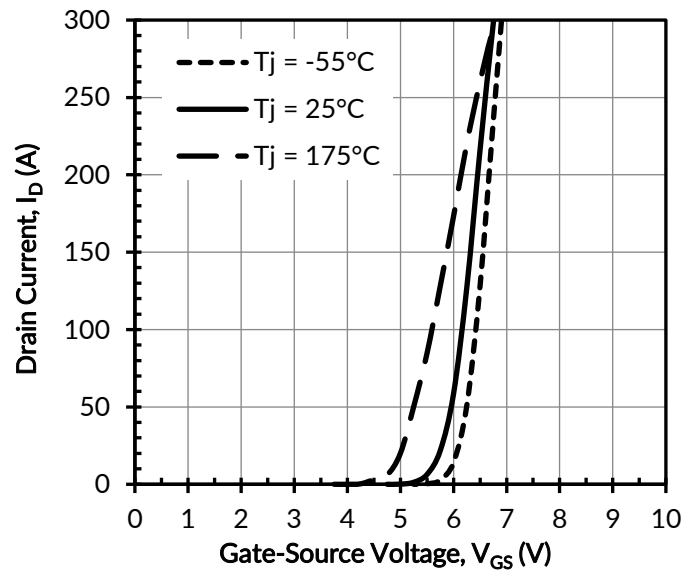


Figure 6. Typical transfer characteristics at $V_{DS} = 5V$

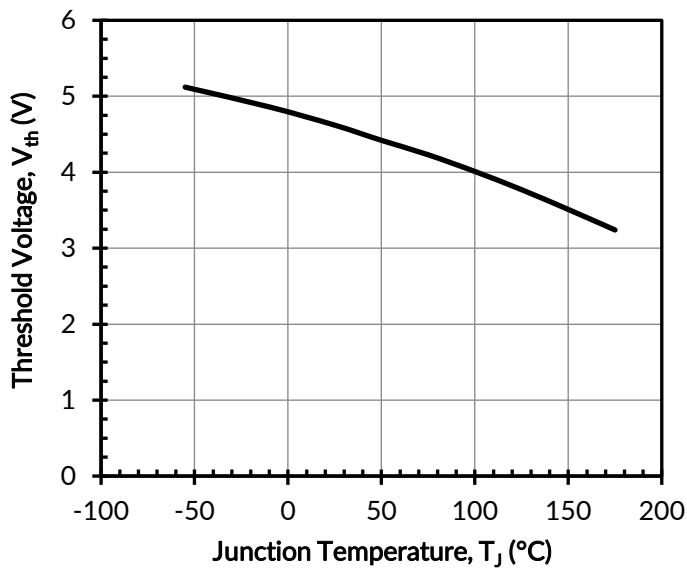


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 10mA$

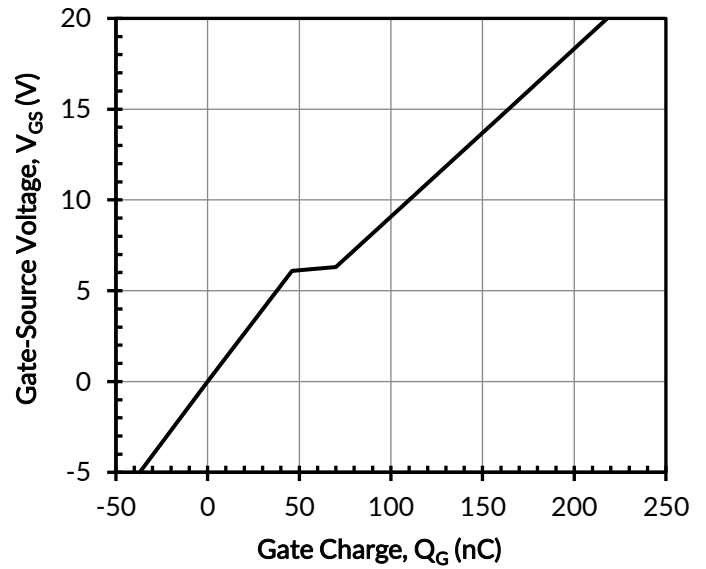


Figure 8. Typical gate charge at $V_{DS} = 400V$ and $I_D = 80A$

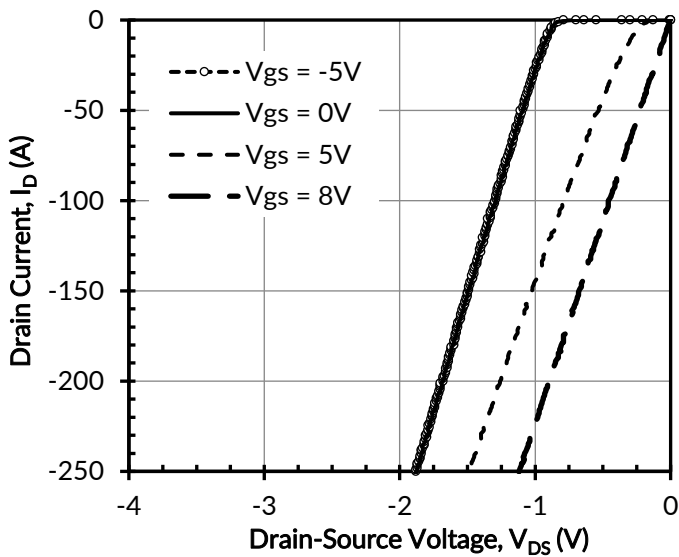


Figure 9. 3rd quadrant characteristics at $T_j = -55^\circ\text{C}$

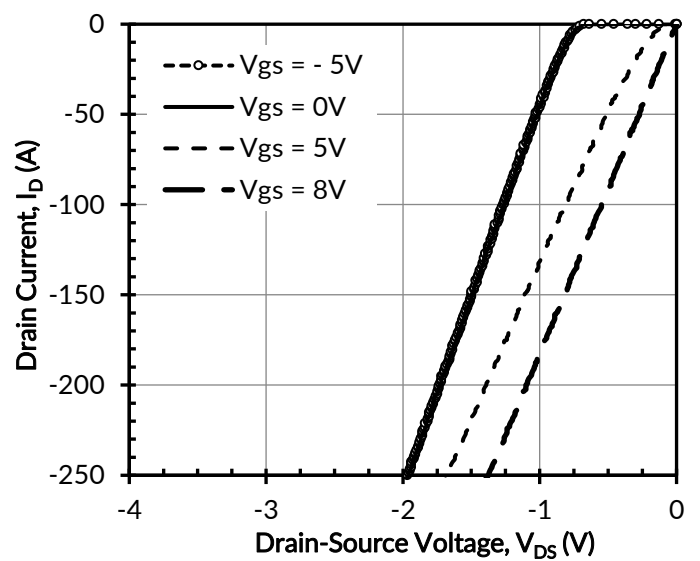


Figure 10. 3rd quadrant characteristics at $T_j = 25^\circ\text{C}$

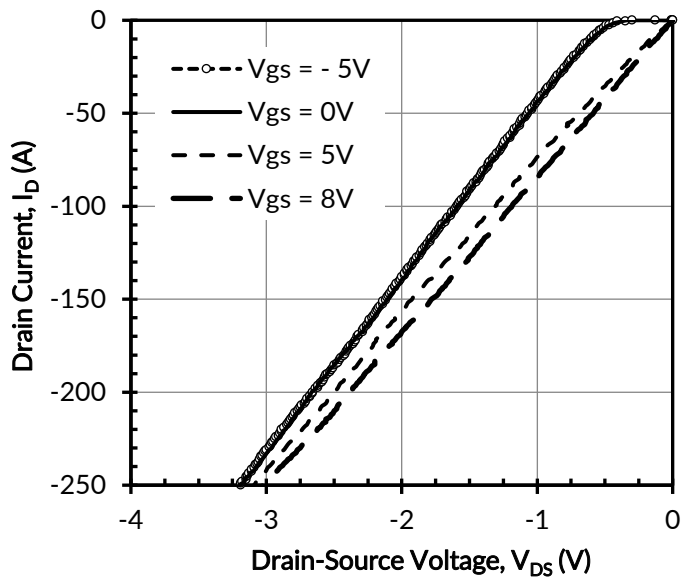


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

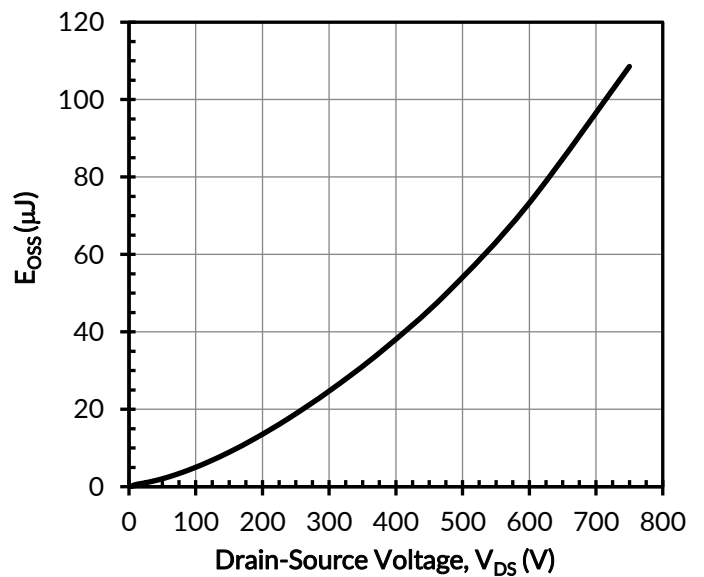


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

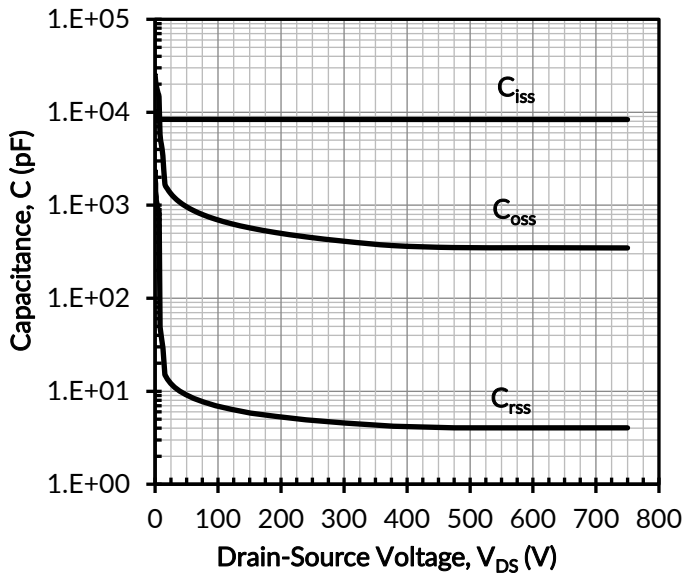


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

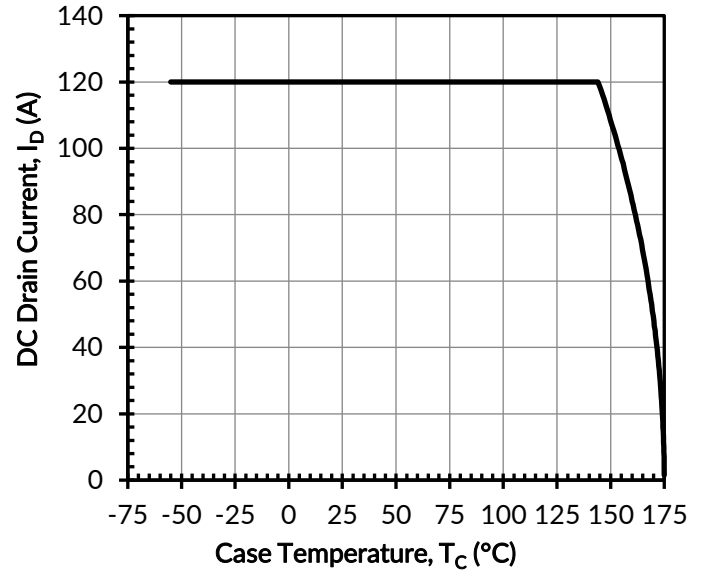


Figure 14. DC drain current derating

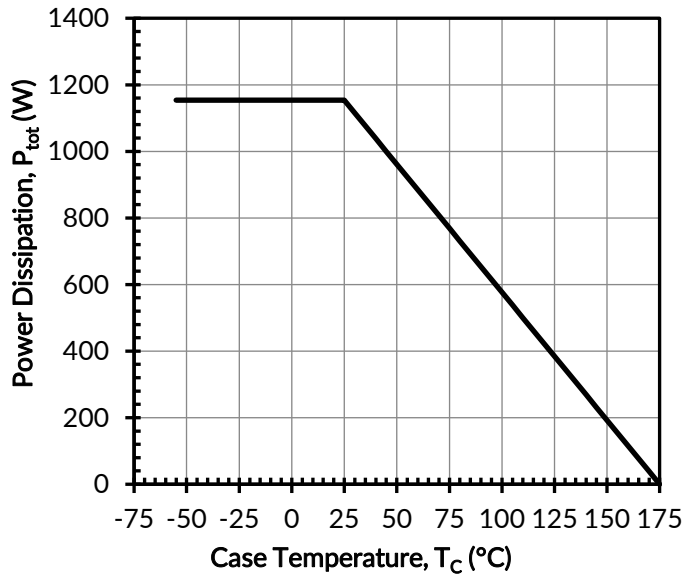


Figure 15. Total power dissipation

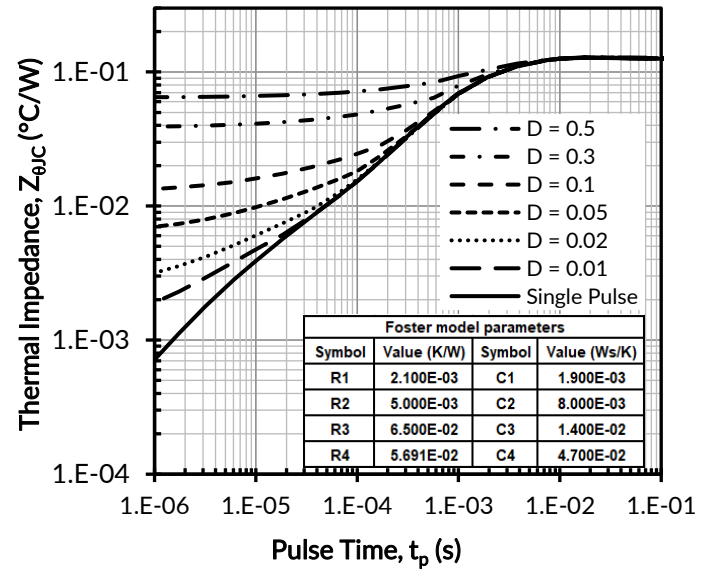


Figure 16. Maximum transient thermal impedance

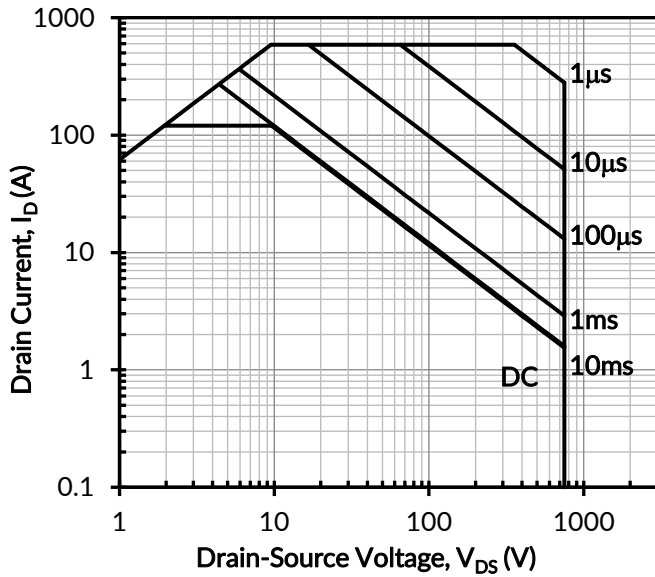


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

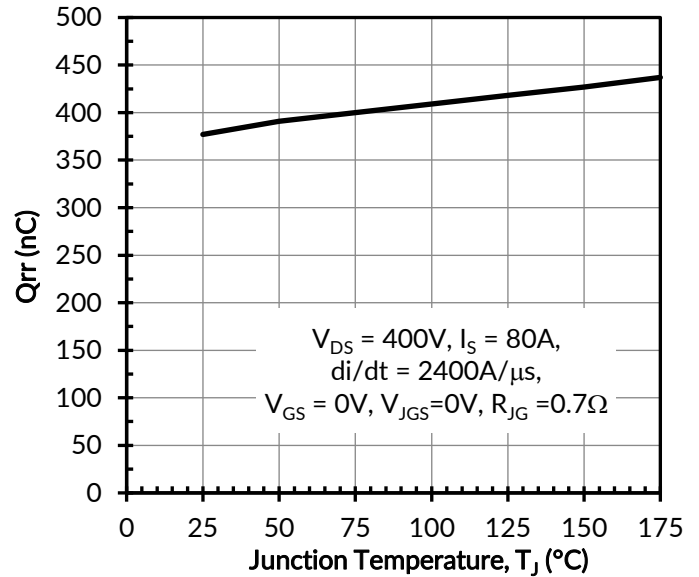


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature

Typical Performance Diagrams - JFET gate as control terminal and $V_{GS}=+12\text{V}$

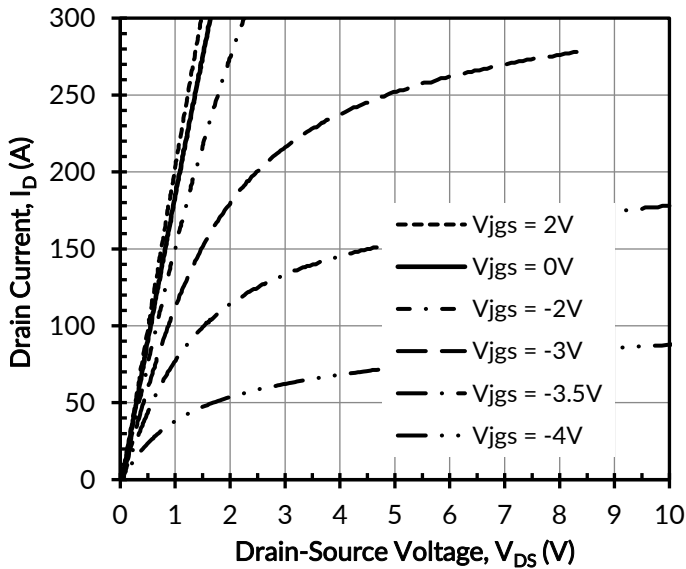


Figure 19. Typical output characteristics with JFET gate as control at $T_J = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

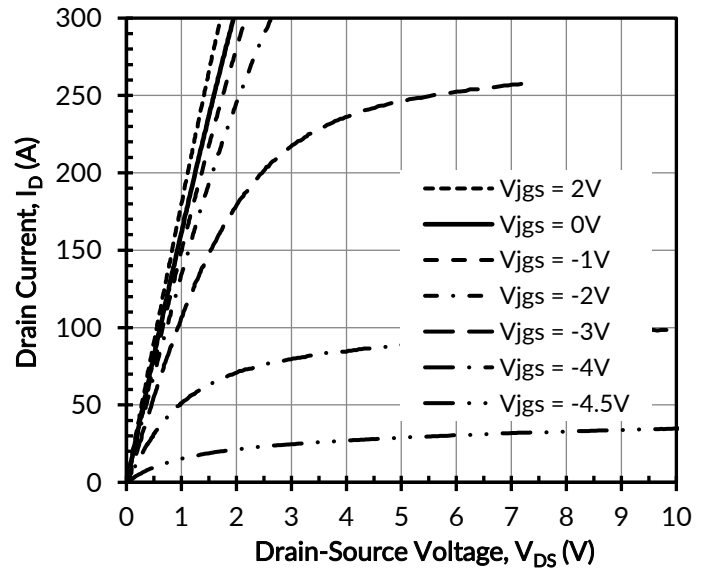


Figure 20. Typical output characteristics with JFET gate as control at $T_J = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

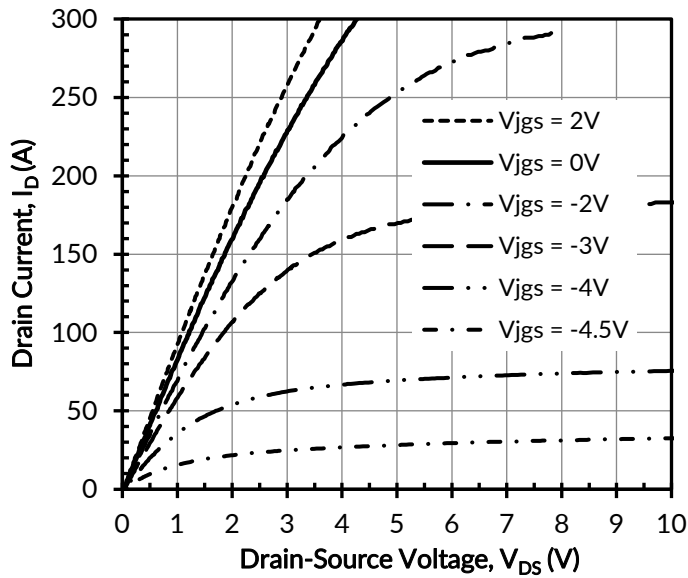


Figure 21. Typical output characteristics with JFET gate as control at $T_J = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

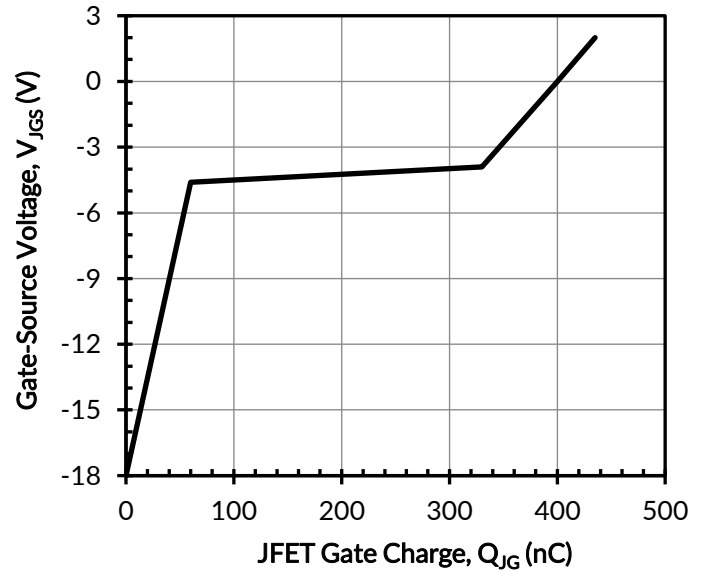


Figure 22. Typical JFET gate charge at $V_{DS} = 400\text{V}$ and $I_D = 80\text{A}$

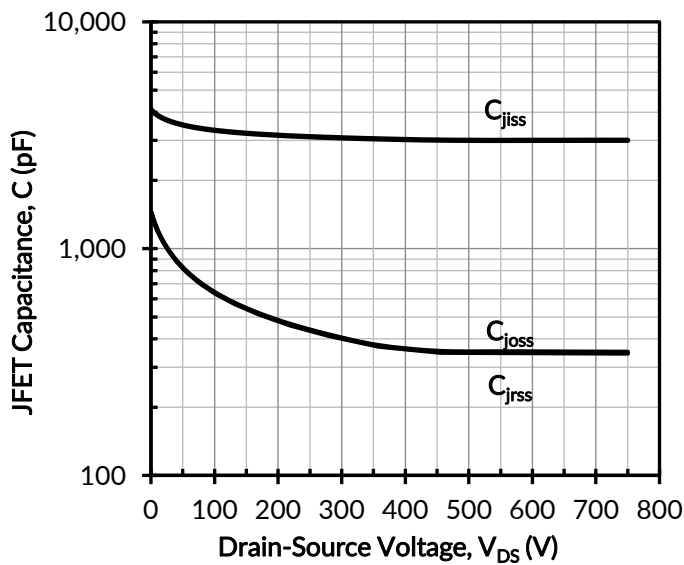
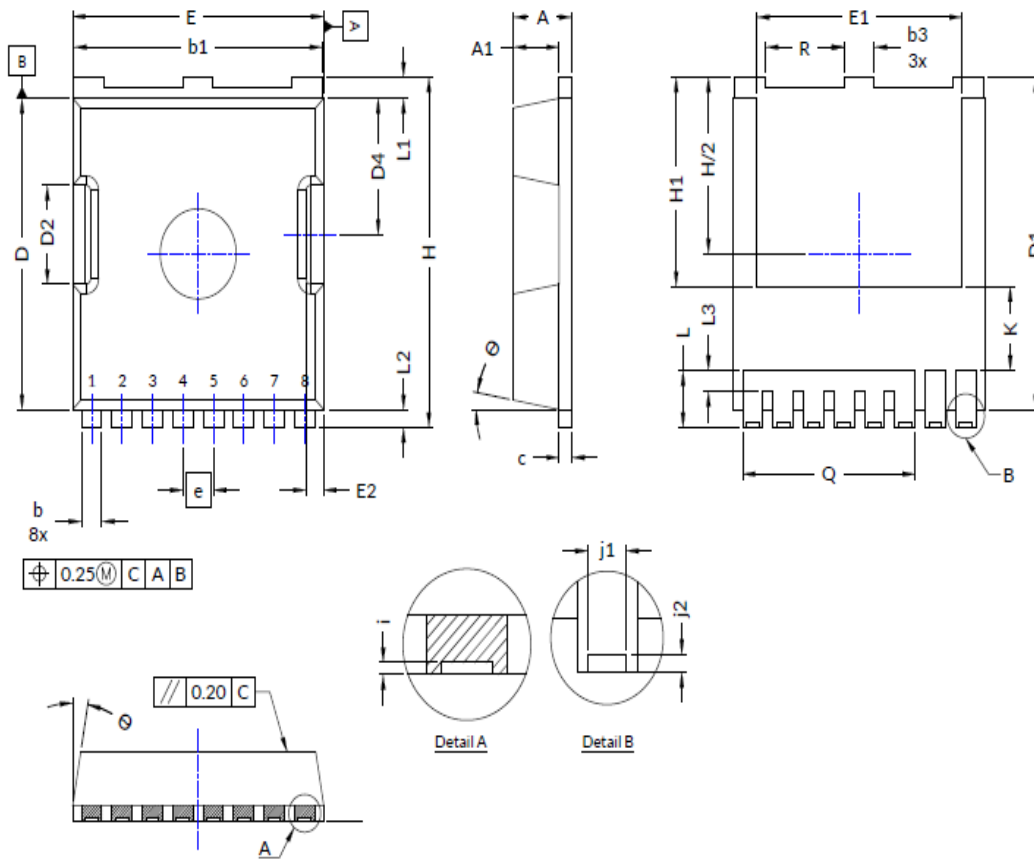


Figure 23. Typical JFET capacitances at $f = 100\text{kHz}$ and $V_{JGS} = -20\text{V}$

Package Outlines



Note:

1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes
3. Dimensions in compliance with JEDEC MO-299B except for backside heatsink exposed pad dimension, E1 and H1

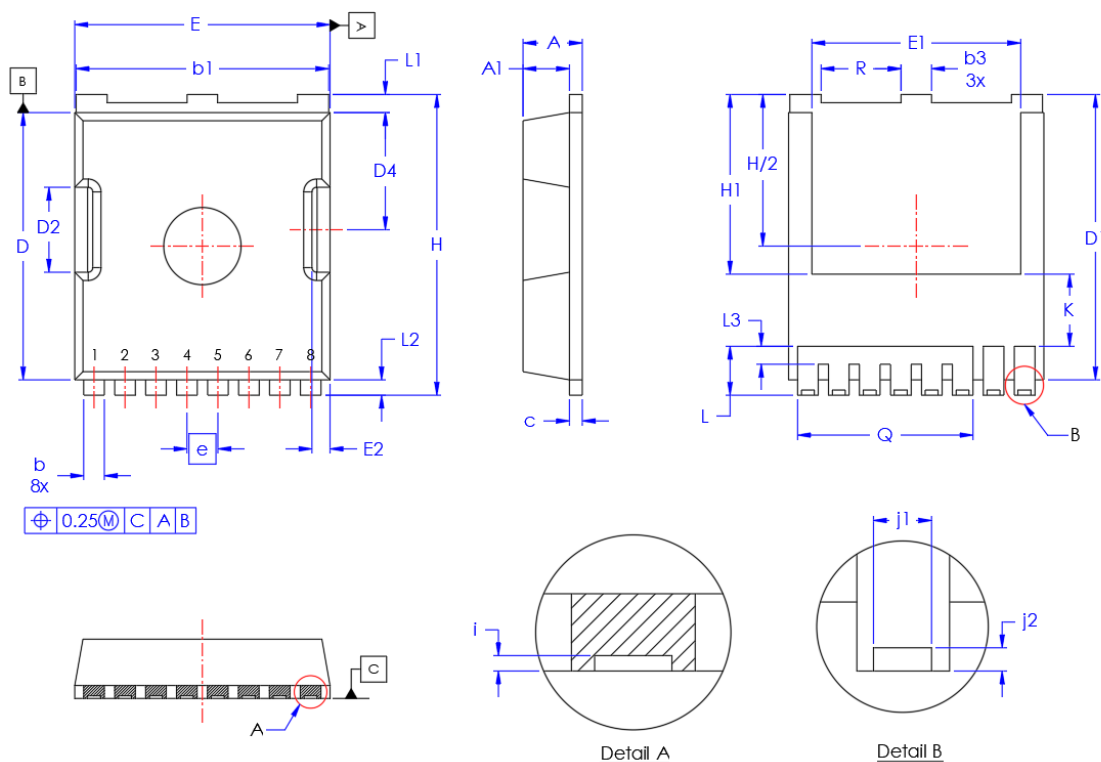
Pin Designations:

- 1: Gate
2: Source Kelvin
3-8: Source

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PACKAGE OUTLINE

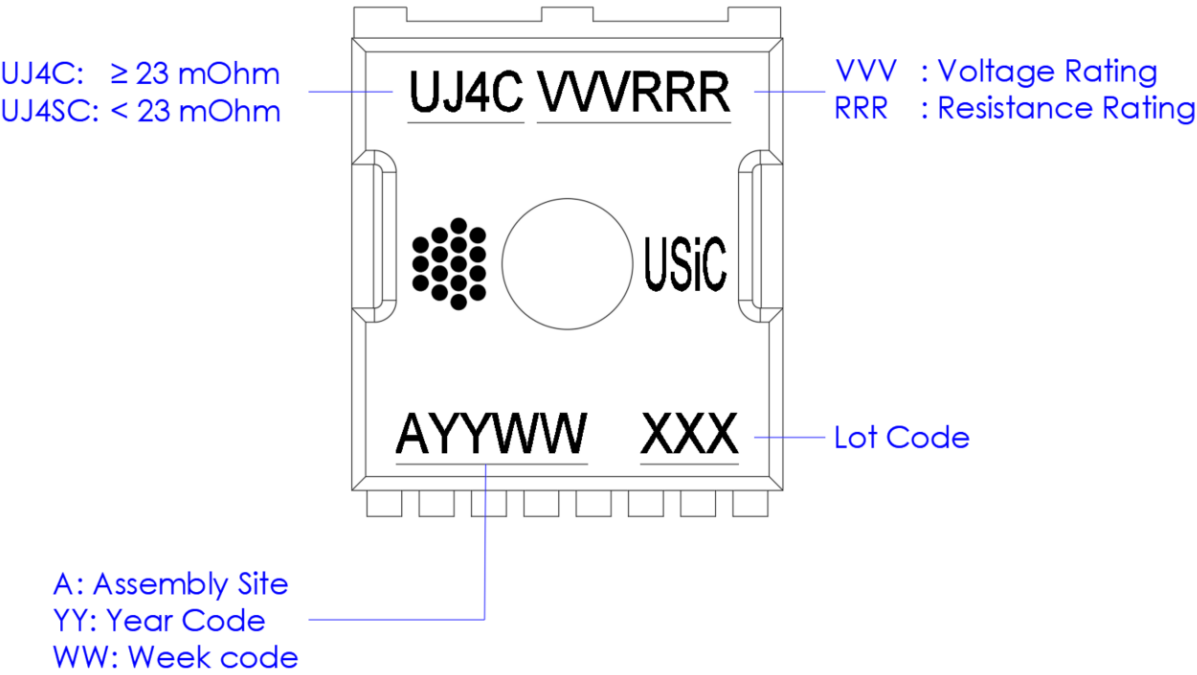


SYMBOL	TO-LL	
	Value	
A	Min	Max
A	2.15	2.45
A1	1.80 REF	
b	0.65	0.90
b1	9.65	9.95
b3	1.10	1.30
c	0.40	0.60
D	10.18	10.58
D1	10.88	11.28
D2	3.15	3.45
D4	4.40	4.70
E	9.70	10.10
E1	7.95	8.25
E2	0.60	0.80
e	1.20 BSC	
H	11.48	11.88
H1	6.80	7.10
i	0.10 REF	
j1	0.46 REF	
j2	0.20 REF	
K	2.80 REF	
L	1.40	2.10
L1	0.50	0.90
L2	0.48	0.72
L3	0.30	0.80
Q	6.80 REF	
R	3.00	3.20

Note:

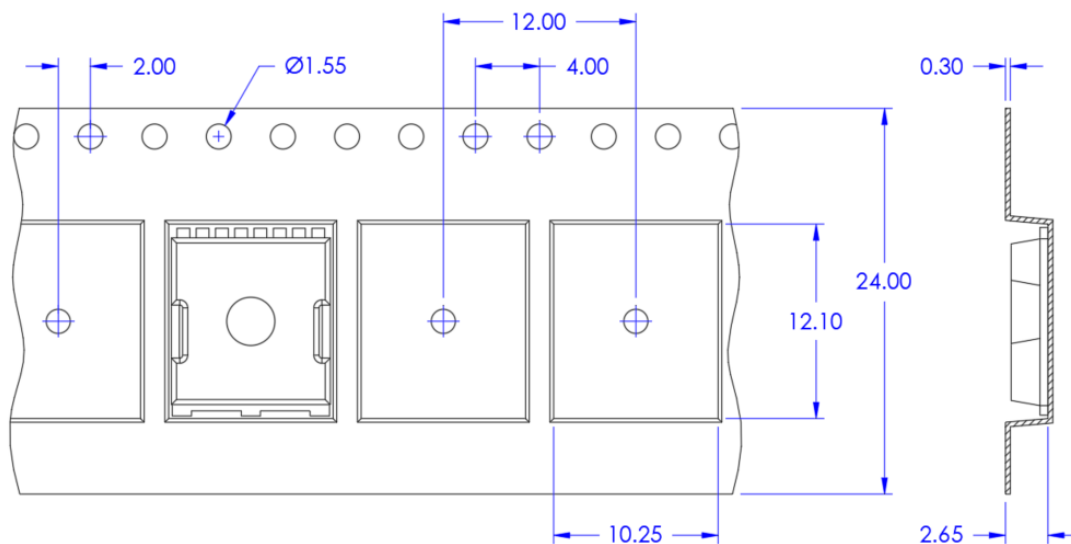
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes

PART MARKING

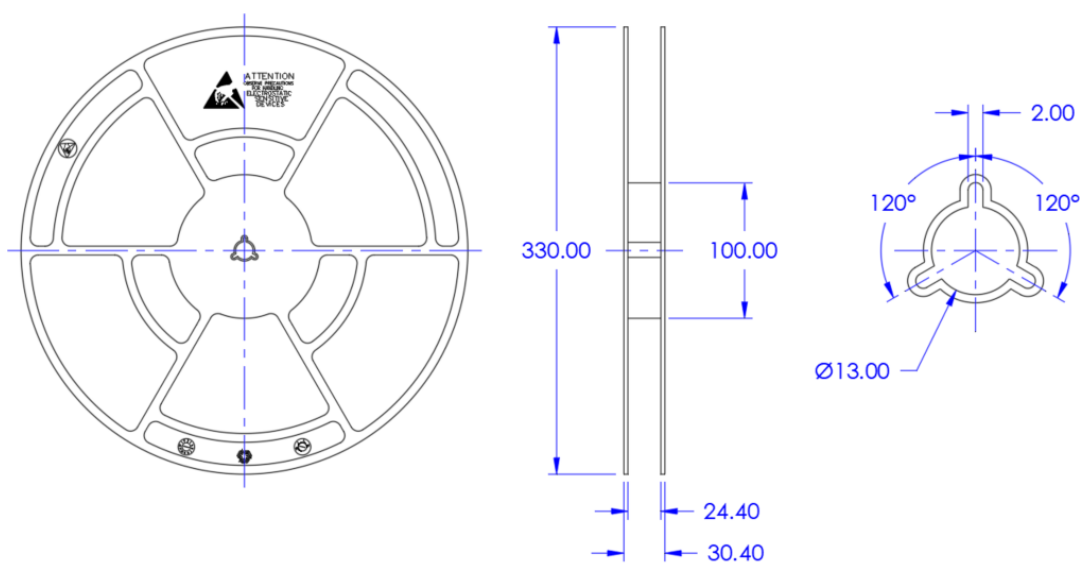


PACKING TYPE


Carrier Tape



Reel



All dimensions in millimeters
Quantity per Reel: 2000 units

	TOLL PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION	Page 4 of 4
	DS_TOLL	Rev B

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REVISION HISTORY

Revision	Create Date (mm/dd/yyyy)	Description of Change	Initiator of Change
A	10/13/2023	Initial Production Release	Glenn Galang
B	01/31/2024	Corrected device orientation inside carrier tape pocket (Page 3)	Glenn Galang

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