UHP112
Two-Port PCI-to-USB OpenHCI Host Controller - Product Brief

Features

- 32-bit, 33 MHz PCI interface compliant with *PCI Local Bus Specification Revision 2.1s*
- Two downstream USB ports
- Full compliance with *Universal Serial Bus Specification Revision 1.1*
- *OpenHCI Open Host Controller Interface Specification for USB Release 1.0a* compatible
- Provides advanced power management capabilities compliant with *PCI Bus Power Management Interface Specification Revision 1.1*
- Fully compatible with *Microsoft Windows** Standard OpenHCD Drivers
- Supports legacy keyboard and mouse devices
- Integrated dual-speed USB transceivers
- 3 V or 5 V switchable PCI signaling
- 100-pin TQFP
- Evaluation kit available

Applications

- Seamless integration with 3 V or 5 V PCI-based computer products
- Supports all USB compliant devices and hubs

Description

The Transdimension's UHP112 provides a single-chip PCI-to-Universal Serial Bus (USB) solution. The UHP112 interfaces directly to any 32-bit 33 MHz PCI bus and is ideal for either onboard applications or add-in card applications. It can easily be configured to communicate in either a 3 V PCI environment or 5 V PCI environment simply by selecting the appropriate communications voltage level on the VIO input pin.

The UHP112 is a 3.3 V device fabricated in 0.35 μm technology. Integrated dual-speed USB transceivers enable a single-chip PCI-to-USB solution.

The UHP112 supports the legacy peripherals feature, as defined in the *OpenHCI Specification Release 1.0a*.

An advanced power management capabilities interface compliant with *PCI Bus Power Management Interface Specification Revision 1.1* is present to offer a variety of power-savings modes to the host system.

The UHP112 provides two downstream USB ports for connectivity with any USB compliant device or hub. Full-speed or low-speed peripherals are supported along with all of the USB transfer types: control, interrupt, bulk, or isochronous. The UHP112's OpenHCI compliance offers significant USB performance benefits and reduced CPU overhead compared to other host controllers.

The UHP112 is fully compatible with the *Microsoft Windows* Standard OpenHCD Drivers.

The UHP112 is supported natively as an OHCI compliant host controller under Windows 98, ME, XP and CE, as well as under MacOS and Linux. For customers using other operating systems, SoftConnex Technologies' USBLink Host solution supports a wide range of products, such as AMX, ITRON, Linux, LynxOS, MS-DOS, Nucleus, OS-40, PowerTV, QNX, ThreadX, VRTX and VxWorks.

USBLink Host is also distinguished by the variety of USB devices that it can support, including: printers; audio, communication, human interface and mass storage devices; digital still and video cameras; Hubs; MP3 players; Host to Host cables and Bluetooth connectivity products. In addition, USBLink Host runs on both little endian (x86, ARM, SA, SH, ST) and big endian (PPC, MIPS) processors. For more information, please visit www.softconnex.com.

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*SoftConnex Technologies is a wholly owned subsidiary of Transdimension Inc.

Description (continued)

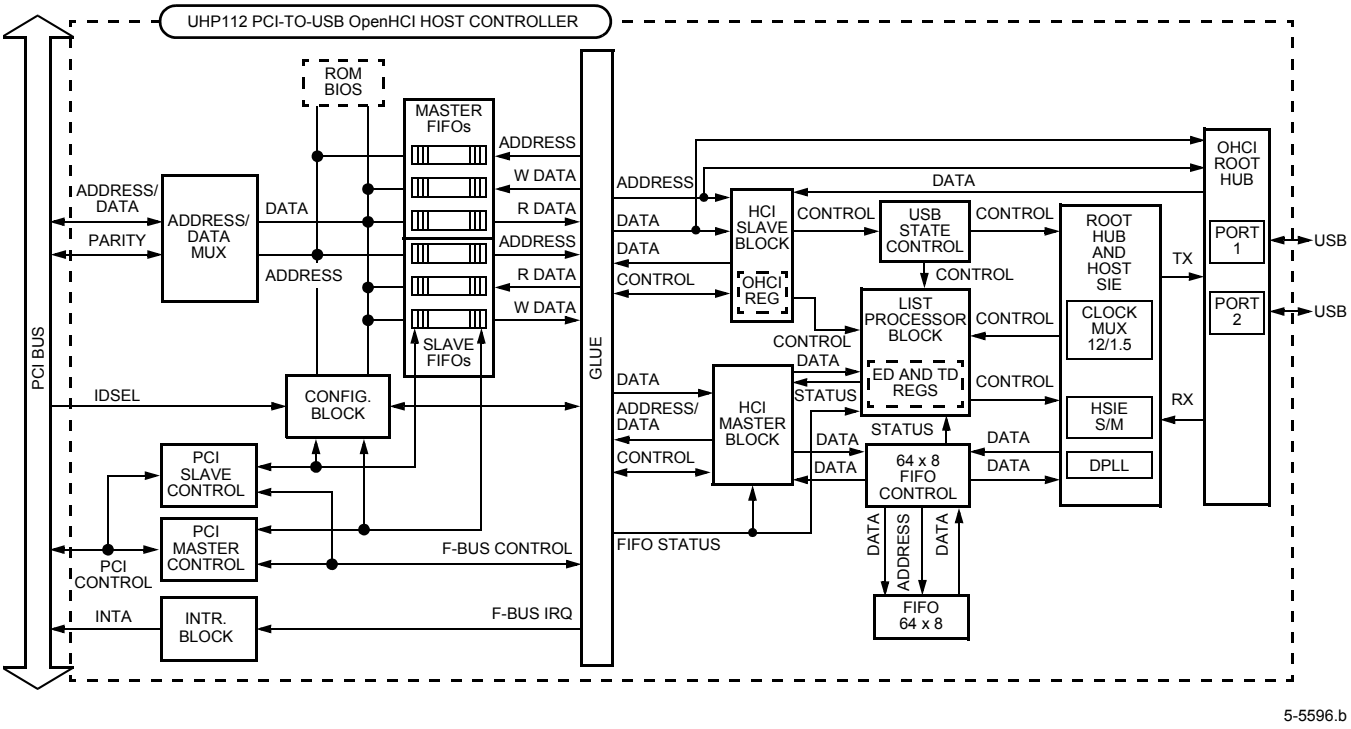

Figure 1. UHP112 Interconnection Diagram

Applicable Documents and Specifications

- *PCI Local Bus Specification Revision 2.1s*., June 1, 1995. PCI Special Interest Group.
- *Universal Serial Bus Specification Revision 1.1*., September 23, 1998. Compaq/Digital Equipment Corporation/ IBM PC Company/Intel/Microsoft/NEC/Northern Telecom.
- *OpenHCI Open Host Controller Interface Specification for USB Release 1.0a*., July 31, 1997. Compaq/Microsoft/ National Semiconductor.
- *PCI Bus Power Management Interface Specification Revision 1.1*., December 18, 1998. PCI Special Interest Group.

Pin Information (continued)

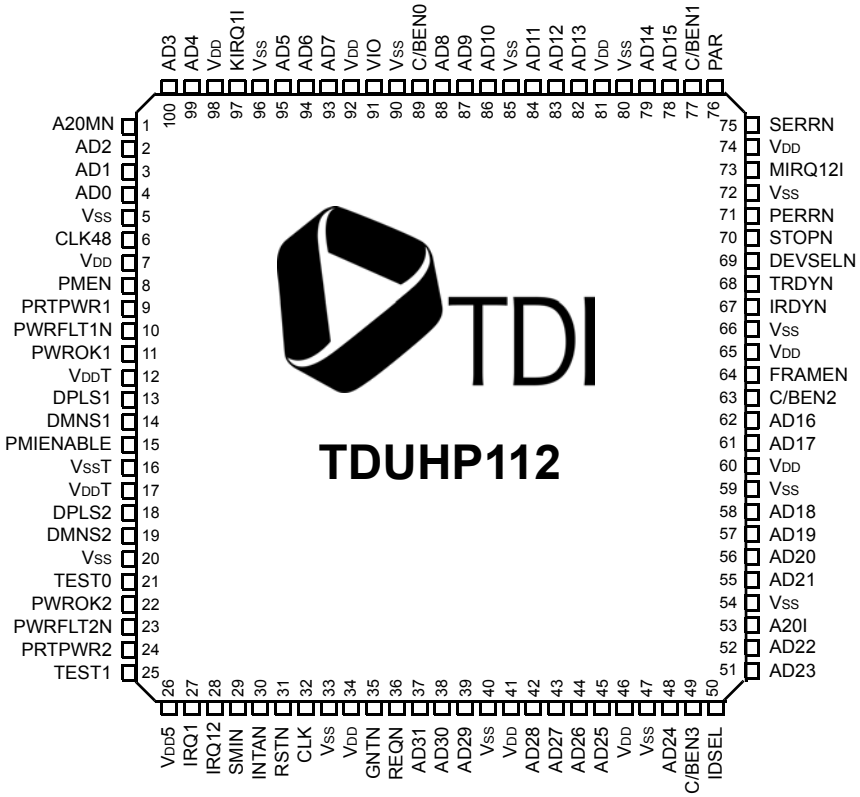

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Figure 2. Pin Diagram (100-Pin TQFP)

Pin Information (continued)

Table 1. Numeric Pin Cross Reference

Pin	Symbol*	Pin	Symbol*	Pin	Symbol*	Pin	Symbol*
1	A20MN	26	VDD5	51	AD23	76	PAR
2	AD2	27	IRQ1	52	AD22	77	C/BEN1
3	AD1	28	IRQ12	53	A20I	78	AD15
4	AD0	29	SMIN	54	VSS	79	AD14
5	VSS	30	INTAN	55	AD21	80	VSS
6	CLK48	31	RSTN	56	AD20	81	VDD
7	VDD	32	CLK	57	AD19	82	AD13
8	PMEN	33	VSS	58	AD18	83	AD12
9	PRTPWR1	34	VDD	59	VSS	84	AD11
10	PWRFLT1N	35	GNTN	60	VDD	85	VSS
11	PWROK1	36	REQN	61	AD17	86	AD10
12	VDDT	37	AD31	62	AD16	87	AD9
13	DPLS1	38	AD30	63	C/BEN2	88	AD8
14	DMNS1	39	AD29	64	FRAMEN	89	C/BEN0
15	PMIENABLE	40	VSS	65	VDD	90	VSS
16	VSST	41	VDD	66	VSS	91	VIO
17	VDDT	42	AD28	67	IRDYN	92	VDD
18	DPLS2	43	AD27	68	TRDYN	93	AD7
19	DMNS2	44	AD26	69	DEVSELN	94	AD6
20	VSS	45	AD25	70	STOPN	95	AD5
21	TEST0	46	VDD	71	PERRN	96	VSS
22	PWROK2	47	VSS	72	VSS	97	KIRQ1I
23	PWRFLT2N	48	AD24	73	MIRQ12I	98	VDD
24	PRTPWR2	49	C/BEN3	74	VDD	99	AD4
25	TEST1	50	IDSEL	75	SERRN	100	AD3

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 2. Pin Descriptions

Pin	Symbol*	Type	Description
1	A20MN	Output/Open Drain	**Legacy Gate A20 Output (Active-Low).**
2	AD2	Bidir	**PCI Address/Data Bit.**
3	AD1	Bidir	**PCI Address/Data Bit.**
4	AD0	Bidir	**PCI Address/Data Bit.**
5	VSS	Power	**Device Ground.**
6	CLK48	Input	**USB Clock (48 MHz).**
7	VDD	Power	**Device Power (3.3 V).**
8	PMEN	Output/Open Drain	**Power Management Event (Active-Low).**
9	PRTPWR1	Bidir	**Port 1 Power.** Logic output expected to turn on port 1 power. Bootstrap low for high active. Bootstrap high for low active.
10	PWRFLT1N	Input	**Port 1 Power Fault (Active-Low).** Logic input indicates an overcurrent fault on port 1.
11	PWROK1	Input	**Port 1 Power OK.** Analog or digital input to inform the UHP112 that USB port 1 power is stable (when >4 V).
12	VDDT	Power	**Transceiver Power (3.3 V).**
13	DPLS1	Bidir	**DIfferential USB Port 1 Signals.**
14	DMNS1	Bidir	
15	PMIENABLE	Input	**Power Management Interface Enable Input (Active-High).**
16	VSST	Power	**Transceiver Ground.**
17	VDDT	Power	**Transceiver Power (3.3 V).**
18	DPLS2	Bidir	**Differential USB Port 2 Signals.**
19	DMNS2	Bidir	
20	VSS	Power	**Device Ground.**
21	TEST0	Input	**Test 0.** For device testing. Connect this to ground during normal use. Connect to logic high for NAND tree mode. See NAND Tree Mode on page 2-32.
22	PWROK2	Input	**Port 2 Power OK.** Analog or digital input to inform the UHP112 that USB port 2 power is stable (when >4 V).
23	PWRFLT2N	Input	**Port 2 Power Fault (Active-Low).** Logic input indicates an overcurrent fault on port 2.
24	PRTPWR2	Bidir	**Port 2 Power.** Logic output expected to turn on port 2 power. Bootstrap low for high active. Bootstrap high for low active.
25	TEST1	Input	**Test 1.** For device testing. Tie this to ground during normal use. Connect to logic high for NAND tree mode. See the NAND Tree Mode section on page 2-32.
26	VDD5	Power	**5 V Power for 5 V PCI Operation.** 5 V must be present on this pin while selecting either 3 V PCI or 5 V PCI operation with the VIO pin. See PCI Connection Instructions section on page 2-26.
27	IRQ1	Output/Open Drain	**System Keyboard Interrupt (Active-High).**
28	IRQ12	Output/Open Drain	**System Mouse Interrupt (Active-High).**
29	SMIN	Output/Open Drain	**System Management Interrupt (Active-Low).**
30	INTAN	Output/Open Drain	**PCI Interrupt (Active-Low).**
31	RSTN	Input	**PCI Reset (Active-Low).** Also the chip reset.
32	CLK	Input	**PCI Clock.** 33 MHz input clock.

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

Pin	Symbol*	Type	Description
33	VSS	Power	**Device Ground.**
34	VDD	Power	**Device Power (3.3 V).**
35	GNTN	Input	**PCI Grant Signal (Active-Low).**
36	REQN	Output/3-State	**PCI Request Signal (Active-Low).**
37	AD31	Bidir	**PCI Address/Data Bit.**
38	AD30	Bidir	**PCI Address/Data Bit.**
39	AD29	Bidir	**PCI Address/Data Bit.**
40	VSS	Power	**Device Ground.**
41	VDD	Power	**Device Power (3.3 V).**
42	AD28	Bidir	**PCI Address/Data Bit.**
43	AD27	Bidir	**PCI Address/Data Bit.**
44	AD26	Bidir	**PCI Address/Data Bit.**
45	AD25	Bidir	**PCI Address/Data Bit.**
46	VDD	Power	**Device Power (3.3 V).**
47	VSS	Power	**Device Ground.**
48	AD24	Bidir	**PCI Address/Data Bit.**
49	C/BEN3	Bidir	**PCI Command/Byte Enable.**
50	IDSEL	Bidir	**PCI ID Select.**
51	AD23	Bidir	**PCI Address/Data Bit.**
52	AD22	Bidir	**PCI Address/Data Bit.**
53	A20I	Input	**Legacy Gate A20 Input.**
54	VSS	Power	**Device Ground.**
55	AD21	Bidir	**PCI Address/Data Bit.**
56	AD20	Bidir	**PCI Address/Data Bit.**
57	AD19	Bidir	**PCI Address/Data Bit.**
58	AD18	Bidir	**PCI Address/Data Bit.**
59	VSS	Power	**Device Ground.**
60	VDD	Power	**Device Power (3.3 V).**
61	AD17	Bidir	**PCI Address/Data Bit.**
62	AD16	Bidir	**PCI Address/Data Bit.**
63	C/BEN2	Bidir	**PCI Command/Byte Enable.**
64	FRAMEN	Bidir	**PCI Frame (Active-Low).**
65	VDD	Power	**Device Power (3.3 V).**
66	VSS	Power	**Device Ground.**
67	IRDYN	Bidir	**PCI Initiator Ready (Active-Low).**
68	TRDYN	Bidir	**PCI Target Ready (Active-Low).**
69	DEVSELN	Bidir	**PCI Device Select (Active-Low).**
70	STOPN	Bidir	**PCI Stop (Active-Low).**
71	PERRN	Bidir	**PCI Parity Error (Active-Low).**
72	VSS	Power	**Device Ground.**
73	MIRQ12I	Input	**Legacy Mouse Controller Interrupt Input.**
74	VDD	Power	**Device Power (3.3 V).**

* Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

Pin	Symbol*	Type	Description
75	SERRN	Output/Open Drain	**PCI System Error (Active-Low).**
76	PAR	Bidir	**PCI Parity.**
77	C/BEN1	Bidir	**PCI Command/Byte Enable.**
78	AD15	Bidir	**PCI Address/Data Bit.**
79	AD14	Bidir	**PCI Address/Data Bit.**
80	VSS	Power	**Device Ground.**
81	VDD	Power	**Device Power (3.3 V).**
82	AD13	Bidir	**PCI Address/Data Bit.**
83	AD12	Bidir	**PCI Address/Data Bit.**
84	AD11	Bidir	**PCI Address/Data Bit.**
85	VSS	Power	**Device Ground.**
86	AD10	Bidir	**PCI Address/Data Bit.**
87	AD9	Bidir	**PCI Address/Data Bit.**
88	AD8	Bidir	**PCI Address/Data Bit.**
89	C/BEN0	Bidir	**PCI Command/Byte Enable.**
90	VSS	Power	**Device Ground.**
91	VIO	Power	**Voltage I/O.** This signal is used to indicate to the UHP112 the PCI signaling interface to use (3 V or 5 V PCI signaling). A 3 V on VIO will indicate 3 V PCI signaling while 5 V on VIO will indicate 5 V PCI signaling. This pin may be connected directly to the PCI VIO signal.
92	VDD	Power	**Device Power (3.3 V).**
93	AD7	Bidir	**PCI Address/Data Bit.**
94	AD6	Bidir	**PCI Address/Data Bit.**
95	AD5	Bidir	**PCI Address/Data Bit.**
96	VSS	Power	**Device Ground.**
97	KIRQ1I	Input	**Legacy Keyboard Controller Interrupt Input.**
98	VDD	Power	**Device Power (3.3 V).**
99	AD4	Bidir	**PCI Address/Data Bit.**
100	AD3	Bidir	**PCI Address/Data Bit.**

* Active-low signals within this document are indicated by an N following the symbol names.

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