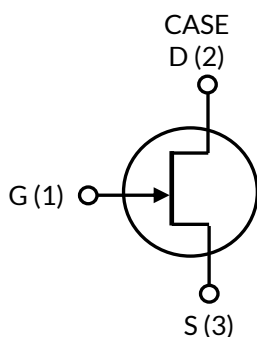


Silicon Carbide (SiC) JFET - EliteSiC, Power N-Channel, TO-247-3L, 1200 V, 66 mohm

Rev. B, January 2025

DATASHEET

UJ3N120065K3S



Description

UnitedSiC offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at $V_{GS} = 0$ V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.

Features

- ♦ Typical on-resistance $R_{DS(on),typ}$ of 66m Ω
- ♦ Voltage controlled
- ♦ Maximum operating temperature of 175°C
- ♦ Extremely fast switching not dependent on temperature
- ♦ Low gate charge
- ♦ Low intrinsic capacitance
- ♦ RoHS compliant

Typical applications

- ♦ Over Current Protection Circuits
- ♦ DC-AC Inverters
- ♦ Switch mode power supplies
- ♦ Power factor correction modules
- ♦ Motor drives
- ♦ Induction heating

Part Number	Package	Marking
UJ3N120065K3S	TO-247-3L	UJ3N120065K3S



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +3	V
		AC ¹	-30 to +20	V
Continuous drain current ²	I_D	$T_C = 25^\circ\text{C}$	34	A
		$T_C = 100^\circ\text{C}$	25	A
Pulsed drain current ³	I_{DM}	$T_C = 25^\circ\text{C}$	90	A
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	254	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	$^\circ\text{C}$

1. +20V AC rating applies for turn-on pulses <200ns applied with external $R_G > 1\Omega$.

2. Limited by $T_{J,max}$

3. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.45	0.59	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS} = -20\text{V}, I_D = 1\text{mA}$	1200			V
Total drain leakage current	I_{DSS}	$V_{DS} = 1200\text{V}, V_{GS} = -20\text{V}, T_J = 25^\circ\text{C}$		5	30	μA
		$V_{DS} = 1200\text{V}, V_{GS} = -20\text{V}, T_J = 175^\circ\text{C}$		56		
Total gate leakage current	I_{GSS}	$V_{GS} = -20\text{V}, T_J = 25^\circ\text{C}$		0.1	50	μA
		$V_{GS} = -20\text{V}, T_J = 175^\circ\text{C}$		1		μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 2\text{V}, I_D = 10\text{A}, T_J = 25^\circ\text{C}$		55		$\text{m}\Omega$
		$V_{GS} = 0\text{V}, I_D = 10\text{A}, T_J = 25^\circ\text{C}$		66	90	
		$V_{GS} = 2\text{V}, I_D = 10\text{A}, T_J = 175^\circ\text{C}$		122		
		$V_{GS} = 0\text{V}, I_D = 10\text{A}, T_J = 175^\circ\text{C}$		142		
Gate threshold voltage	$V_{G(th)}$	$V_{DS} = 5\text{V}, I_D = 35\text{mA}$	-9.3	-6.6	-4.7	V
Gate resistance	R_G	$f = 1\text{MHz}$, open drain		2.6		Ω

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=100V, V_{GS}=-20V$ $f=100kHz$		1008		pF
Output capacitance	C_{oss}			100		
Reverse transfer capacitance	C_{rss}			95		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to $800V$, $V_{GS}=-20V$		56		pF
C_{oss} stored energy	E_{oss}	$V_{DS}=800V, V_{GS}=-20V$		18		μJ
Total gate charge	Q_G	$V_{DS}=800V, I_D=25A$, $V_{GS} = -18V$ to $0V$		114		nC
Gate-drain charge	Q_{GD}			75		
Gate-source charge	Q_{GS}			16		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=800V, I_D=25A$, Gate Driver $= -18V$ to $0V$, $R_G=1\Omega$, Inductive Load, FWD: UJ2D1215T $T_J=25^\circ C$		32		ns
Rise time	t_r			43		
Turn-off delay time	$t_{d(off)}$			19		
Fall time	t_f			16		
Turn-on energy	E_{ON}			785		μJ
Turn-off energy	E_{OFF}	$V_{DS}=800V, I_D=25A$, Gate Driver $= -18V$ to $0V$, $R_G=1\Omega$, Inductive Load, FWD: UJ2D1215T $T_J=150^\circ C$		150		
Total switching energy	E_{TOTAL}			935		
Turn-on delay time	$t_{d(on)}$			28		ns
Rise time	t_r			42		
Turn-off delay time	$t_{d(off)}$			18		
Fall time	t_f			15		
Turn-on energy	E_{ON}			730		μJ
Turn-off energy	E_{OFF}			146		
Total switching energy	E_{TOTAL}			876		

Typical Performance Diagrams

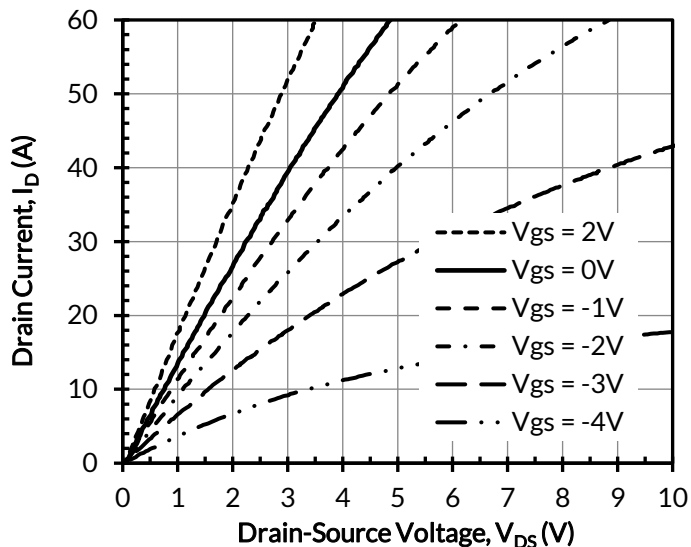


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

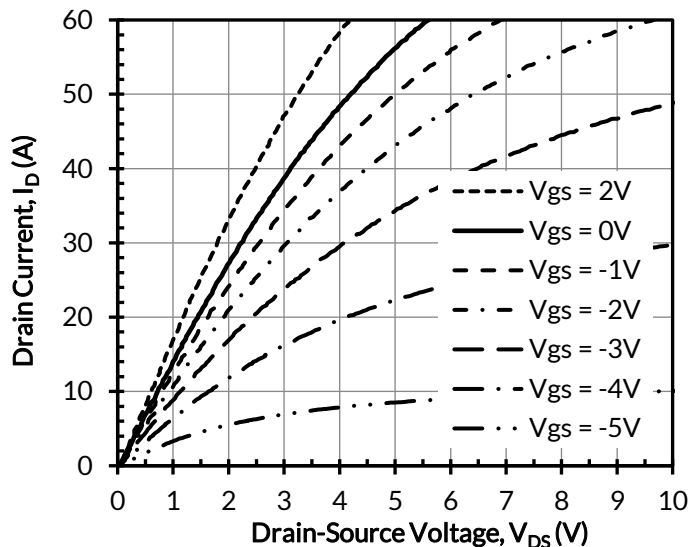


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

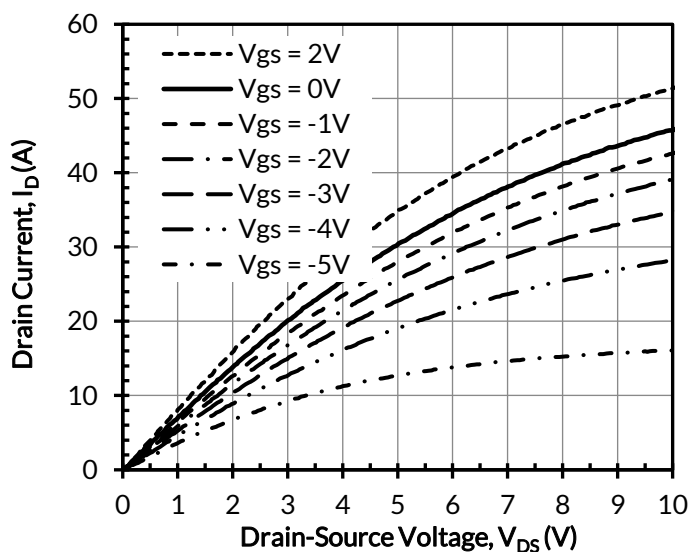


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

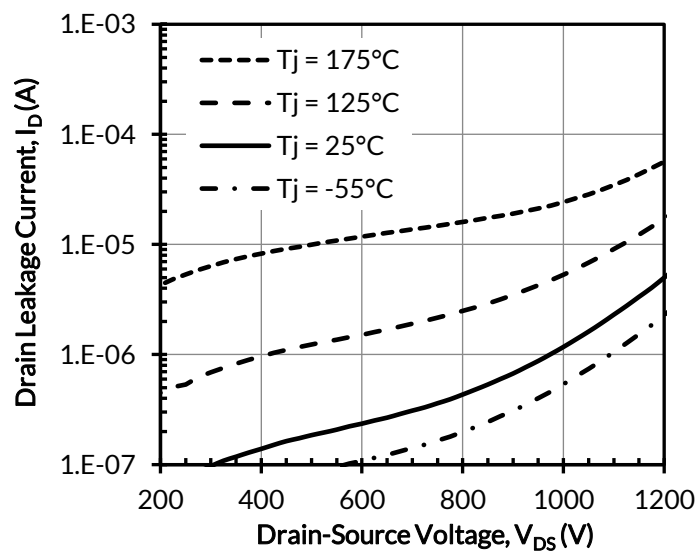


Figure 4. Typical drain-source leakage at $V_{GS} = -20\text{V}$

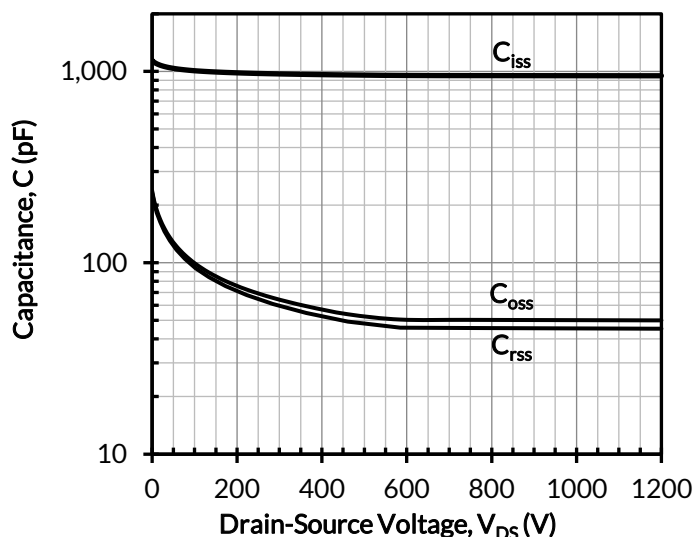


Figure 5. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = -20\text{V}$

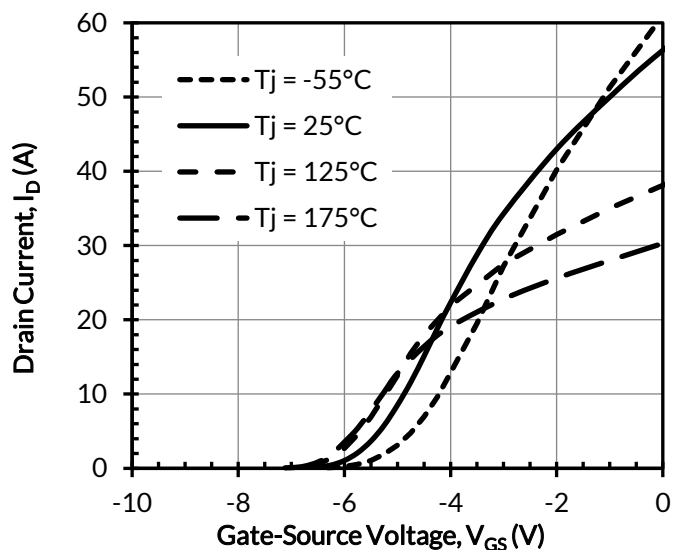


Figure 6. Typical transfer characteristics at $V_{DS} = 5\text{V}$

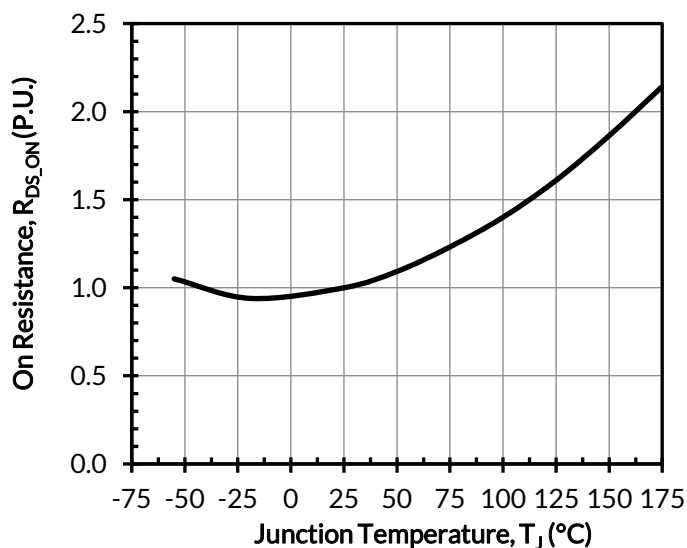


Figure 7. Normalized on-resistance vs. temperature at $V_{GS} = 0\text{V}$ and $I_D = 10\text{A}$

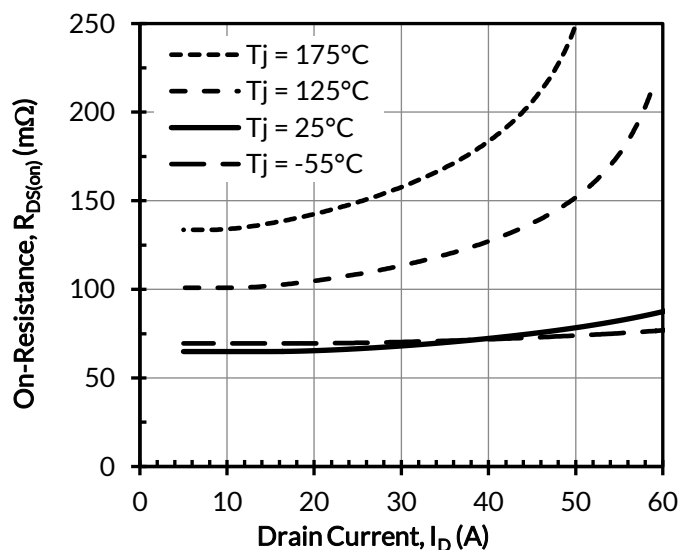


Figure 8. Typical drain-source on-resistances at $V_{GS} = 0\text{V}$

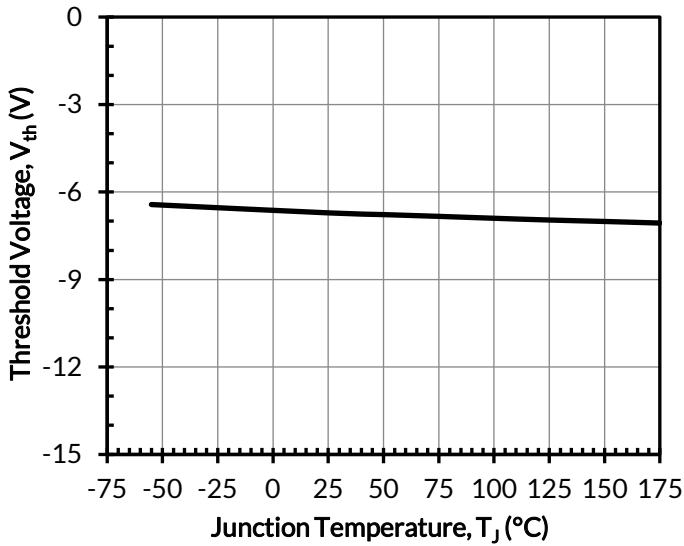


Figure 9. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 35mA$

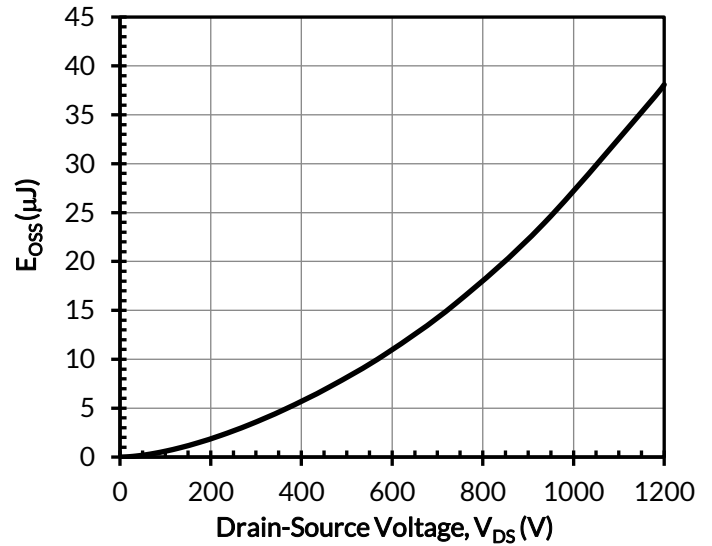


Figure 10. Typical stored energy in C_{OSS} at $V_{GS} = -20V$

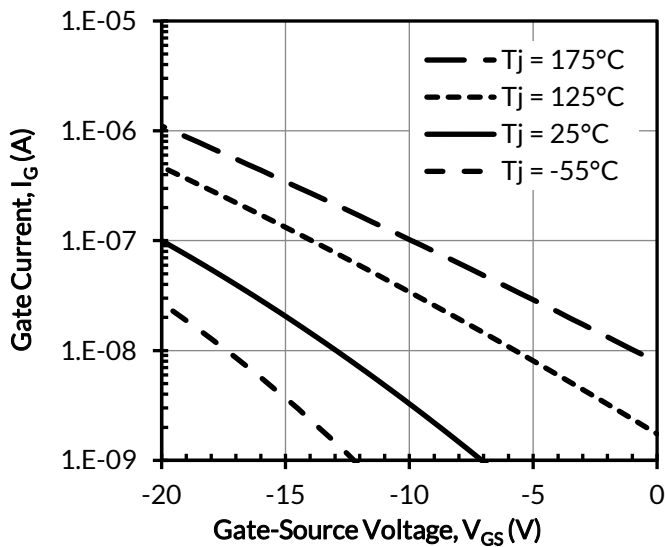


Figure 11. Typical gate leakage at $V_{DS} = 0V$

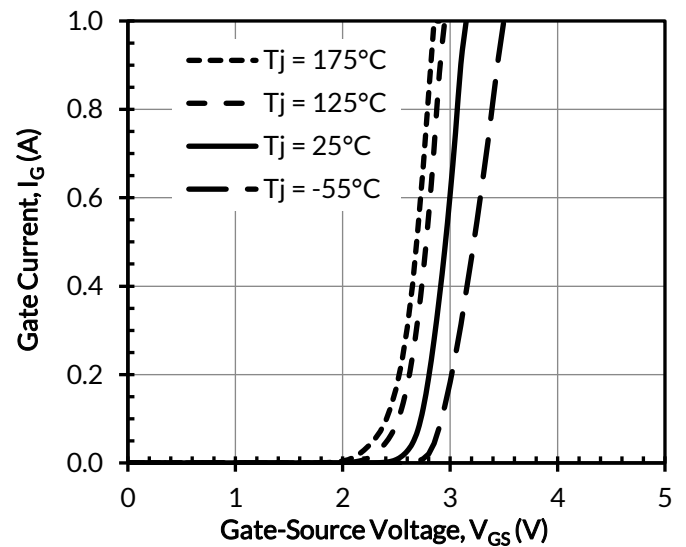


Figure 12. Typical gate forward current at $V_{DS} = 0V$

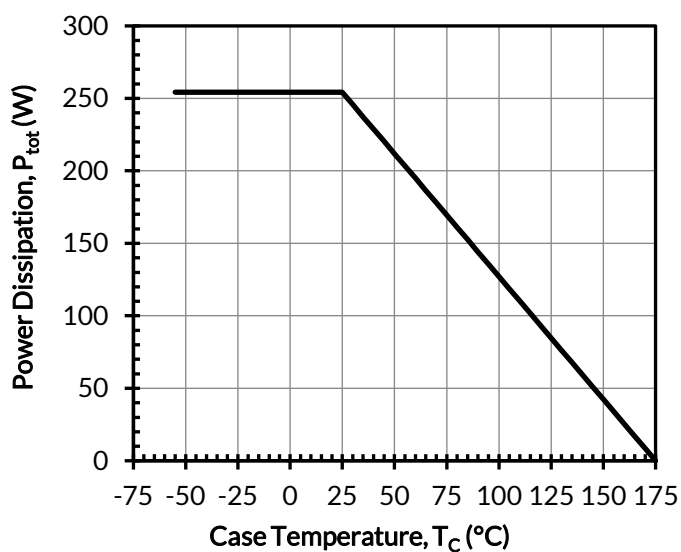


Figure 13. Total power Dissipation

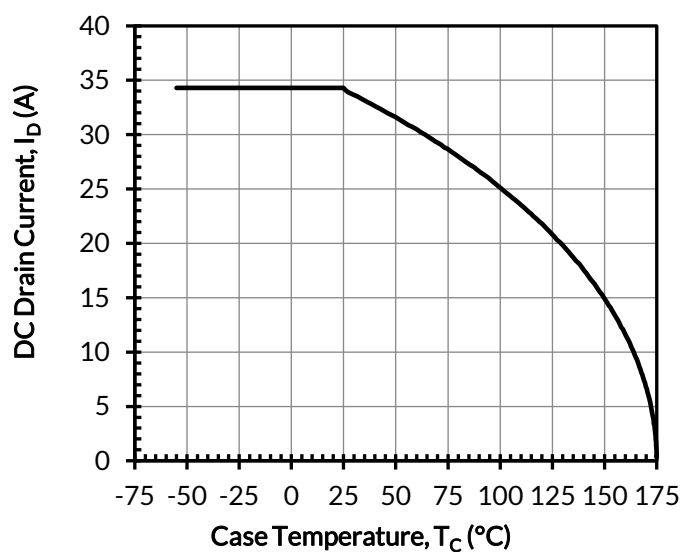


Figure 14. DC drain current derating

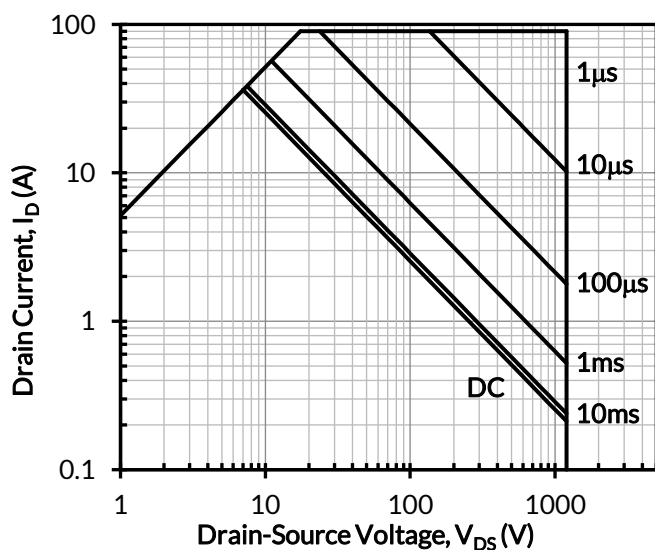


Figure 15. Safe operation area at $T_C = 25^\circ\text{C}$,
Parameter t_p

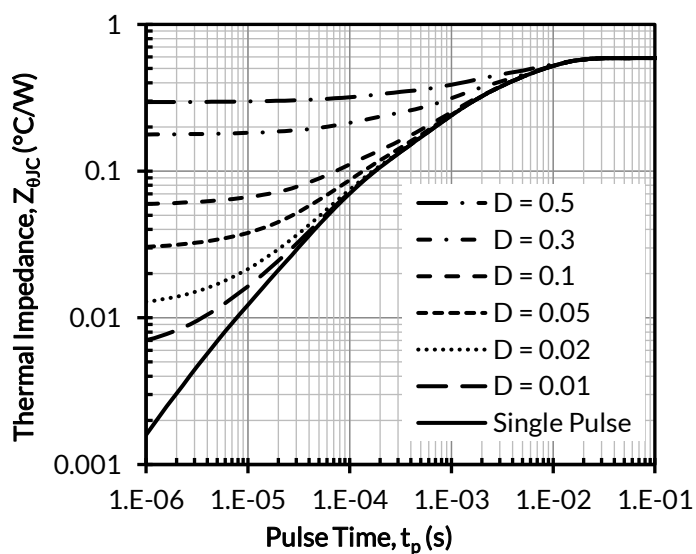


Figure 16. Maximum transient thermal impedance

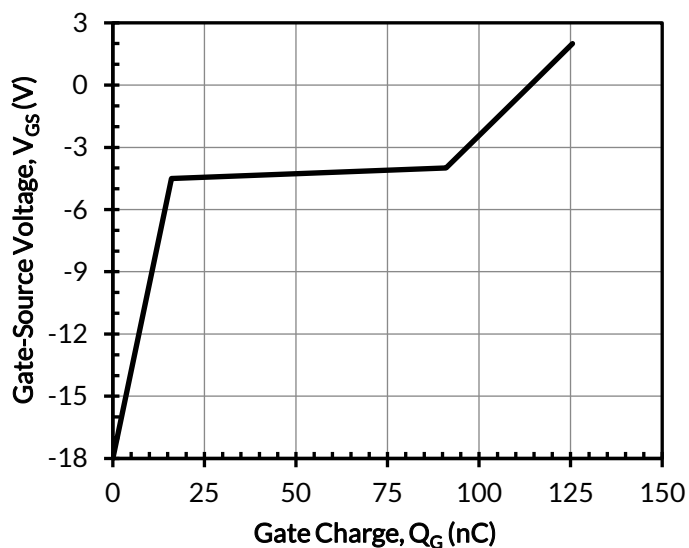


Figure 17. Typical gate charge at $V_{DS} = 800V$ and $I_D = 25A$

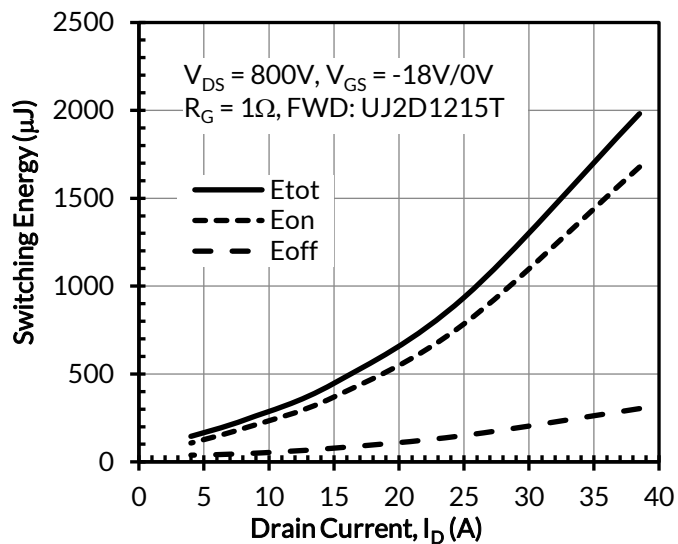


Figure 18. Clamped inductive switching energy vs. drain current at $T_J = 25^\circ C$

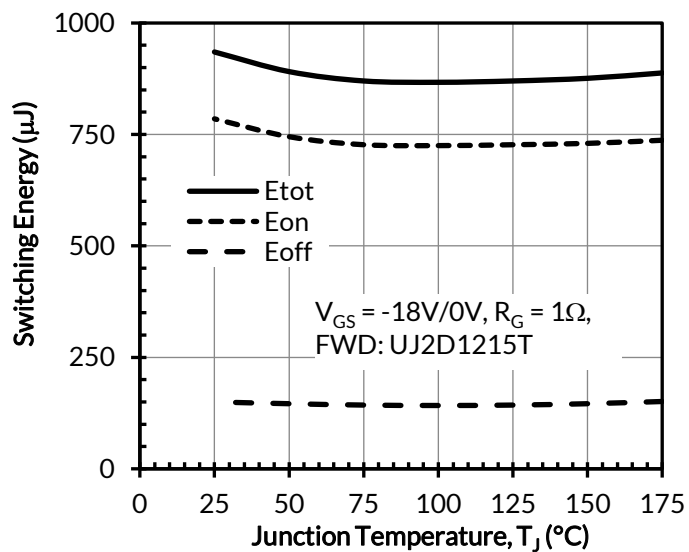


Figure 19. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 800V$ and $I_D = 25A$

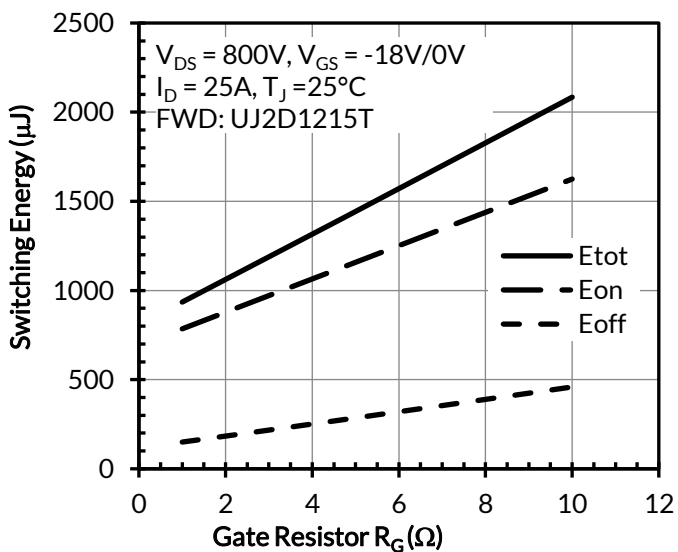


Figure 20. Clamped inductive switching energy vs. gate resistor R_G

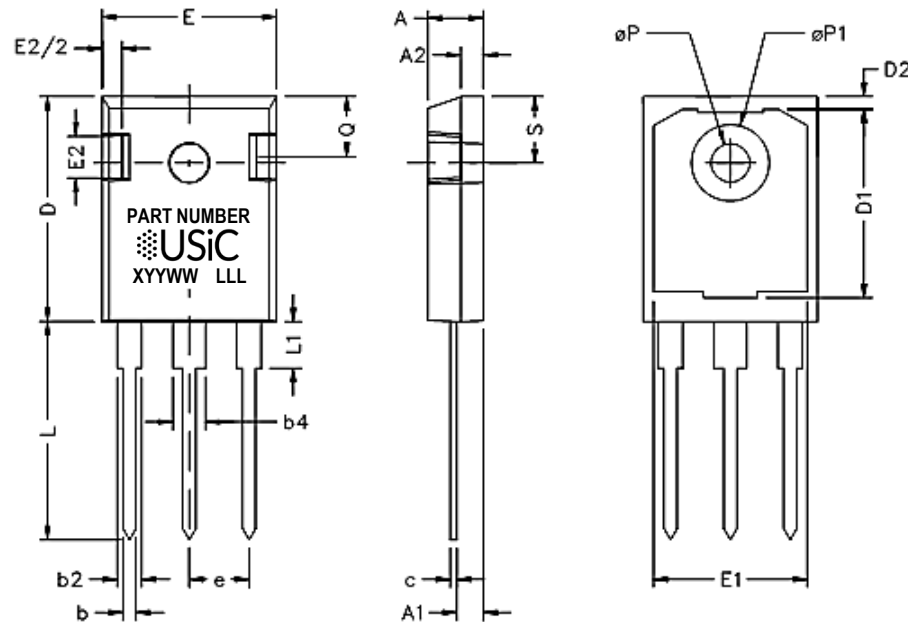
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PACKAGE OUTLINE



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.185	0.209	4.699	5.309
A1	0.087	0.102	2.21	2.61
A2	0.059	0.098	1.499	2.489
b	0.039	0.055	0.991	1.397
b2	0.065	0.094	1.651	2.388
b4	0.102	0.135	2.591	3.429
c	0.015	0.035	0.381	0.889
D	0.819	0.845	20.803	21.463
D1	0.515	-	13.081	-
D2	0.02	0.053	0.508	1.346
E	0.61	0.64	15.494	16.256
e	0.214 BSC		5.44 BSC	
E1	0.53	-	13.462	-
E2	0.135	0.157	3.429	3.988
L	0.78	0.8	19.812	20.32
L1	-	0.177	-	4.496
ØP	0.14	0.144	3.556	3.658
ØP1	0.278	0.291	7.061	7.391
Q	0.212	0.244	5.385	6.198
S	0.243 BSC		6.17 BSC	

PART MARKING**PART NUMBER** **USiC**
XYYYWW LLL

PART NUMBER = REFER TO
DS_PN DECODER FOR DETAILS

X = ASSEMBLY SITE

YY = YEAR

WW = WORK WEEK

LLL = LOT ID

PACKING TYPE

ANTI-STATIC TUBE

QUANTITY /TUBE : 30 UNITS

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