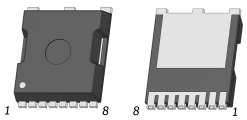
Silicon Carbide (SiC) JFET – EliteSiC, Power N-Channel, H-PDSO-F8, 750 V, 4.3 mohm

UJ4N075004L8S



H-PDSO-F8
CASE 740AA

Description

onsemi's UJ4N075004L8S is a 750 V, 4.3 mΩ high-performance Gen 4 normally-on SiC JFET transistor. This device exhibits ultra-low on resistance ($R_{DS(on)}$) in a compact H-PDSO-F8 package, making it an ideal fit to address the challenging thermal and space constraints of solid-state circuit breakers and relay applications. Additionally, the JFET is a robust device technology capable of the high-energy switching required in circuit protection applications.

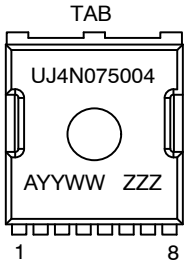
Features

- Single Digit On-Resistance in a H-PDSO-F8 SMDpackage
- Operating Temperature: 175 °C (Max)
- High Pulse Current Capability
- Excellent Device Robustness
- Silver-Sintered Die Attach for Excellent Thermal Resistance
- Short Circuit Rated
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Typical Applications

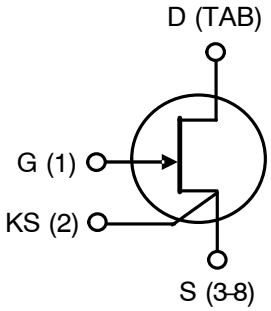
- Solid State / Semiconductor Circuit Breaker
- Solid State / Semiconductor Relay
- Battery Disconnects
- Surge Protection
- Inrush Current Control

MARKING DIAGRAM



UJ4N075004	= Specific Device Number
A	= Assembly Location
YY	= Year
WW	= Work Week
ZZZ	= Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Value	Unit
V_{DS}	Drain-Source Voltage		750	V
V_{GS}	Gate-Source Voltage	DC	−30 to +3	V
		AC (Note 1)	−30 to +30	V
I_D	Continuous Drain Current (Note 2)	T_C < 145 °C	120	A
I_{DM}	Pulsed Drain Current (Note 3)	T_C = 25 °C	588	A
T_{SC}	Short Circuit Withstand Time	V_{DS} = 400 V, $T_{J(START)}$ = 175 °C	5	μS
P_{tot}	Power Dissipation	T_C = 25 °C	1153	W
$T_{J,max}$	Maximum Junction Temperature		175	°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to 175	°C
T_{solder}	Reflow Soldering Temperature	Reflow MSL 1	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. +30 V AC rating applies for turn-on pulses < 200 ns applied with external R_G > 1 Ω.
2. Limited by Bondwires
3. Pulse width t_p limited by $T_{J,max}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		–	0.10	0.13	°C/W

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – STATIC						
BV_{DS}	Drain-Source Breakdown Voltage	V_{GS} = −20 V, I_D = 2 mA	750	–	–	V
I_{DSS}	Total Drain Leakage Current	V_{DS} = 750 V, V_{GS} = −20 V, T_J = 25 °C	–	13	120	μA
		V_{DS} = 750 V, V_{GS} = −20 V, T_J = 175°C	–	65	–	
I_{GSS}	Total Gate Leakage Current	V_{GS} = −20 V , T_J = 25 °C	–	0.1	100	μA
		V_{GS} = −20 V , T_J = 175 °C	–	0.3	–	μA
$R_{DS(on)}$	Drain-Source On-resistance	V_{GS} = 2 V, I_D = 80 A, T_J = 25 °C	–	4.3	–	mΩ
		V_{GS} = 0 V, I_D = 80 A, T_J = 25 °C	–	4.9	6.6	
		V_{GS} = 2 V, I_D = 80 A, T_J = 175 °C	–	9.9	–	
		V_{GS} = 0 V, I_D = 80 A, T_J = 175 °C	–	11.5	–	
$V_{G(th)}$	Gate Threshold Voltage	V_{DS} = 5 V, I_D = 180 mA	−8.3	−6.0	−3.7	V
R_G	Gate Resistance	f = 1 MHz, open drain	–	0.8	–	Ω
TYPICAL PERFORMANCE – DYNAMIC						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = −20 V, f = 100 kHz	–	3028	–	pF
C_{oss}	Output Capacitance		–	364	–	
C_{rss}	Reverse Transfer Capacitance		–	360	–	
$C_{oss(er)}$	Effective Output Capacitance, Energy Related	V_{DS} = 0 V to 400 V, V_{GS} = −20 V	–	448	–	pF
E_{oss}	C_{OSS} Stored Energy	V_{DS} = 400 V, V_{GS} = −20 V	–	36	–	μJ
Q_G	Total Gate Charge	V_{DS} = 400 V, I_D = 80 A, V_{GS} = −18 V to 0 V	–	400	–	nC
Q_{GD}	Gate-Drain Charge		–	270	–	
Q_{GS}	Gate-Source Charge		–	60	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL PERFORMANCE DIAGRAMS

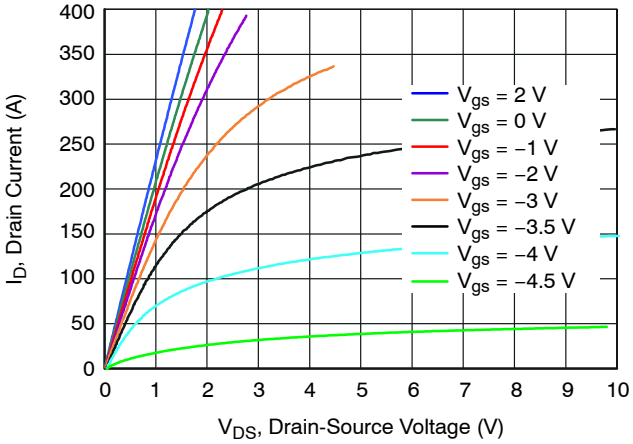


Figure 1. Typical Output Characteristics at T_J = −55 °C, t_p < 250 μs

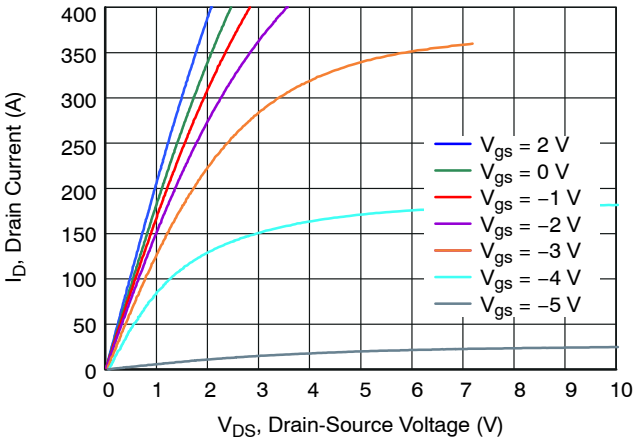


Figure 2. Typical Output Characteristics at T_J = 25 °C, t_p < 250 μs

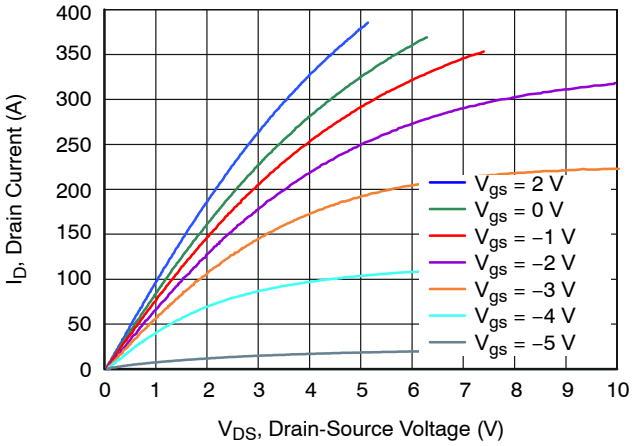


Figure 3. Typical Output Characteristics at T_J = 175 °C, t_p < 250 μs

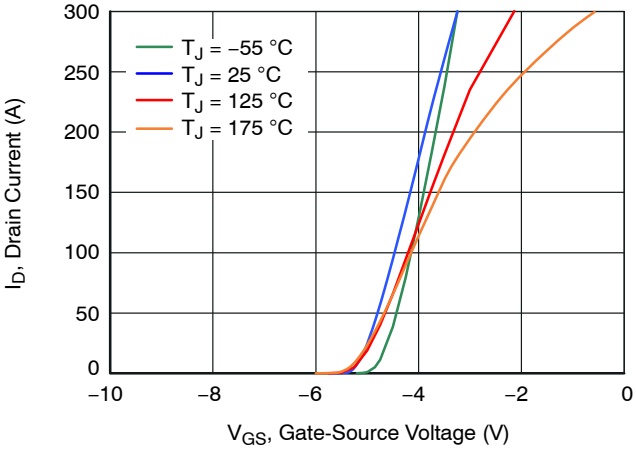


Figure 4. Typical Transfer Characteristics at V_{DS} = 5 V

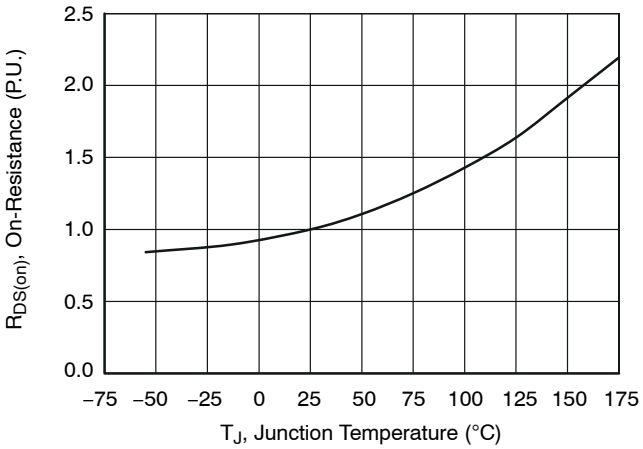


Figure 5. Normalized On-Resistance vs. Temperature at V_{GS} = 0 V and I_D = 80 A

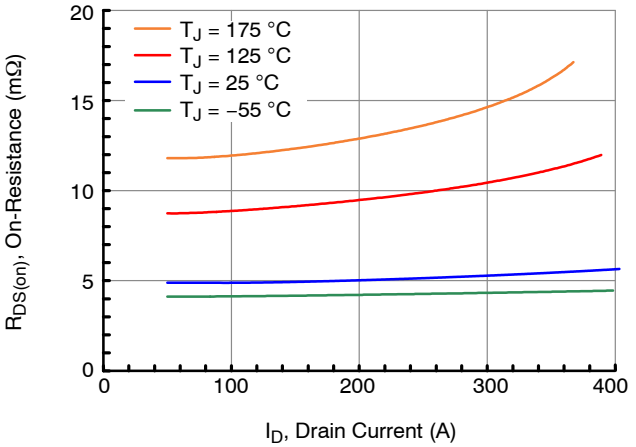


Figure 6. Typical Drain-Source On-Resistance V_{GS} = 0 V

TYPICAL PERFORMANCE DIAGRAMS (continued)

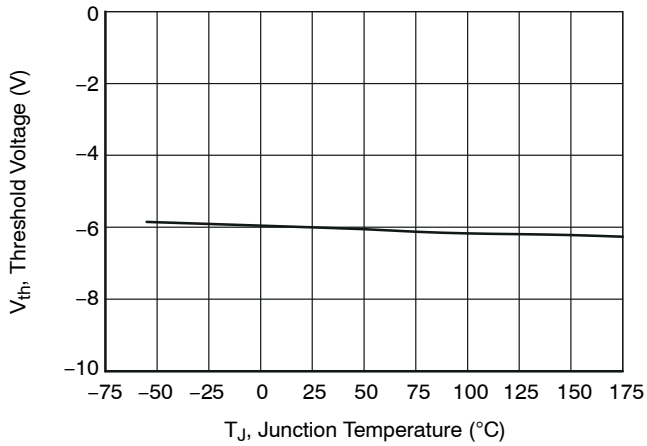


Figure 7. Threshold Voltage vs. Junction Temperature at V_{DS} = 5 V and I_D = 180 mA

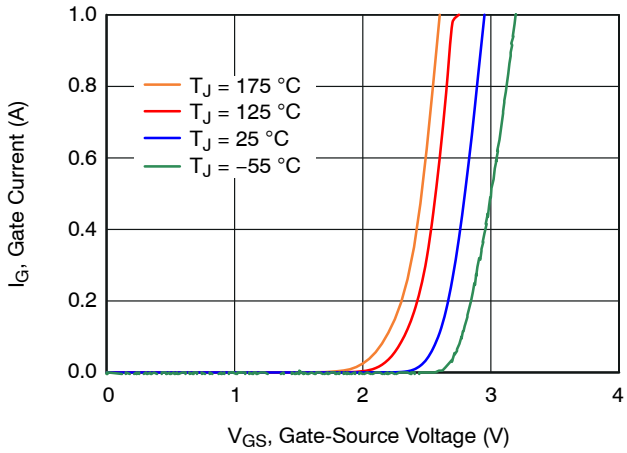


Figure 8. Typical Gate Forward Current at V_{DS} = 0 V

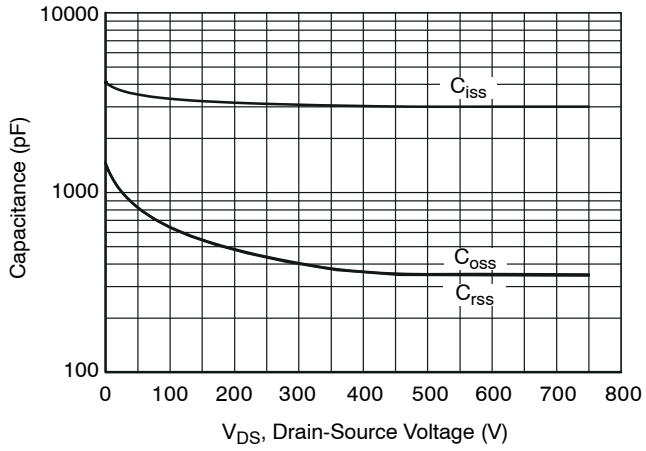


Figure 9. Typical Capacitances at f = 100 KHz and V_{GS} = −20 V

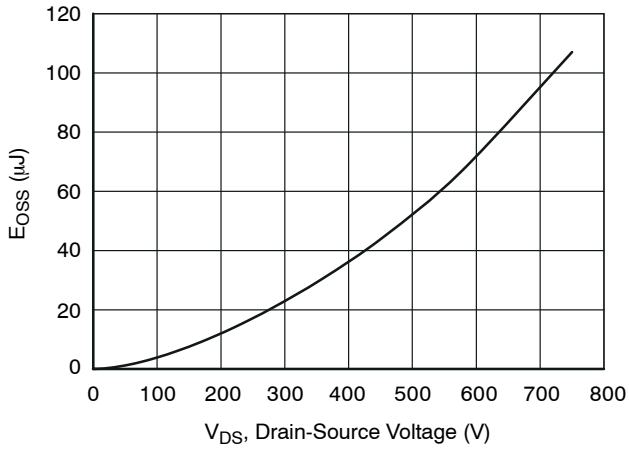


Figure 10. Typical Stored Energy in C_{OSS} at V_{GS} = −20 V

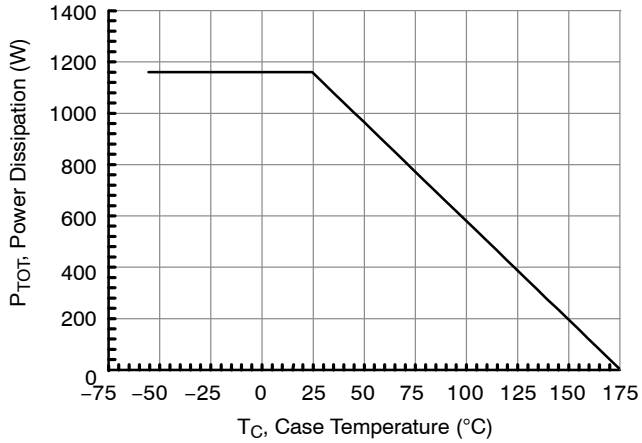


Figure 11. Total Power Dissipation

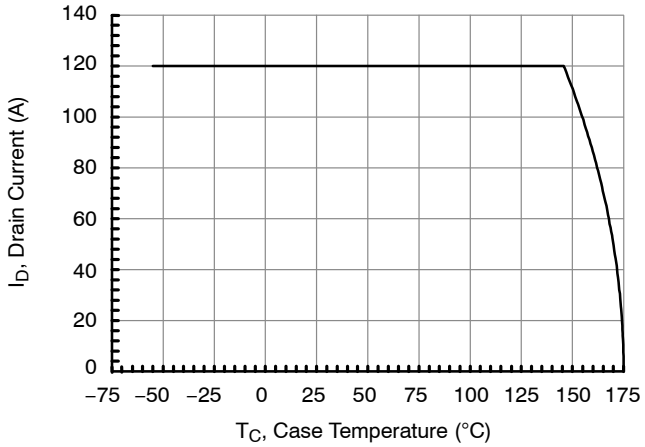


Figure 12. DC Drain Current Derating

TYPICAL PERFORMANCE DIAGRAMS (continued)

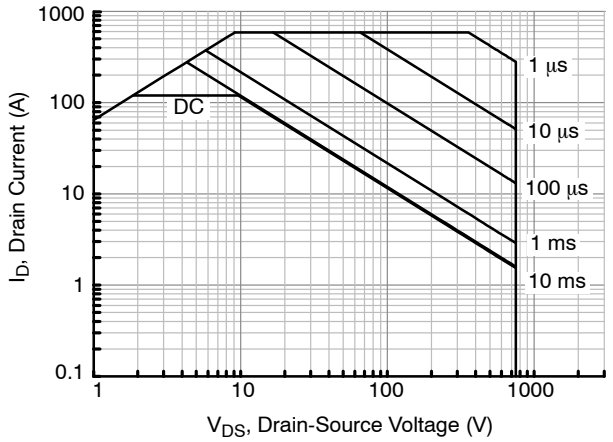


Figure 13. Safe Operation Area at T_C = 25 °C, Parameter t_p

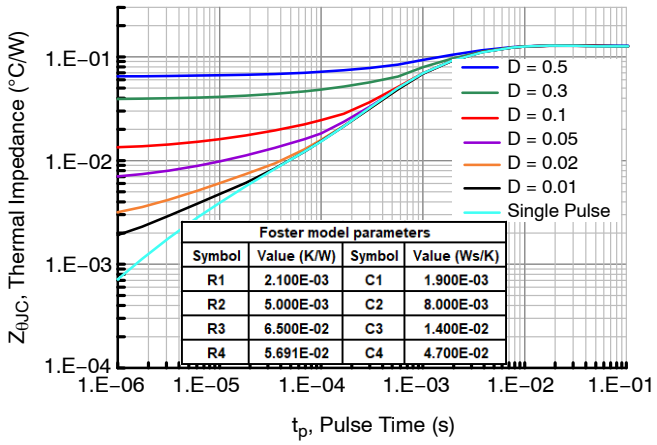


Figure 14. Maximum Transient Thermal Impedance

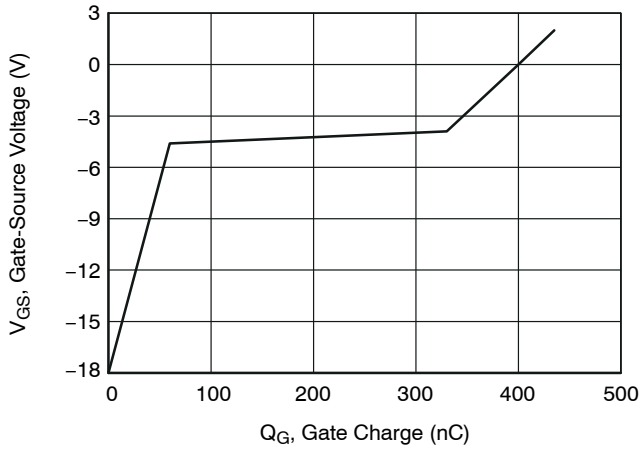


Figure 15. Typical Gate Charge at V_{DS} = 400 V and I_D = 80 A

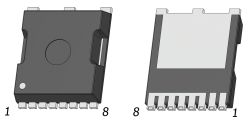
ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
UJ4N075004L8S	UJ4N075004	H-PDSO-F8 (Pb-Free, Halogen Free)	2,000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

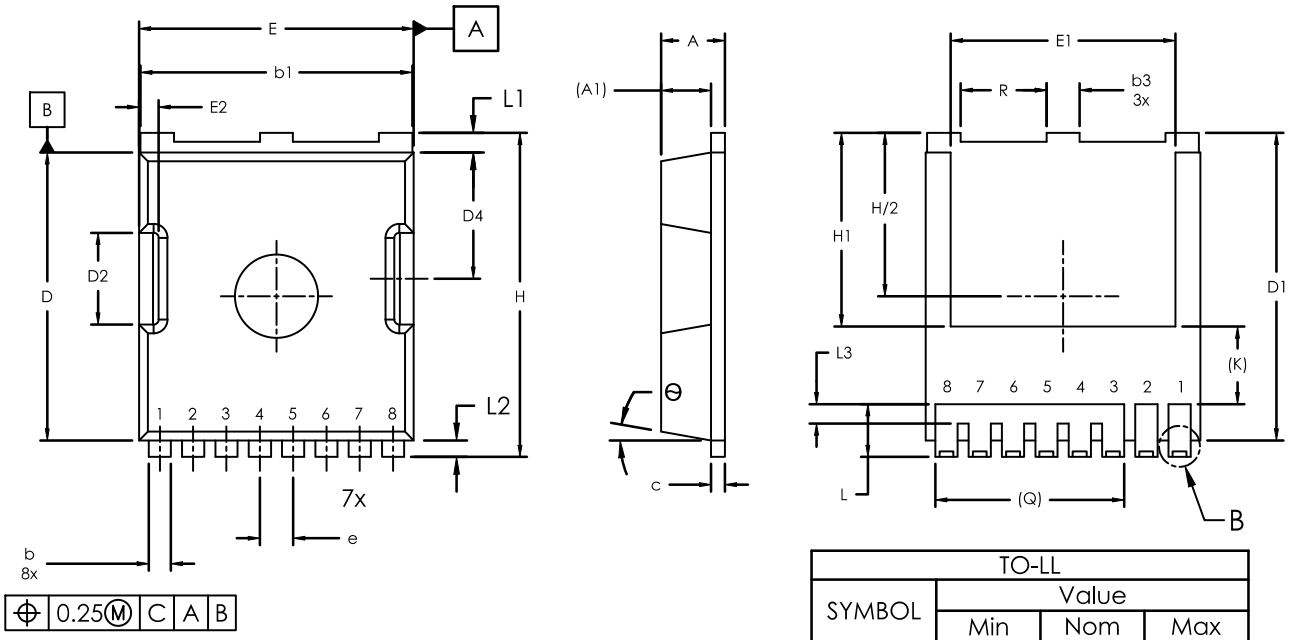
REVISION HISTORY

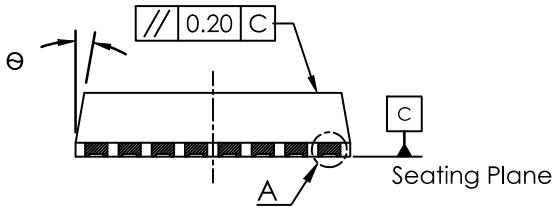
Revision	Description of Changes	Date
C	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with onsemi standards for SiC products.	1/15/2025
2	Converted the Data Sheet to **onsemi** format.	5/7/2025

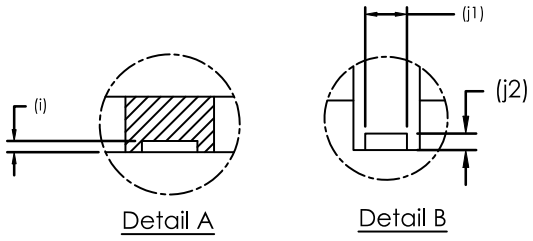


H−PDSO−F8 9.90x10.38x2.30, 1.20P
CASE 740AA
ISSUE B

DATE 24 JUN 2025







TO-LL			
SYMBOL	Value		
	Min	Nom	Max
A	2.15	2.30	2.45
A1		1.80 REF	
b	0.65	0.80	0.90
b1	9.65	9.80	9.95
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	10.88	11.08	11.28
D2	3.15	3.30	3.45
D4	4.40	4.55	4.70
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
E2	0.60	0.70	0.80
e		1.20 BSC	
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
i		0.10 REF	
j1		0.46 REF	
j2		0.20 REF	
K		2.80 REF	
L	1.40	1.90	2.10
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L3	0.30	0.70	0.80
Q		6.80 REF	
R	3.00	3.10	3.20
θ		10°	

Note:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Dimensions does not include Burrs and Mold Flashes

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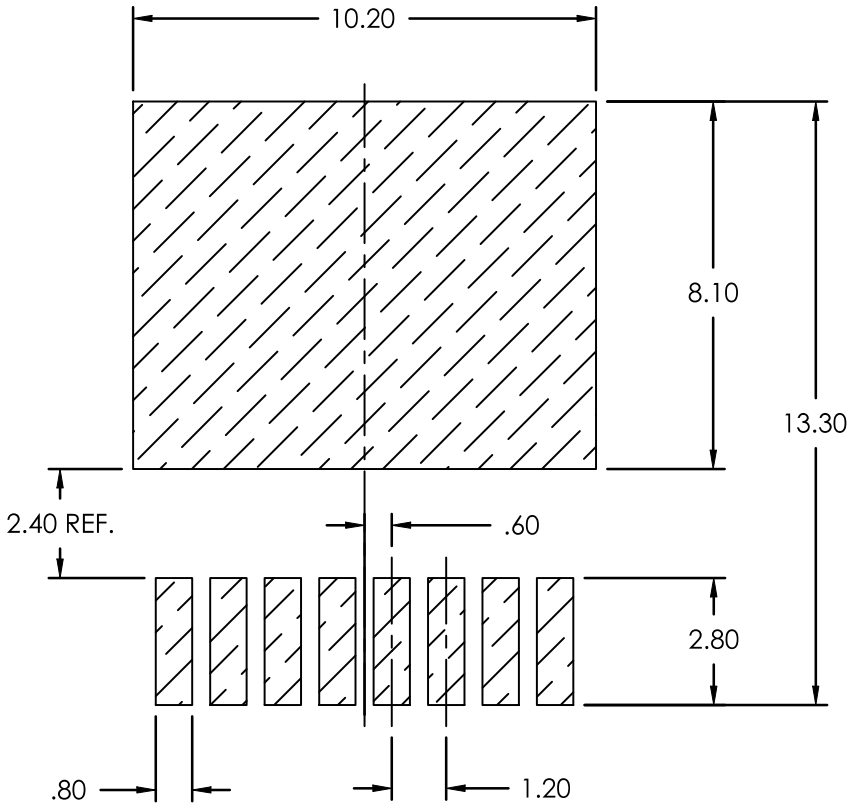
DESCRIPTION:	**H−PDSO−F8 9.90x10.38x2.30, 1.20P**		**PAGE 1 OF 2**

H−PDSO−F8 9.90x10.38x2.30, 1.20P
CASE 740AA
ISSUE B

DATE 24 JUN 2025

RECOMMENDED PCB LAND PATTERN



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales