

# Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TO-247-4L, 750 V, 9 mohm

SiC JFET w/ Si MOSFET

## UJ4SC075009K4S

### Description

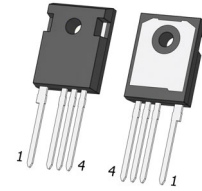
The UJ4SC075009K4S is a 750 V, 9 mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-4L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

### Features

- On-Resistance  $R_{DS(on)}$ : 9 mΩ (typ)
- Operating Temperature: 175 °C (Max)
- Excellent Reverse Recovery:  $Q_{rr} = 322$  nC
- Low Body Diode  $V_{FSD}$ : 1.1 V
- Low Gate Charge :  $Q_G = 75$  nC
- Threshold Voltage  $V_{G(th)}$ : 4.5 V (typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2
- TO-247-4L Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

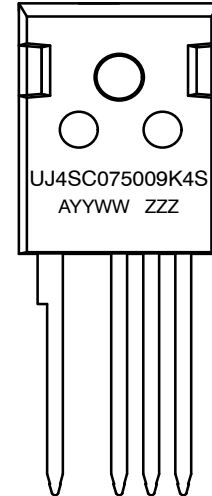
### Typical Applications

- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating



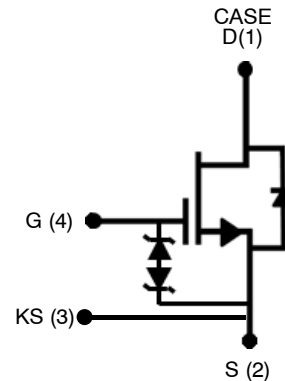
TO-247-4L  
CASE 340AN

### MARKING DIAGRAM



UJ4SC075009K4S = Specific Device Number  
A = Assembly Location  
YY = Year  
WW = Work Week  
ZZZ = Lot ID

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

# UJ4SC075009K4S

## MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Value	Unit
V <sub>DS</sub>	Drain-Source Voltage		750	V
V <sub>GS</sub>	Gate-Source Voltage	DC	-20 to +20	V
		AC (f > 1 Hz)	-25 to +25	V
I <sub>D</sub>	Continuous Drain Current (Note 1)	T <sub>C</sub> < 61 °C	106	A
		T <sub>C</sub> = 100 °C	86	A
I <sub>DM</sub>	Pulsed Drain Current (Note 2)	T <sub>C</sub> = 25 °C	344	A
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 3)	L = 15 mH, I <sub>AS</sub> = 5.2 A	202	mJ
dv/dt	SiC FET dv/dt Ruggedness	V <sub>DS</sub> ≤ 500 V	100	V/ns
P <sub>tot</sub>	Power Dissipation	T <sub>C</sub> = 25 °C	375	W
T <sub>J,max</sub>	Maximum Junction Temperature		175	°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to 175	°C
T <sub>L</sub>	Max. Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		250	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Limited by bondwires
- Pulse width t<sub>p</sub> limited by T<sub>J,max</sub>
- Starting T<sub>J</sub> = 25 °C

## THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case		-	0.31	0.40	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = +25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### TYPICAL PERFORMANCE – STATIC

BV <sub>DS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	750	-	-	V	
I <sub>DSS</sub>	Total Drain Leakage Current	V <sub>DS</sub> = 750 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25 °C	-	4.0	84	μA	
		V <sub>DS</sub> = 750 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	35	-		
I <sub>GSS</sub>	Total Gate Leakage Current	V <sub>DS</sub> = 0 V, T <sub>J</sub> = 25 °C V <sub>GS</sub> = -20 V / + 20 V	-	2	±20	μA	
R <sub>DS(on)</sub>	Drain-Source On-resistance	V <sub>GS</sub> = 12 V, I <sub>D</sub> = 70 A	T <sub>J</sub> = 25 °C	-	9	11.5	mΩ
			T <sub>J</sub> = 125 °C	-	14.8	-	
			T <sub>J</sub> = 175 °C	-	19.4	-	
V <sub>G(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 10 mA	3.5	4.5	5.5	V	
R <sub>G</sub>	Gate Resistance	f = 1 MHz, open drain	-	2.3	-	Ω	

### TYPICAL PERFORMANCE – REVERSE DIODE

I <sub>S</sub>	Diode Continuous Forward Current (Note 1)	T <sub>C</sub> < 61 °C	-	-	106	A
I <sub>S,pulse</sub>	Diode Pulse Current (Note 2)	T <sub>C</sub> = 25 °C	-	-	344	A
V <sub>FSD</sub>	Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 35 A, T <sub>J</sub> = 25 °C	-	1.10	1.24	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 35 A, T <sub>J</sub> = 175 °C	-	1.14	-	
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = 400 V, I <sub>S</sub> = 70 A, V <sub>GS</sub> = 0 V, R <sub>G,EXT</sub> = 5 Ω, di/dt = 2500 A/μs, T <sub>J</sub> = 25 °C	-	322	-	nC
t <sub>rr</sub>	Reverse Recovery Time		-	29	-	ns

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = +25 °C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### TYPICAL PERFORMANCE – REVERSE DIODE (CONTINUED)

Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = 400 V, I <sub>S</sub> = 70 A, V <sub>GS</sub> = 0 V, R <sub>G,EXT</sub> = 5 Ω, di/dt = 2500 A/μs, T <sub>J</sub> = 150 °C	–	365	–	nC
t <sub>rr</sub>	Reverse Recovery Time		–	32	–	ns

### TYPICAL PERFORMANCE – DYNAMIC

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, f = 100 kHz	–	3340	–	pF
C <sub>OSS</sub>	Output Capacitance		–	230	–	
C <sub>rss</sub>	Reverse Transfer Capacitance		–	1.4	–	
C <sub>OSS(er)</sub>	Effective Output Capacitance, Energy Related	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	–	286	–	pF
C <sub>OSS(tr)</sub>	Effective Output Capacitance, Time Related		–	605	–	pF
E <sub>OSS</sub>	C <sub>OSS</sub> Stored Energy	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V	–	23	–	μJ
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 70 A, V <sub>GS</sub> = 0 V to 15 V	–	75	–	nC
Q <sub>GD</sub>	Gate-Drain Charge		–	13	–	
Q <sub>GS</sub>	Gate-Source Charge		–	22	–	
t <sub>d(on)</sub>	Turn-on Delay Time	Notes 4 and 5 V <sub>DS</sub> = 400 V, I <sub>D</sub> = 70 A, Gate Driver = 0 V, to +15 V, Turn-on R <sub>G,EXT</sub> = 1.5 Ω, Turn-off R <sub>G,EXT</sub> = 5 Ω, Inductive Load,	–	22	–	ns
t <sub>r</sub>	Rise Time		–	34	–	
t <sub>d(off)</sub>	Turn-off Delay Time		–	63	–	
t <sub>f</sub>	Fall Time		–	13	–	
E <sub>ON</sub>	Turn-on Energy Including R <sub>S</sub> Energy	FWD: same device with V <sub>GS</sub> = 0 V and R <sub>G</sub> = 5 Ω, RC snubber: R <sub>S</sub> = 5 Ω and C <sub>S</sub> = 560 pF, T <sub>J</sub> = 25 °C	–	440	–	μJ
E <sub>OFF</sub>	Turn-off Energy Including R <sub>S</sub> Energy		–	115	–	
E <sub>TOTAL</sub>	Total Switching Energy		–	555	–	
E <sub>RS_ON</sub>	Snubber R <sub>S</sub> Energy During Turn-on		–	9.2	–	
E <sub>RS_OFF</sub>	Snubber R <sub>S</sub> Energy During Turn-off		–	42	–	
t <sub>d(on)</sub>	Turn-on Delay Time	Notes 4 and 5 V <sub>DS</sub> = 400 V, I <sub>D</sub> = 70 A, Gate Driver = 0 V, to +15 V, Turn-on R <sub>G,EXT</sub> = 1.5 Ω, Turn-off R <sub>G,EXT</sub> = 5 Ω, Inductive Load,	–	21	–	ns
t <sub>r</sub>	Rise Time		–	38	–	
t <sub>d(off)</sub>	Turn-off Delay Time		–	68	–	
t <sub>f</sub>	Fall Time		–	13	–	
E <sub>ON</sub>	Turn-on Energy Including R <sub>S</sub> Energy	FWD: same device with V <sub>GS</sub> = 0 V and R <sub>G</sub> = 5 Ω, RC snubber: R <sub>S</sub> = 5 Ω and C <sub>S</sub> = 560 pF, T <sub>J</sub> = 150 °C	–	539	–	μJ
E <sub>OFF</sub>	Turn-off Energy Including R <sub>S</sub> Energy		–	129	–	
E <sub>TOTAL</sub>	Total Switching Energy		–	668	–	
E <sub>RS_ON</sub>	Snubber R <sub>S</sub> Energy During Turn-on		–	8.3	–	
E <sub>RS_OFF</sub>	Snubber R <sub>S</sub> Energy During Turn-off		–	42	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the switching test circuit in Figure 29.

5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

TYPICAL CHARACTERISTICS

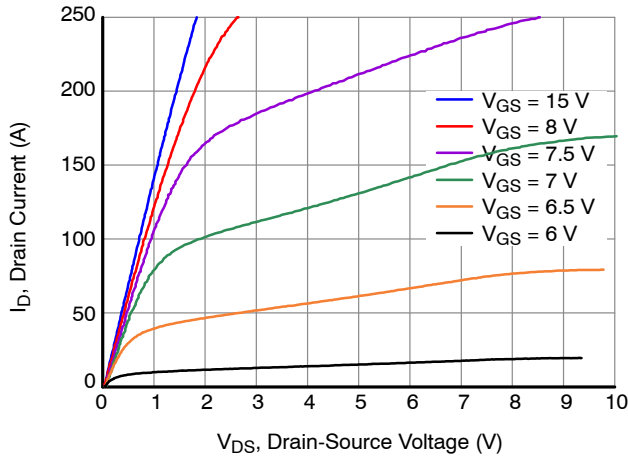


Figure 1. Typical Output Characteristics at  $T_J = -55\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

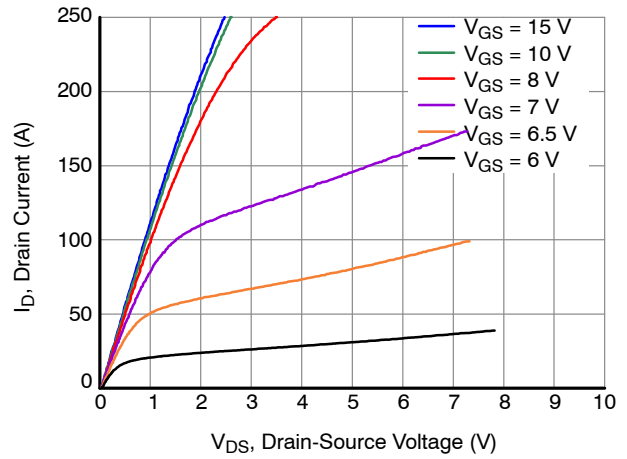


Figure 2. Typical Output Characteristics at  $T_J = 25\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

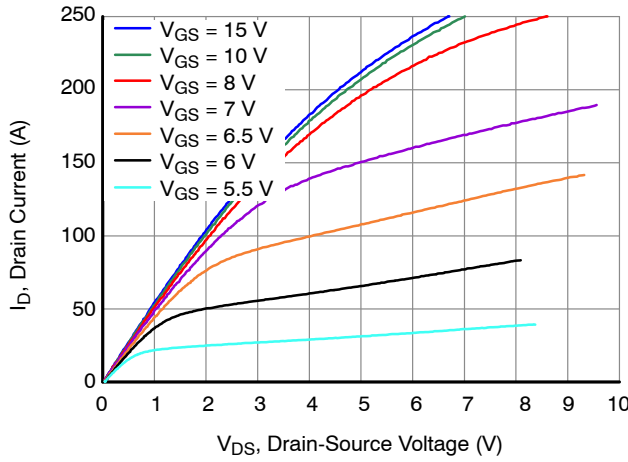


Figure 3. Typical Output Characteristics at  $T_J = 175\text{ }^\circ\text{C}$ ,  $t_p < 250\text{ }\mu\text{s}$

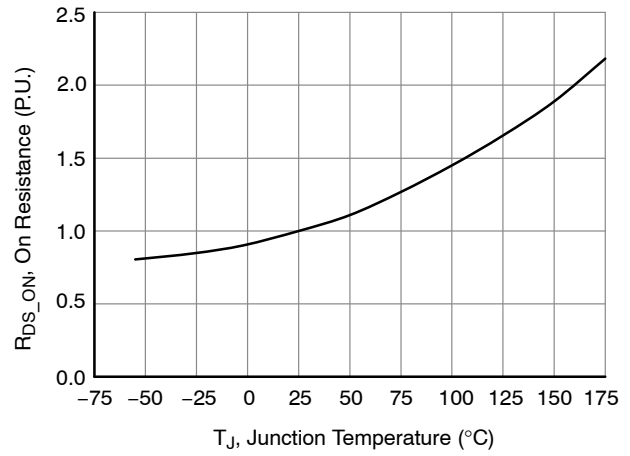


Figure 4. Normalized On-Resistance vs. Temperature at  $V_{GS} = 12\text{ V}$  and  $I_D = 70\text{ A}$

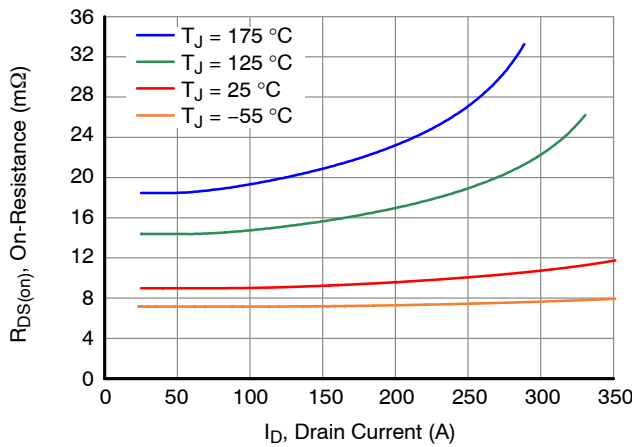


Figure 5. Typical Drain-Source On-Resistances at  $V_{GS} = 12\text{ V}$

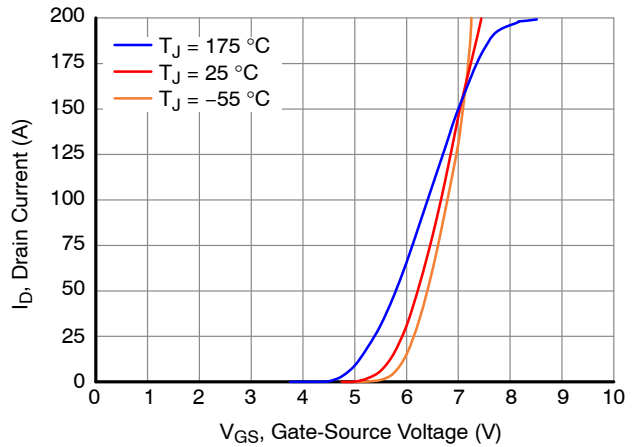


Figure 6. Typical Transfer Characteristics at  $V_{DS} = 5\text{ V}$

TYPICAL CHARACTERISTICS (continued)

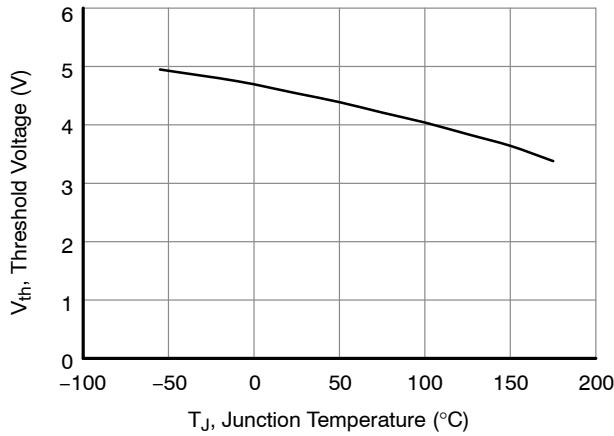


Figure 7. Threshold Voltage vs. Junction Temperature at  $V_{DS} = 5\text{ V}$  and  $I_D = 10\text{ mA}$

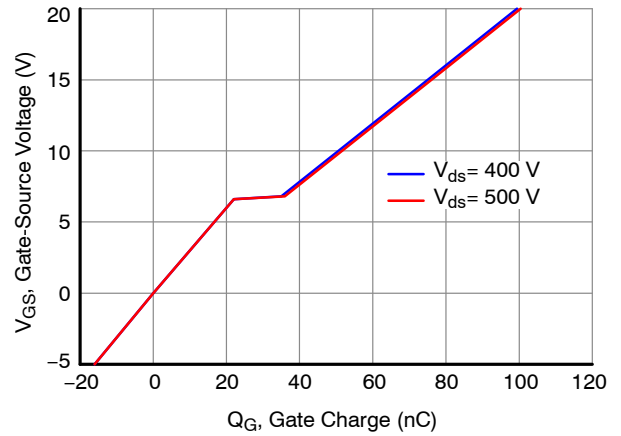


Figure 8. Typical Gate Charge at  $I_D = 70\text{ A}$

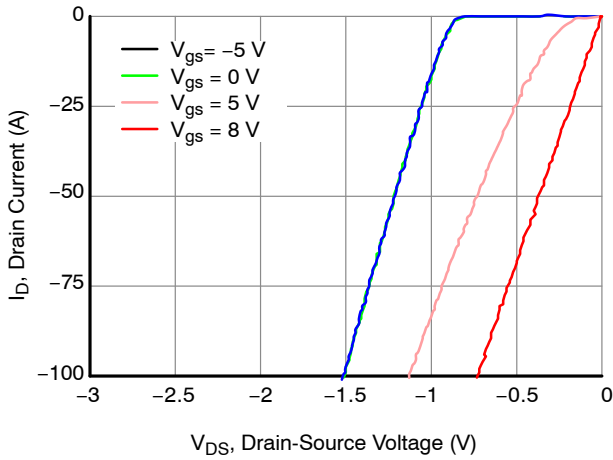


Figure 9. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = -55\text{ °C}$

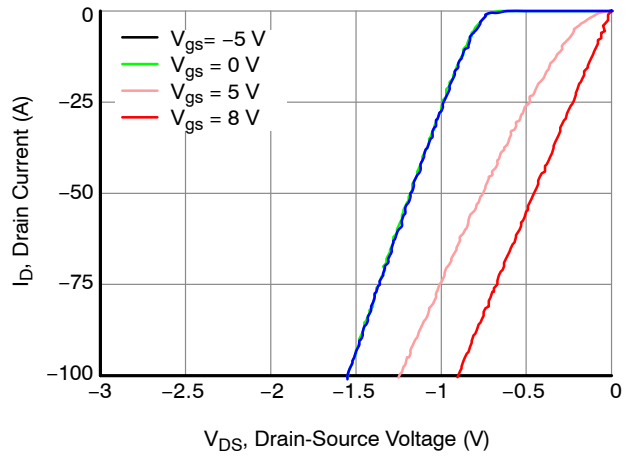


Figure 10. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 25\text{ °C}$

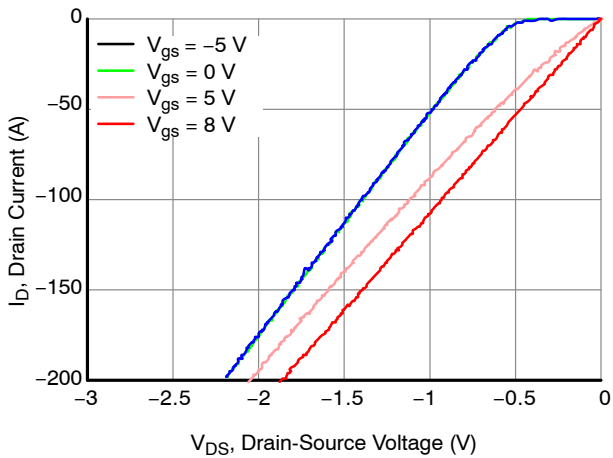


Figure 11. 3<sup>rd</sup> Quadrant Characteristics at  $T_J = 175\text{ °C}$

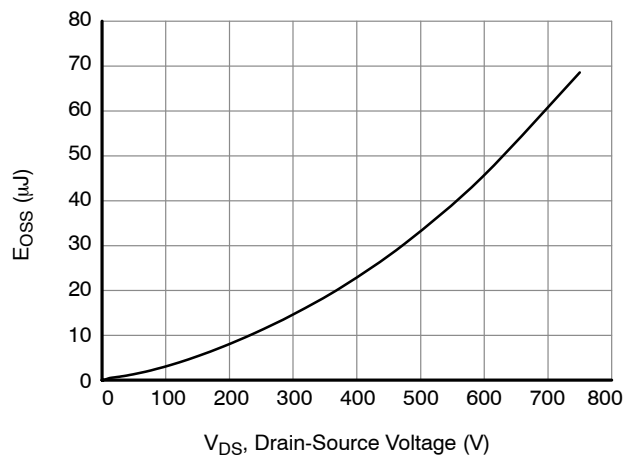
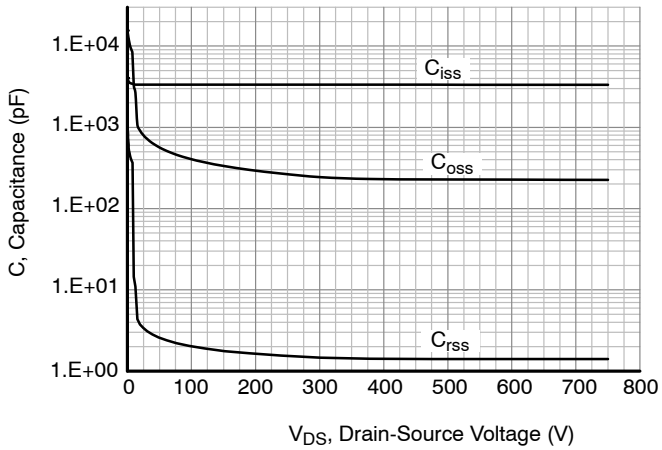


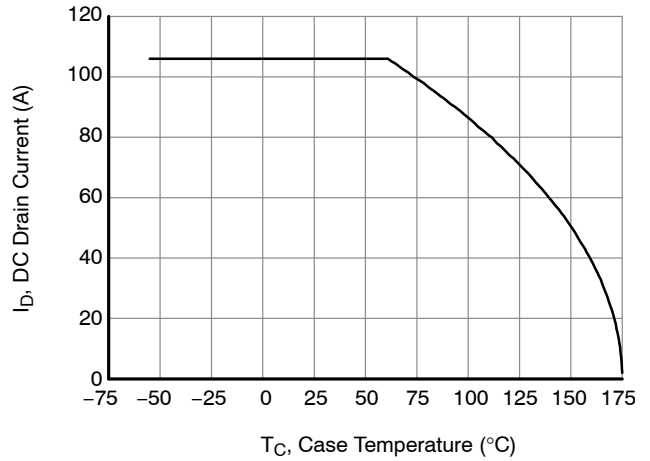
Figure 12. Typical Stored Energy in  $C_{OSS}$  at  $V_{GS} = 0\text{ V}$

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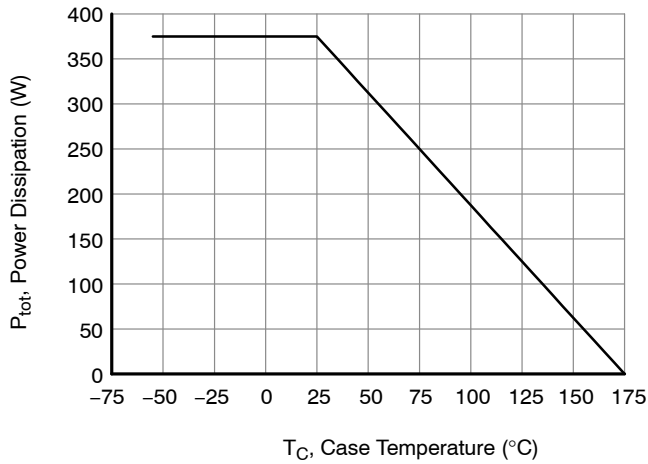
## TYPICAL CHARACTERISTICS (continued)



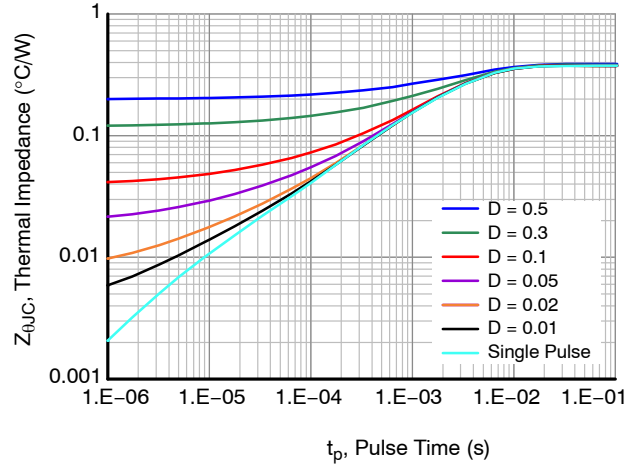
**Figure 13. Typical Capacitances at  $f = 100 \text{ kHz}$  and  $V_{GS} = 0 \text{ V}$**



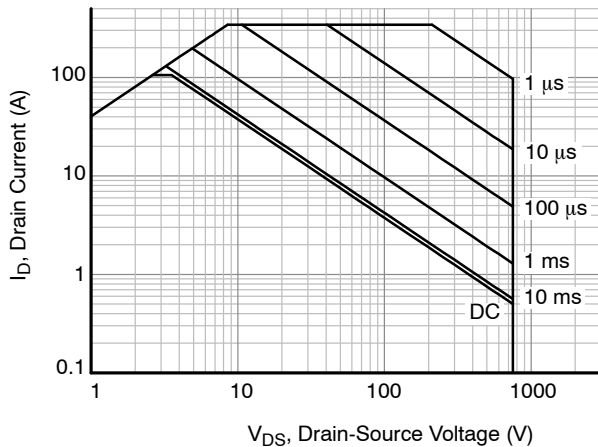
**Figure 14. DC Drain Current Derating**



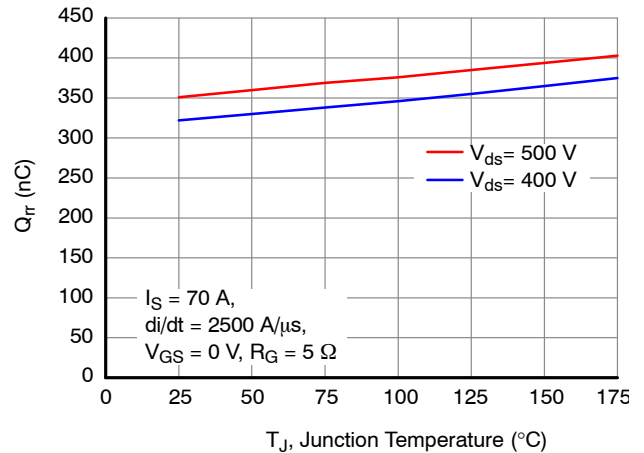
**Figure 15. Total Power Dissipation**



**Figure 16. Maximum Transient Thermal Impedance**



**Figure 17. Safe Operation Area at  $T_C = 25 \text{ }^\circ\text{C}$ ,  $D = 0$ , Parameter  $t_p$**



**Figure 18. Reverse Recovery Charge  $Q_{rr}$  vs. Junction Temperature**

TYPICAL CHARACTERISTICS (continued)

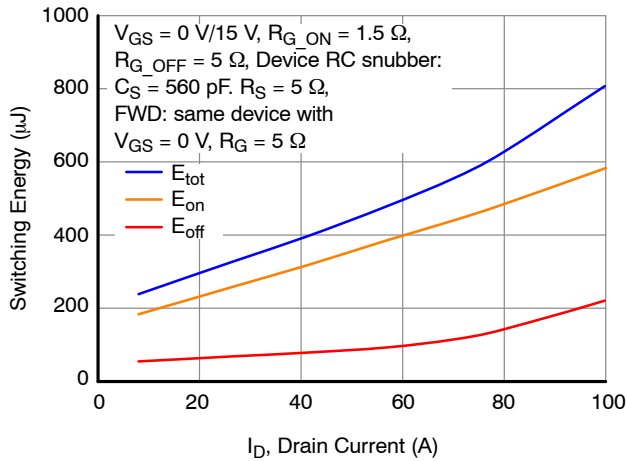


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at  $V_{DS} = 400\text{ V}$  and  $T_J = 25\text{ °C}$

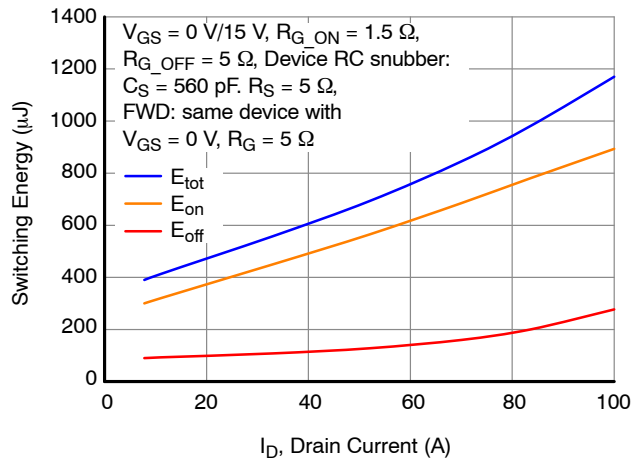


Figure 20. Clamped Inductive Switching Energy vs. Drain Current at  $V_{DS} = 500\text{ V}$ , and  $T_J = 25\text{ °C}$

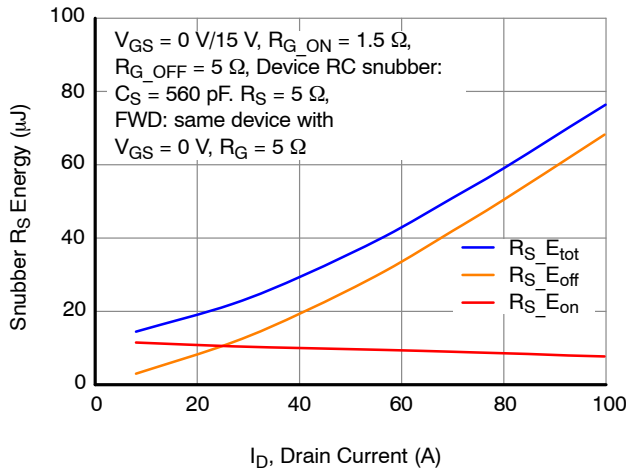


Figure 21. RC Snubber Energy Loss vs. Drain Current at  $V_{DS} = 400\text{ V}$  and  $T_J = 25\text{ °C}$

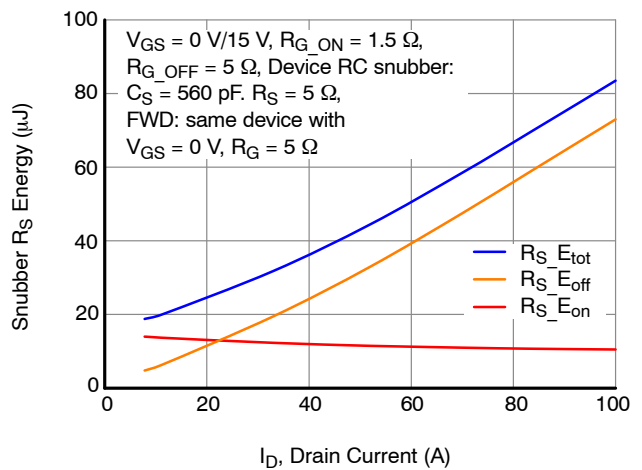


Figure 22. RC Snubber Energy Losses vs. Drain Current at  $V_{DS} = 500\text{ V}$  and  $T_J = 25\text{ °C}$

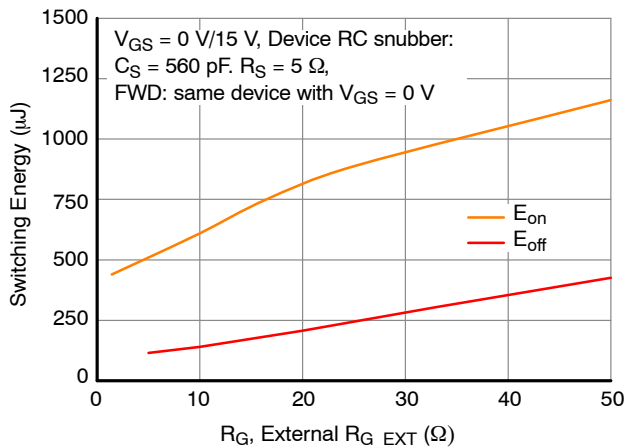


Figure 23. Clamped Inductive Switching Energies vs.  $R_{G\_EXT}$  at  $V_{DS} = 400\text{ V}$ ,  $I_D = 70\text{ A}$  and  $T_J = 25\text{ °C}$

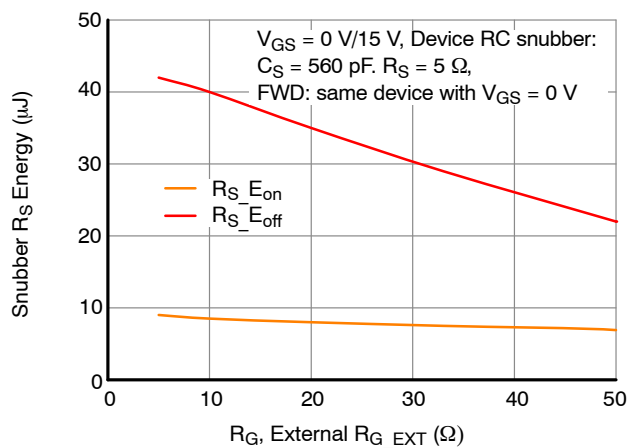


Figure 24. RC Snubber Energy Losses vs.  $R_{G\_EXT}$  at  $V_{DS} = 400\text{ V}$ ,  $I_D = 70\text{ A}$  and  $T_J = 25\text{ °C}$

TYPICAL CHARACTERISTICS (continued)

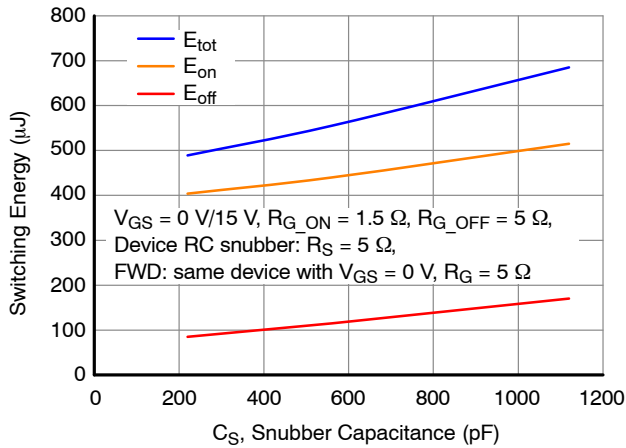


Figure 25. Clamped Inductive Switching Energies vs. Snubber Capacitance  $C_S$  at  $V_{DS} = 400$  V,  $I_D = 70$  A and  $T_J = 25$  °C

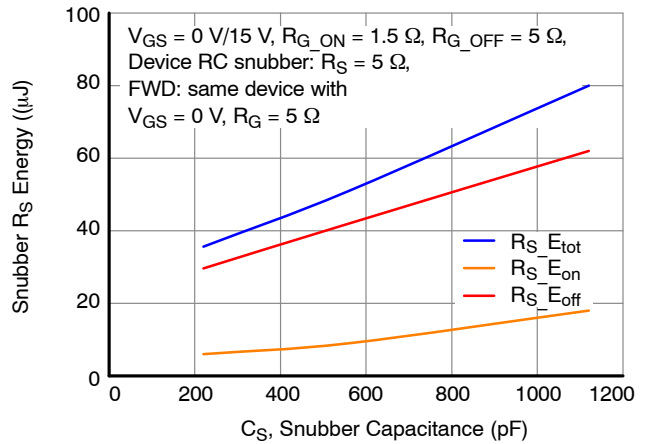


Figure 26. RC Snubber Energy Losses vs. Snubber Capacitance  $C_S$  at  $V_{DS} = 400$  V,  $I_D = 70$  A and  $T_J = 25$  °C

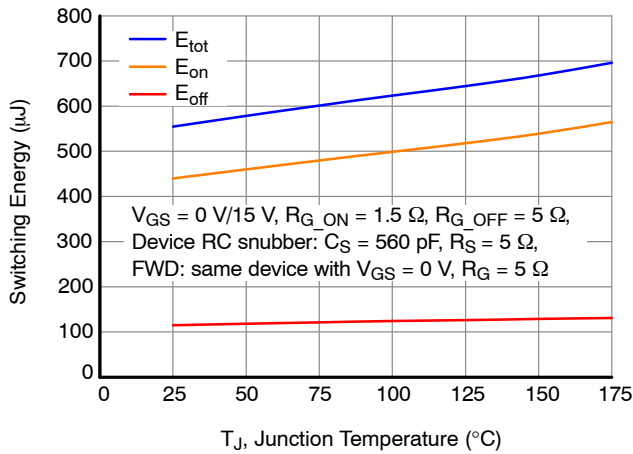


Figure 27. Clamped Inductive Switching Energy vs. Junction Temperature at  $V_{DS} = 400$  V and  $I_D = 70$  A

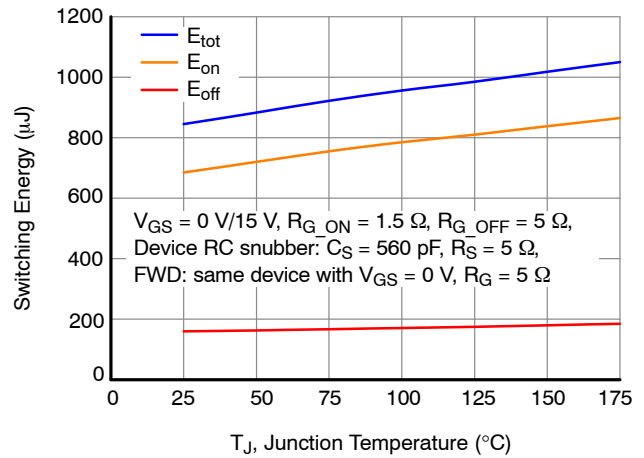


Figure 28. Clamped Inductive Switching Energy vs. Junction Temperature at  $V_{DS} = 500$  V,  $I_D = 70$  A

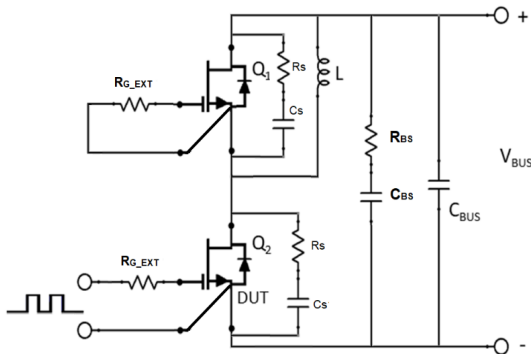


Figure 29. Schematic of the Half-Bridge Mode Switching Test Circuit. Note, a Bus RC Snubber ( $R_{BS} = 1$  Ω,  $C_{BS} = 100$  nF) is Used to Reduce the Power Loop High Frequency Oscillations.



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## APPLICATIONS INFORMATION

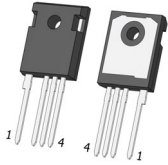
SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses.

The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.onsemi.com](http://www.onsemi.com).

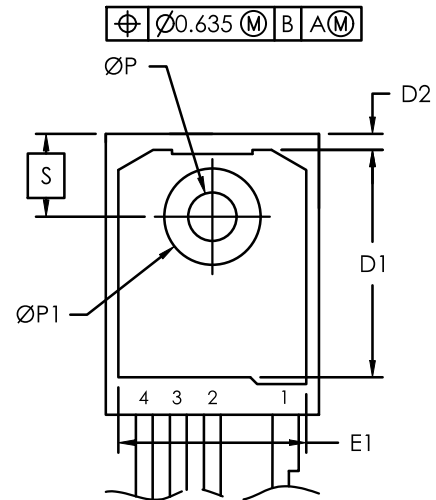
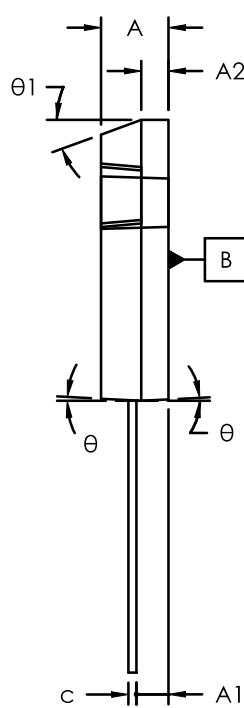
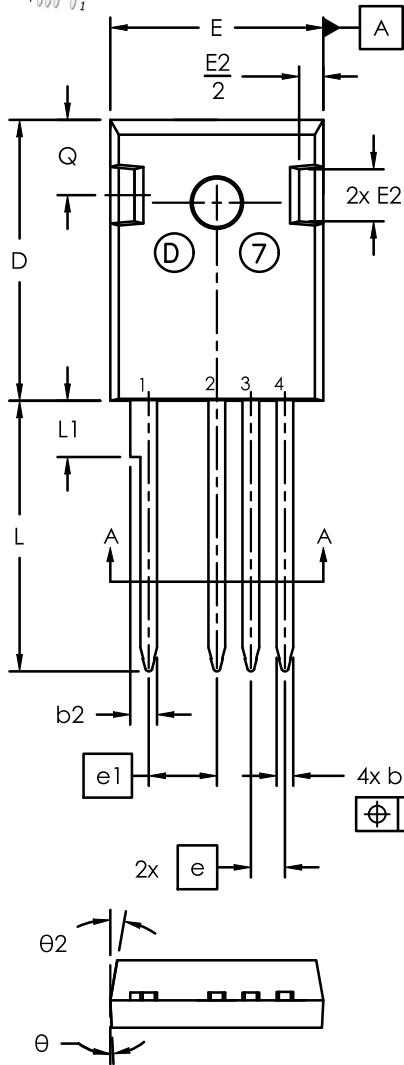
## ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UJ4SC075009K4S	UJ4SC075009K4S	TO-247-4L (Pb-Free, Halogen Free)	30 Units / Tube



TO247-4 15.90x20.96x5.03, 5.44P  
CASE 340AN  
ISSUE D

DATE 14 APR 2025



$\text{Ø} \text{Ø}0.254 \text{ (M) B A (M)}$

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
c	0.38	0.60	0.89
D	20.80	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	2.54 BSC		
e1	5.08 BSC		
E1	13.46	—	—
E2	3.43	3.89	5.20
L	19.81	20.17	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.17 BSC		
θ	3°		
θ1	20°		
θ2	10°		

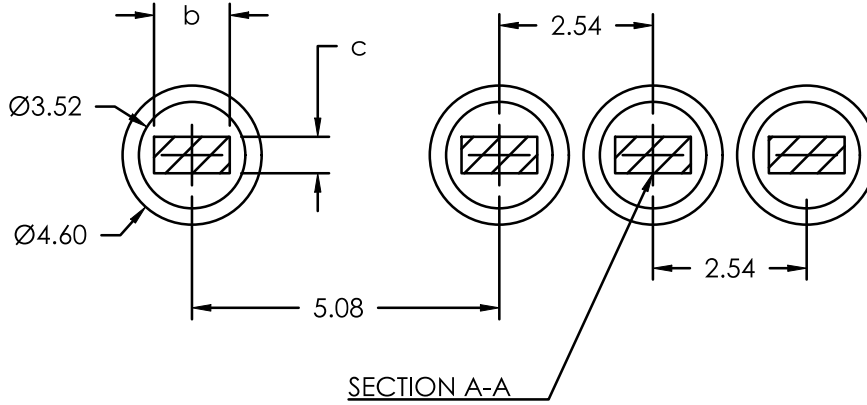
NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.
5. Through Hole diameter value = End Hole diameter
6. PCB Through Hole pattern as per IPC-2221/IPC-2222

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RECOMMENDED PCB THROUGH HOLE



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.  
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

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