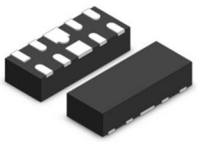
Transient Voltage Suppressors for ESD Protection

ULC0544P10

Description

The ULC0544P10 is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from over-voltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

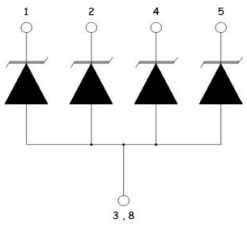
DFN2510P10



Feature

- 50 Watts Peak Pulse Power per Line (tp=8/20μs)
- Protects Four High Speed Lines
- Low Clamping Voltage
- RoHS Compliant
- IEC61000-4-2(ESD):±15kV (air discharge)
  ±10kV (contact discharge);
- IEC61000-4-4 (EFT) 40A (5/50 η s)
- IEC61000-4-5 (LIGHTING) 2A (8/20 μ s)

Functional Diagram



Applications

- USB 3.0 / USB 3.1 Interfaces
- HDMI 1.4 / HDMI 2.0 Interfaces
- Video Graphics Cards
- Notebooks, Desktops, and Servers
- Portable Instrumentation
- Industrial Controls
- Peripherals

Mechanical Data

- DFN2510P10 (2.5x1.0mm) Package
- Molding Compound Flammability Rating : UL 94V-O
- Weight 5.0 Millgrams (Approximate)
- Quantity Per Reel : 3,000pcs
- Reel Size : 7 inch
- Lead Finish : Lead Free
- Device Marking: UL4L

Mechanical Characteristics

Symbol	Parameter	Value	Units
Ppp	**Peak Pulse Power (tp=8/20μs waveform)**	50	Watts
T_J	**Operating Junction Temperature Range**	-55 to +150	ºC
T_{STG}	**Storage Temperature Range**	-55 to +150	ºC
T_L	**Soldering Temperature, T max = 10s**	260	ºC

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Electrical Characteristics (@ 25℃ Unless Otherwise Specified)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Reverse Working Voltage	V_{RWM}	--	--	--	5	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	6	--	--	V
Reverse Leakage Current	I_R	V_{RWM} =5V ; T=25°C	--	--	1	μA
Junction capacitance	C_J	I/O To GND;V_R =0V , f=1MHz ;	--	0.35	--	pF
Positive Clamping Voltage	V_C	I_{PP} =1A , T_P =8/20μS ;	--	--	14	V
		I_{PP} =2A , T_P =8/20μS ;	--	--	25	

Characteristic Curves

Fig1. Insertion Loss

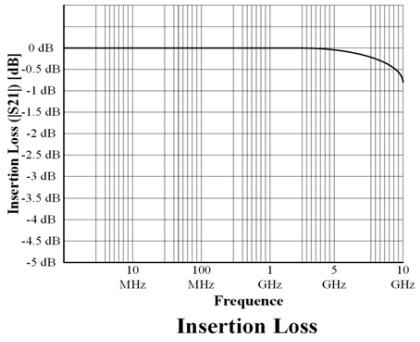


Fig2. ESD Pulse Waveform (according to IEC 61000-4-2)

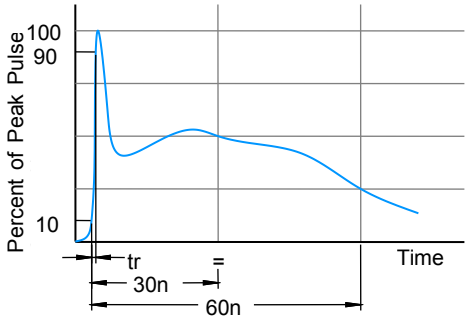


Fig3. ESD Clamping Volatge & Peak Pulse Curerent

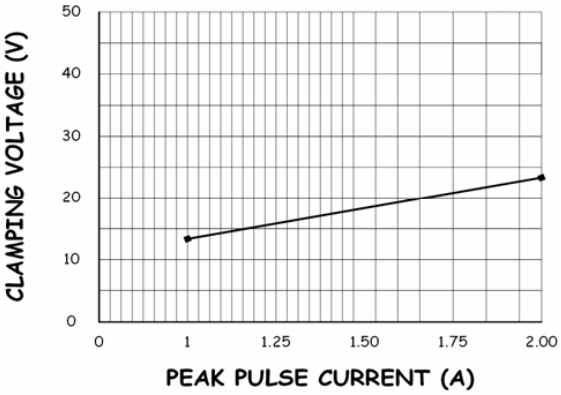
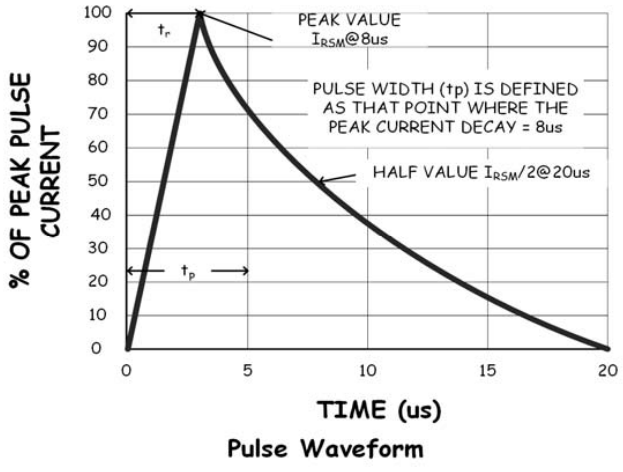


Fig4. Pulse Waveform



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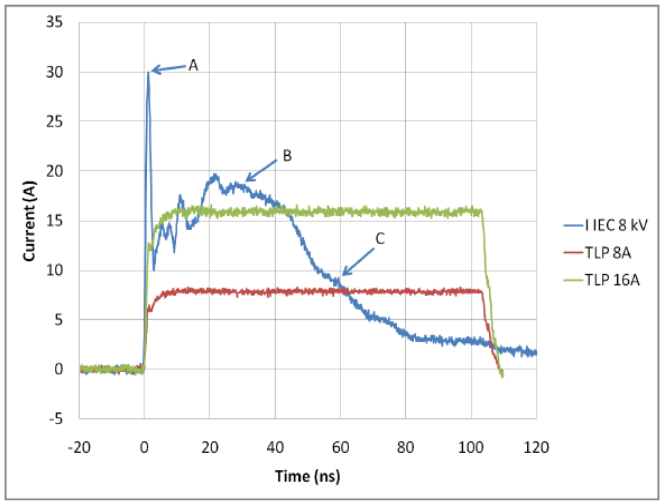
Transmission Line Pulse (TLP)

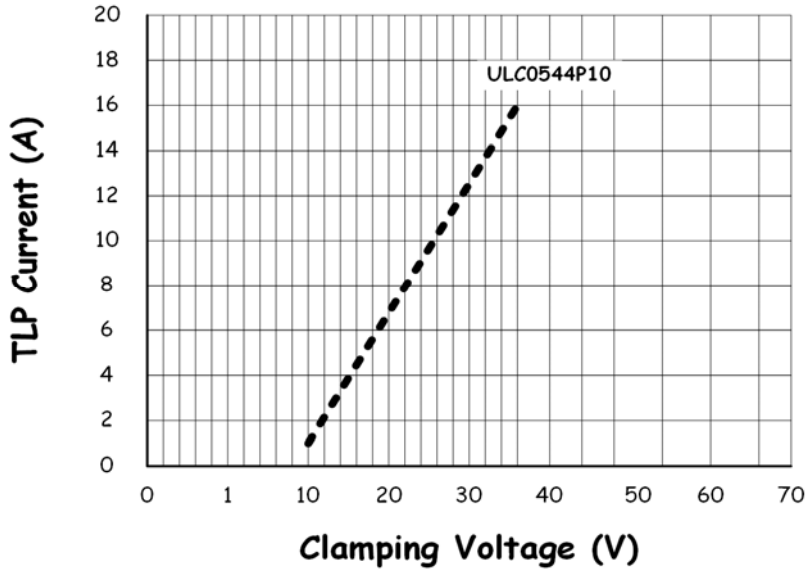
Transmission Line Pulse (TLP) is a measurement technique used in the Electrostatic Discharge (ESD) arena to characterize performance attributes of devices under ESD stresses. TLP is able to obtain current versus voltage (I−V) curves in which each data point is obtained with a 100 ns long pulse, with currents up to 40 A. TLP was first used in the ESD field to study human body model (HBM) in integrated circuits, but it is an equally valid tool in the field of system level ESD. The applicability of TLP to system level ESD is illustrated in Figure 1, which compares an 8 kV IEC 61000−4−2 current waveform with TLP current pulses of 8 and 16 A. The current levels and time duration for the pulses are similar and the initial rise time for the TLP pulse is comparable to the rise time of the IEC 61000−4−2's initial current spike. This application note will give a basic introduction to TLP measurements and explain the datasheet parameters extracted from TLP for Yeashin Technology's protection products.



Comparison of a Current Waveform of IEC 61000−4−2 with TLP Pulses at 8 and 16 A.

The IEC 61000−4−2 ESD waveforms is true to the Standard and is shown here as captured on an oscilloscope. The points A, B, and C show the points on the waveforms specified in IEC 61000−4−2.

TLP Characteristic



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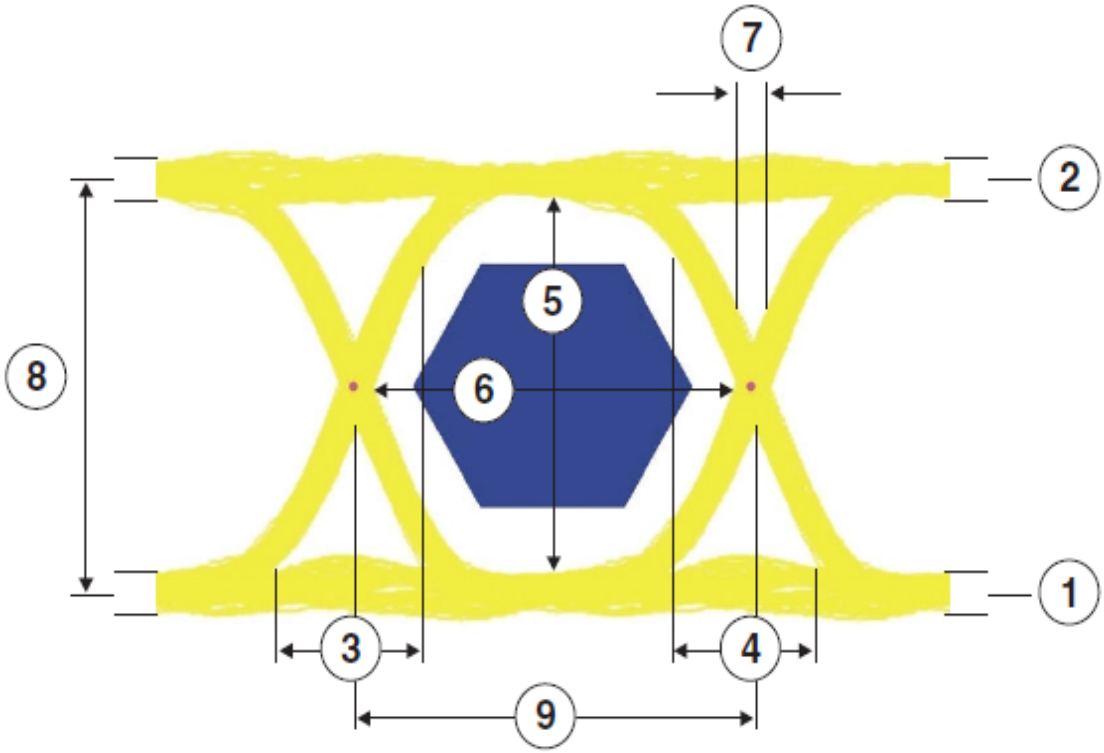
Eye Diagram

1 Zero Level : measure of the mean value of the logical 0.
2 One Level : measure of the mean value of the logical 1.
3 Rise Time : measure of the transition time of the data from the 10% level to the 90% level on the upward slope.
4 Fall Time : measure of the transition time of the data from the 90% level to the 10% level on the downward slope.
5 Eye Height : measure of the vertical opening. Determine eye closure due to noise.
6 Eye Width : measure of the horizontal opening. Determine influence of jitter on the eye opening.
7 Deterministic Jitter : deviation of a transition from its ideal time caused by reflections relative to other transitions.
8 Eye Amplitude : difference between the logic 0 level and the logic 1 level histogram mean value.
9 Bit Rate : inverse of the bit period.



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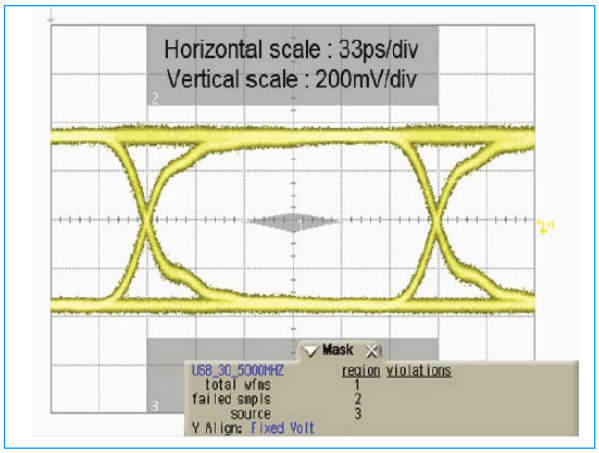
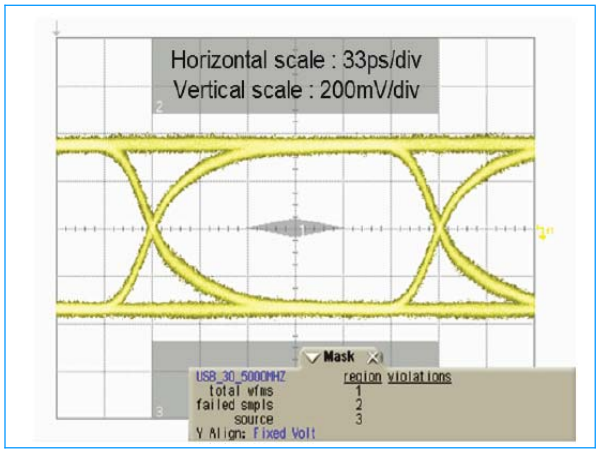
Eye Diagram at 5Gbps and 10Gbps

High Speed Test : 5Gbps

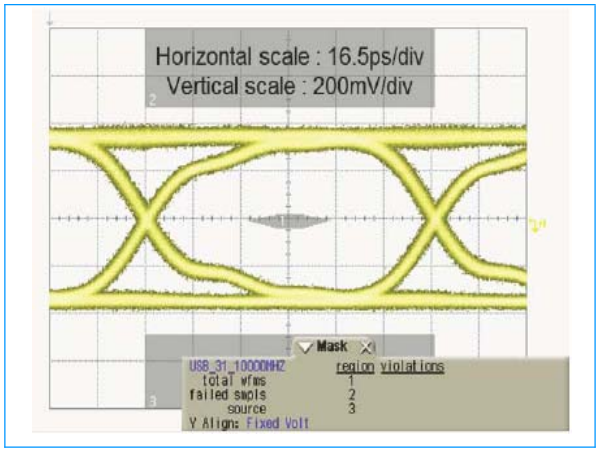


Eye Diagram -- USB 3.0 mask at 5.0Gbps.
Without Component

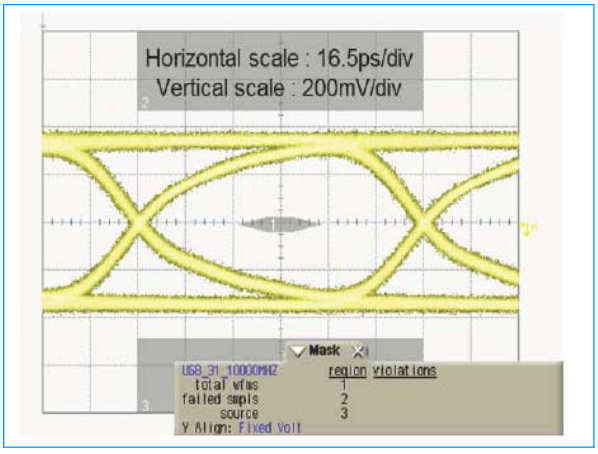


Eye Diagram -- USB 3.0 mask at 5.0Gbps.
With Component

High Speed Test : 10Gbps



Eye Diagram -- USB 3.1 mask at 10.0Gbps.
Without Component



Eye Diagram -- USB 3.1 mask at 10.0Gbps.
With Component

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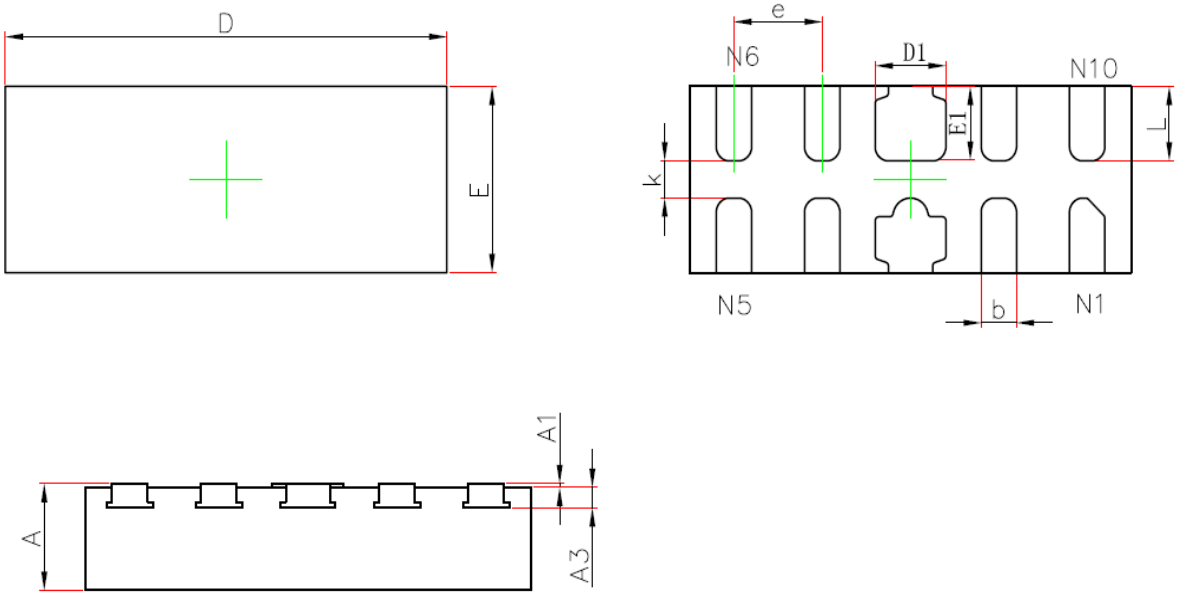
DFN2510P10 Package Outline & Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.110REF.		0.004REF.	
D	2.450	2.550	0.096	0.100
E	0.950	1.050	0.037	0.041
D1	0.350	0.450	0.014	0.018
E1	0.350	0.450	0.014	0.018
k	0.150MIN.		0.006MIN.	
b	0.150	0.250	0.006	0.010
e	0.500TYP.		0.020TYP.	
L	0.350	0.450	0.014	0.018

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LAYOUT DIAGRAM INFORMATION

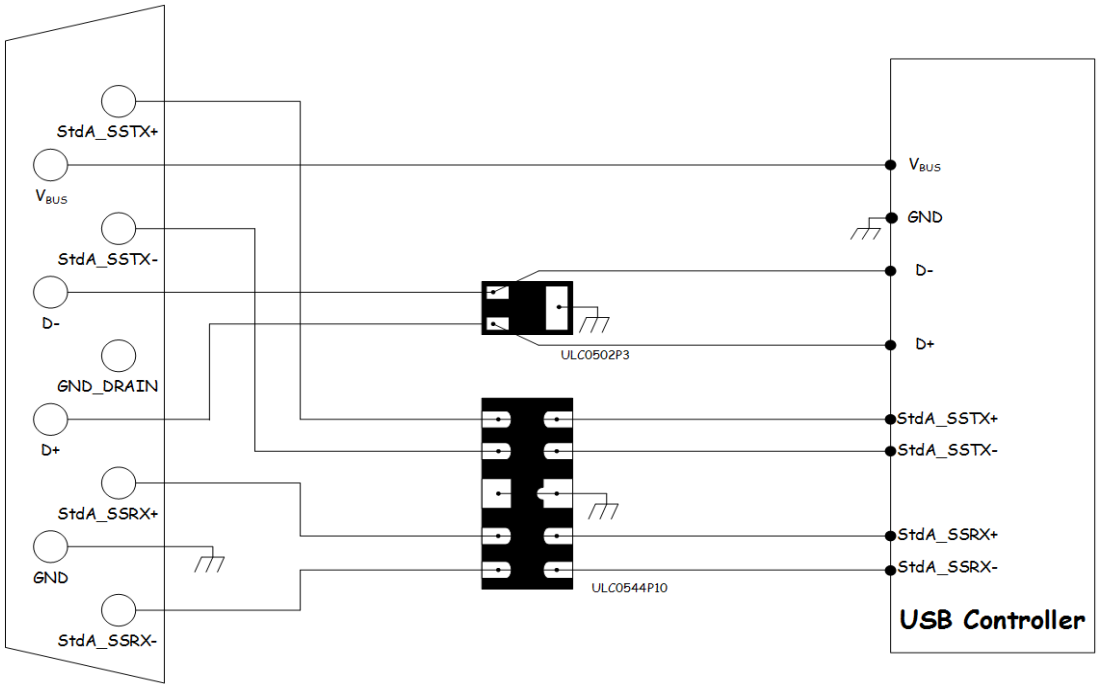

Figure 1. USB 3.1 Layout Diagram

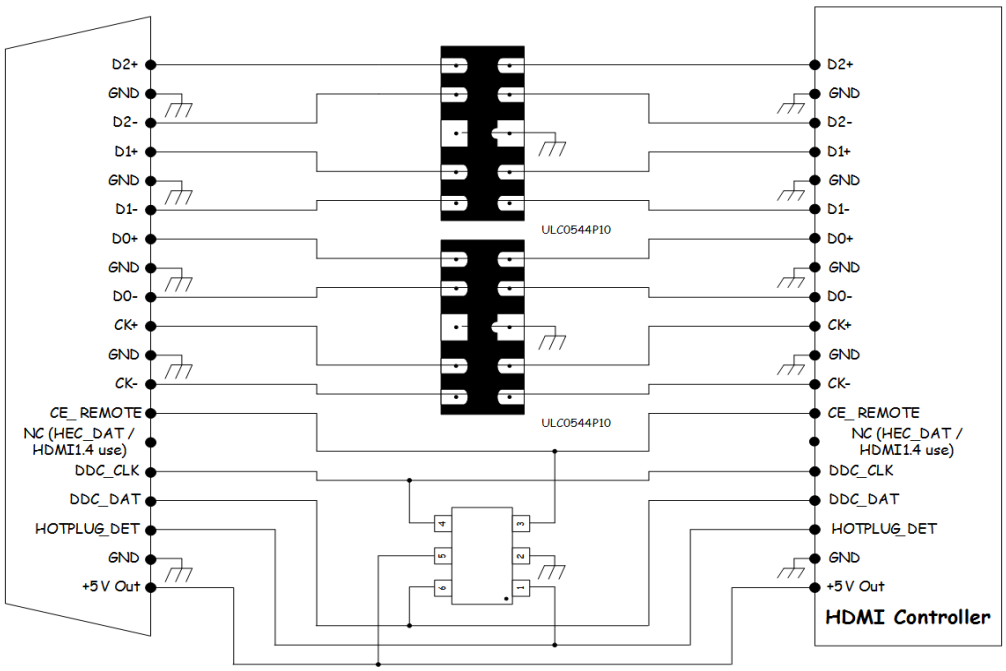

Figure 2. HDMI 2.0 Layout Diagram