



ULN2001LC

LINEAR INTEGRATED CIRCUIT

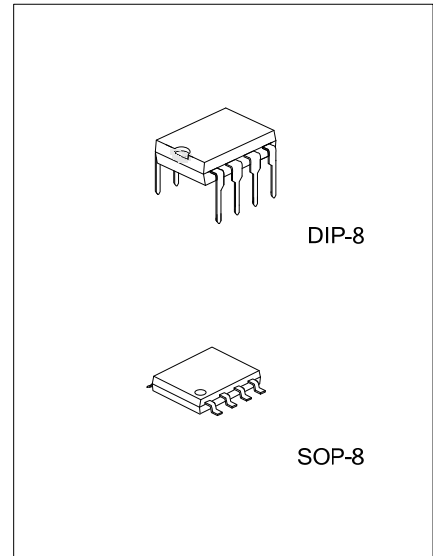
3CH DARLINGTON SINK DRIVER

DESCRIPTION

The UTC **ULN2001LC** is high-voltage, high-current darlington transistor arrays. Each consists of three NPN darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single darlington pair is 100mA. All units feature integral clamp diodes for switching inductive loads.

Applications include relay, hammer, lamp and display (LED) drivers.

The UTC **ULN2001LC** has a 2.7kΩ series base resistor for operation directly with TTL or 5V CMOS devices.



FEATURES

- * Output Current (Single Output): 100mA max
- * High Sustaining Voltage Output: 50V min
- * Inputs Compatible with Various Types of Logic
- * Output Clamp Diodes
- * Relay-Driver Applications

ORDERING INFORMATION

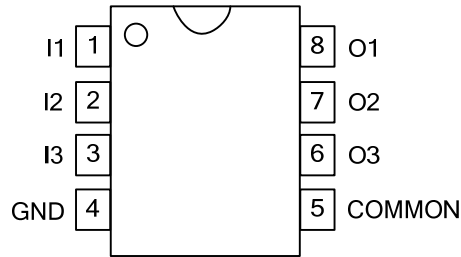
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULN2001LCL-D08-T	ULN2001LCG-D08-T	DIP-8	Tube
ULN2001LCL-S08-R	ULN2001LCG-S08-R	SOP-8	Tape Reel

<p>ULN2001LCG-D08-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

DIP-8	SOP-8
<p>8 7 6 5 → Date Code UTC □□□□ ULN2001LC □ □ □ → L: Lead Free □ □ → G: Halogen Free □ □ → Lot Code 1 2 3 4</p>	<p>8 7 6 5 → Date Code UTC □□□□ ULN2001LC □ □ □ → L: Lead Free □ □ → G: Halogen Free □ □ → Lot Code 1 2 3 4</p>

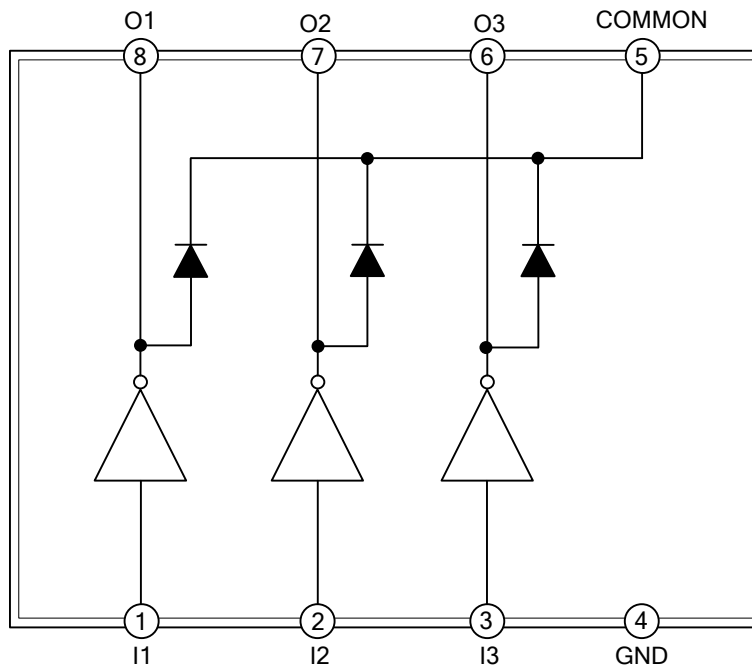
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	I1	1 Channel Input Pin
2	I2	2 Channel Input Pin
3	I3	3 Channel Input Pin
4	GND	Ground
5	COMMON	Clamp Diode
6	O3	3 Channel Output Pin
7	O2	2 Channel Output Pin
8	O1	1 Channel Output Pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage	V_{CE}	50	V
Clamp Diode Reverse Voltage	V_{COM}	50	V
Input Voltage	V_I	30	V
Peak Collector Current	I_{CP}	100	mA
Output Clamp Current	I_{OK}	100	mA
Power Dissipation	DIP-8	P_D	0.750
	SOP-8		0.625
Junction Temperature	T_J	+125	$^\circ\text{C}$
Storage Temperature	T_{STG}	-65 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$		0		50	V
Output Current	I_{OUT}	$T_A=+85^\circ\text{C}$			100	mA/ch
Input Voltage	V_{IN}		0		12	V
Input Voltage (Output On)	$V_{IN(ON)}$	$I_{OUT}=100\text{mA}$	2.8		12	V
Input Voltage (Output Off)	$V_{IN(OFF)}$		0		0.7	V
Clamp Diode Reverse Voltage	V_R				50	V
Clamp Diode Forward Current	I_F				70	mA

■ THERMAL DATA

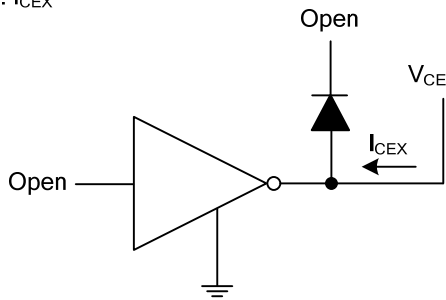
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-8	θ_{JA}	133
	SOP-8		160

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

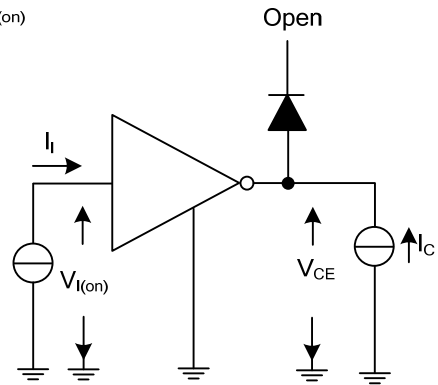
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage (Output On)	$V_{I(ON)}$	2	$V_{CE}=1.5\text{V}$	$I_C=20\text{mA}$	1.9	2.3	V
				$I_C=50\text{mA}$	2.0	2.4	V
				$I_C=80\text{mA}$	2.0	2.4	V
				$I_C=100\text{mA}$	2.1	2.5	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	$V_I=2.4\text{V}$ ($I_I>250\mu\text{A}$)	$I_C=20\text{mA}$	0.83		V
				$I_C=50\text{mA}$	0.92		V
				$I_C=80\text{mA}$	0.99		V
				$I_C=100\text{mA}$	1.10		V
Input Current	I_I	2	$I_C=60\text{mA}$	$V_I=12\text{V}$	6.3		mA
				$V_I=6\text{V}$	2.8		mA
				$V_I=4.5\text{V}$	1.97		mA
				$V_I=2.4\text{V}$	0.83		mA
Clamp Diode Forward Voltage	V_F	5	$I_F=70\text{mA}$		1.1	1.4	V
Output Leakage Current	I_{CEX}	1	$V_{CE}=50\text{V}, I_I=0$			50	μA
Collector-Emitter Voltage	V_{CE}	1	$V_{CE}=50\text{V}, I_I=0$	50			V
Clamp Diode Reverse Voltage	V_R	4	$V_R=50\text{V}$	50			V
Clamp Diode Reverse Current	I_R	4	$V_R=50\text{V}$			50	μA
Propagation Delay Time, Low- to High	t_{PLH}	6	$V_L=12\text{V}, R_L=120\Omega$		0.15	1	μs
Propagation Delay Time, High - to Low	t_{PHL}	6	$V_L=12\text{V}, R_L=120\Omega$		0.15	1	μs

TEST CIRCUIT

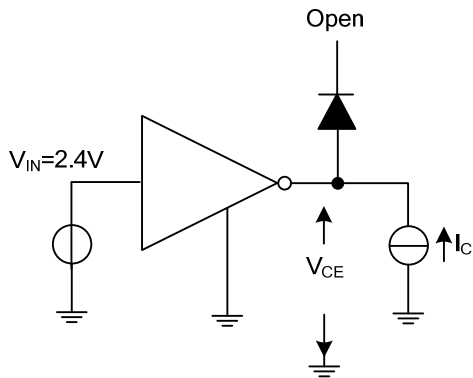
1. I_{CEX}



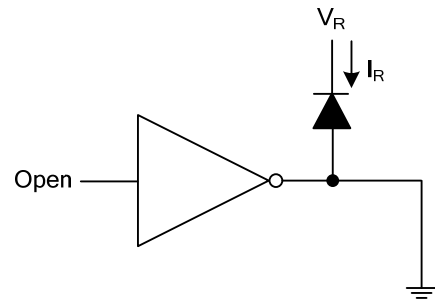
2. I_I & $V_{I(on)}$



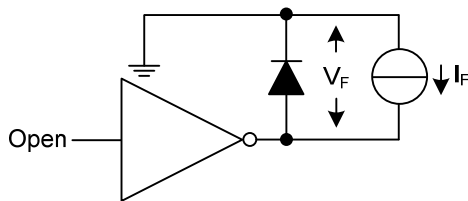
3. $V_{CE(sat)}$



4. I_R



5. V_F



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