# ULPMC10

# Microcontroller for Struix System-in-Package (SiP)

**ON Semiconductor®**

**QFN48 6x6**
**CASE 485AN**

1   48

## MARKING DIAGRAM

○

XXXXXXXX
AWLYYWWG

XXX = Specific Device Code
A    = Assembly Location
WL  = Wafer Lot
YY  = Year
WW = Work Week
G    = Pb−Free Package

## Introduction

ULPMC10 is an industry−leading 32−bit microprocessor built around an ARM® Cortex®−M3 core that is designed for capturing and processing biometric signals within medical devices. ULPMC10 is ideally suited to be integrated with custom designed proprietary application specific integrated circuit (ASICs) within the Struix System−in−Package (SiP) solution from ON Semiconductor. This complete energy efficient solution enables manufacturers to develop miniature, high performance, low power, precision−sensing medical applications.

ULPMC10 delivers outstanding computational performance and exceptional system response to events, while meeting the challenges of low dynamic and static power constraints. The processor is highly configurable, enabling a wide range of medical implementations from those requiring low duty−cycle operations to size−sensitive devices requiring a minimal semiconductor footprint.

ULPMC10 features built−in, advanced power management including system monitoring for fail−safe operation. This allows for a wide variety of battery voltages for efficiently powering the device without the need for external, active components. It encompasses a combination of charge pump based power conversion and regulation providing an optimal balance between power and execution speed.

A comprehensive and easy−to−use suite of development tools is available from IAR Systems including CMSIS based software interfaces.

## Key Features

### Powerful and Efficient Processing Architecture

- 32−bit ARM Cortex−M3 Processor
- 512 kB On−chip Flash for Program and User Data Storage
- 24 kB On−chip SRAM Memory
- Flexible DMA, 2 General−purpose Timers, CRC Calculator
- No External Voltage Required for Flash Write Operation

### Ultra Low−Power and Smart Power Management

- Less than 200 μA / MHz, up to 5 MHz Clock Speed
- Less than 400 μA / MHz, between 5 MHz and 40 MHz Clock Speed
- Flexible Input Voltage Range between 1.3 V; 3.6 V (3 V Nominal Supply Voltage)
- Ultra−low−current Sleep Mode with Real−time Clock Active (< 200 nA)
- On−chip Charge Pump for Effective Power Conversion and Powering of External, Devices such as Wireless Bluetooth® Low−energy

- Low−current Standby Mode with Real−time Clock Active, Register, and SRAM Retention (< 500 nA)
- Integrated Power Supplies Minimize Need for External Components, Only a Minimum of External Passives is Required

### Clock Management

- Built−in RTC with External Crystal
- On−chip RC Oscillator for Internal Clock Generation up to 40 MHz
- Integrated PLL (up to 20 MHz Output Signal) − Allow for RTC Crystal only Operation (no Additional Crystal Required)
- Divider Structure to Efficiently Clock any Portion of the Device

### Analog−to−Digital Conversion

- Single 12−bit ADC with 3 Multiplexed Inputs
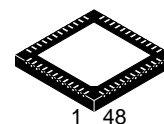- On−the−fly Data Rate Configurability

### Temperature Sensor

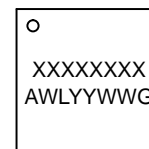- Built−in, Junction−based Temperature Sensor Covering 0°C up to 50°C

**July, 2015 − Rev. 4**

# ULPMC10

**Digital Interface**

- 24−pin DIO interface encompassing:
- PWM for external actuator or sensor control
- 2 SPI ports
- UART

- PCM
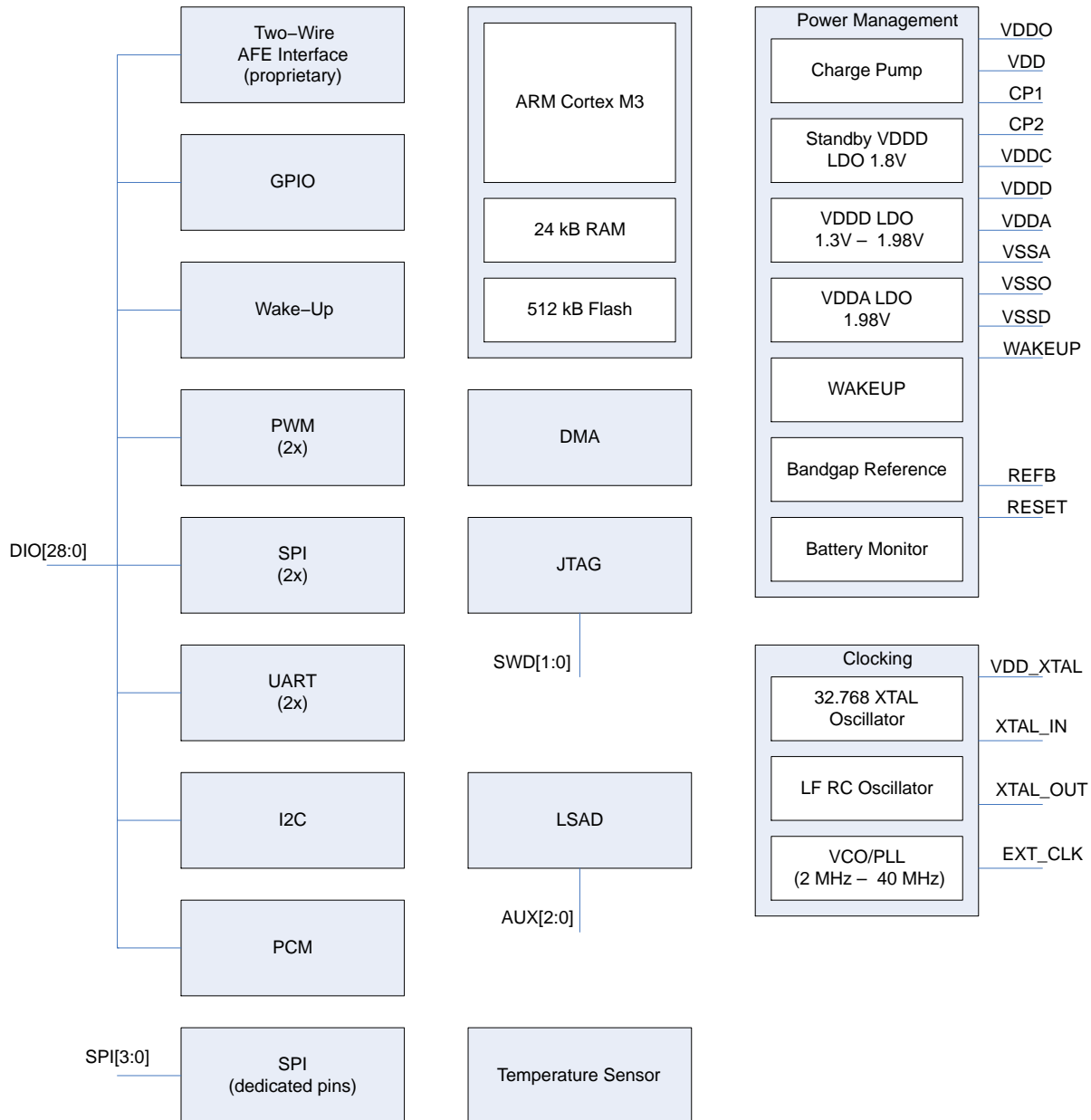- I$^2$C
- JTAG (2−wire)
- GPIO
- IRQ

## SYSTEM DIAGRAM



**Figure 1. ULPMC10 System Overview**

# ULPMC10

## ARCHITECTURE OVERVIEW

### Operating Modes

Five low−power operating modes are available:

- Run mode
    - Run_Fast mode – used during normal program execution; the entire device is fully operational in Run mode
    - Run_Slow mode – used for lower current consumption, with slower program execution
- Standby mode – used for ultra−low current consumption, with no program execution but RAM and register retention
- Sleep mode – used for ultra low current consumption, with no program execution
- Shutdown mode – used for ultra low current consumption, with no program execution

Each mode is designed to provide the lowest possible current consumption, while maintaining power to specific parts of the device.

### Run Mode

*Run_Fast Mode*

Run_Fast mode provides a low−power mode where the entire system is fully functional with a system clock up to 40 MHz. In Run_fast mode, the device enables the on−chip VDDD Digital Supply Regulator to provide power to the ARM Cortex−M3 processor. The processor is clocked from either an internal or an external clock source (via the PLL). The program can be executed from the internal flash or SRAM memory.

The application may also adjust the device clock frequency through the internal oscillator or through clock divisors to minimize power consumption. The Analog−to−Digital Converter (ADC) may be configured as required in run mode. Internal clock dividers provide all the necessary clocks to the peripherals.

While in Run mode, the application may switch into either Sleep mode, Standby mode, or Shutdown Mode.

*Run_Slow Mode*

Run_Slow mode is similar to Run_Fast mode except that the maximum system clock is 5 MHz.

### Standby Mode

*Deep Standby Mode*

Deep Standby mode provides a low−power mode where the digital system state is retained. In Deep Standby mode, the ARM Cortex−M3 processor execution is paused and the VDDD Digital Supply Regulator voltage is reduced. The contents of all the registers and SRAM are retained and the RTC stays enabled.

When in Deep Standby mode, the device may be switched into Run_Fast or Run_Slow mode by either the RTC alarm or by up to four external events (through the Wakeup controller).

*Fast Standby Mode*

Fast Standby mode is similar to Deep Standby mode, except that it operates at a higher current and allows for a faster startup time.

You can find more details on Fast Standby mode in the Hardware Reference for the ULPMC10 Microcontroller manual, available on request from your ON Semiconductor sales support representative.

### Sleep Mode

Sleep mode provides an ultra−low power mode where the system is waiting for a wakeup event. In sleep mode, the power supervisor automatically disables and powers down the digital and analog supply regulators and the internal oscillator. The RTC stays enabled.

When in sleep mode, the device may be switched into Run_Fast mode or Run_slow mode by either the RTC alarm or by up to four external events (through the Wakeup controller). After exiting Sleep mode, the system state is reset and execution starts from the beginning of the ROM program.

### Shutdown Mode

Shutdown mode is similar to Sleep mode except that the RTC is disabled. This is lowest power mode for ULPMC10.

### Power Supply

The device can powered from a single battery supply such as a 2032 lithium coin cell or any other battery with a voltage between 1.3 V and 3.6 V. The device supplies all required regulated voltages and references on−chip. This allows the device to operate directly from a single battery supply without the need for external regulators or switches.

### VDD

The main power supply input for the device is VDD. The supplied voltage to VDD is typically 3.3 V but VDD can be supplied with any voltage between 1.3 V and 3.6 V. The device will operate reliably across this entire power supply range. This flexibility allows for a wide range of battery types to be directly connected to the device. Note, for flash write VDD needs to be at least 1.8 V.

VDD is monitored by the built−in power supervisor.

### Regulators

All required voltages for normal device operation are generated on−chip.

### VDDD

The VDDD Digital Supply Regulator (VDDD) provides a nominal 1.3 V power supply for the digital domain on the chip (consisting of the ARM Cortex−M3 Processor, digital peripheral and memories, and on−chip flash) in case flash write access is not required and the system clock frequency is less than 5 MHz (Run_Slow Mode). If flash write access

is required or the system clock is greater than 5 MHz, VDDD provides a nominal 1.8 V voltage.

## VDDC

An on–chip charge pump can be applied for effective power conversion when applying VDD voltages larger than 2.6 V. In this case, the charge pump divides the VDD voltage to create a divided voltage VDDC of 1.3 V. The VDDC voltage can be used instead of the VDDD voltage to supply the ARM Cortex–M3 processor, digital peripheral and memories, including the on–chip flash. Note, this power scheme only applies to Run_Slow mode.

## VDDA

An on–chip regulator for the analog blocks creates a 2 V voltage (from the battery voltage VDD) for the A/D Converter, PLL and temperature sensor.

## VDDO

A dedicated pin sets the logic high voltage for the digital I/O pins. VDDO is typically connected to VDD or VDDD.

## Power Supervisor, Power – on Reset, and Brown–Out Protection

The device contains a dedicated hardware power supervisor for monitoring the supply voltages. The power supervisor ensures the device operates deterministically, and without any unexpected behavior during all supply conditions.

The power supervisor releases the internal Power–on Reset (POR) when the supply voltage on VDD exceeds the minimum threshold for proper operation. The release of POR enables the VDDD Digital Supply Regulator. The power supervisor continues to monitor VDD. If VDD drops below the minimum threshold for proper operation the device is reset.

No external circuitry is required for proper device startup. All required start–up delays and reset thresholds are generated on–chip.

In Run_Fast or Run_Slow mode, the power supervisor continually monitors VDDD. If VDDD drops below the minimum threshold for proper operation the device is reset.

The power supervisor is automatically disabled in standby, sleep and shutdown modes to save power.

## System Wakeup

Wakeup occurs when the device is switched from standby mode, sleep mode or shutdown mode into any of the run modes. This can be accomplished through one of the wakeup mechanisms. The wakeup controller allows for up to four external events to wake up the system. One dedicated wakeup pin will wake up the system when a Low–to–High transition is detected. Additionally, three DIO pins can be configured for wakeup as well (two DIO pins will trigger a wakeup through a Low–to–High transition, one DIO pin will trigger a wakeup through a High–to–Low transition). The RTC Alarm can also be configured to wake up the system at a predetermined time.

## Clocking

The device contains several clock generators and clock I/O capability. After Power–on Reset, the device selects the internal oscillator as the system clock source. The default clock frequency at POR is 10.24 MHz. After boot, the application may select another frequency or switch to another clock source. The device may select the real–time crystal oscillator (32.768 kHz) as the clock source, when low operating frequencies are required to save power.

## Internal Oscillator

The device contains a reconfigurable, factory–calibrated internal oscillator. The calibration settings are stored in the on–chip flash. Settings are available for all integer frequencies in the normal operating range (1 MHz to 40 MHz). Finer calibration is possible.

The default setting after Power–on Reset is 10.24 MHz. The application can switch to any operating frequency after entering any of the run modes.

## Phase–Locked Loop

The device contains a phase locked loop (PLL). The phase–locked loop is designed to provide ample flexibility to support various use cases where internal or external reference clocks are used to derive the system clock. At start–up the PLL will be free–running and an adequate configuration must be applied before the PLL will function properly. This configuration includes setting a reference clock and an output clock. The PLL must be recalibrated every time the reference clock stops or the PLL unlocks.

## Real–Time Clock

The device contains an ultra low–power real–time clock (RTC). The RTC includes a real–time crystal oscillator, read–write RTC counters, and a configurable alarm. The real–time crystal oscillator utilizes a 32.768 kHz external crystal.

The RTC is powered directly from VDD. This allows the RTC to continue to run when the VDDD Digital Supply Regulator voltage is reduced in standby mode or disabled in sleep or shutdown modes and thus the system date and time information are always maintained. The RTC is reset after the initial Power–on Reset but remains operational through a digital reset (watchdog) and operating mode switching.

The alarm function can be configured to wake up the system from standby mode or sleep mode at a pre–determined time. The alarm will also generate an interrupt to the ARM Cortex–M3 processor.

## Clock Divisors

On–chip clock divisors and prescalers are available to provide selectable frequencies to the ARM Cortex–M3 processor, sensor interface, peripherals and external interfaces. These divided clocks are derived from the root clock source and may be configured independently. This adjustability allows the optimum clock frequency to be selected for each system component.

## ADC

One 12−bit Analog−to−Digital Converter (ADC) with three external, configurable inputs is available. The ADC operates rail−to−rail from 0 V to VDDA (2.0 V) using an internal precision bandgap voltage reference. Two's complement output samples are provided to the ARM Cortex−M3 processor and synchronized to an ADC interrupt. The DMA may also be used to transfer samples directly from the ADC to SRAM.

## Temperature Sensor

The device contains a built−in temperature sensor. The temperature sensor works by generating a differential voltage that varies linearly with temperature. The voltage is routed into the ADC resulting in a single−ended output voltage measurable by the ADC.

The temperature sensor is calibrated during factory production by ON Semiconductor. The calibration value is stored in the flash. The device junction temperature may be determined based on the calibration factor and converted ADC output value.

## ARM Cortex−M3 Processor

The ARM Cortex−M3 processor is a 32−bit RISC controller specifically designed to meet the needs of advanced, high−performance, low−power applications. The ARM Cortex−M3 processor provides outstanding computational performance and exceptional system response to interrupts while providing small core footprint, industry leading code density enabling smaller memories, reduced pin count and low power consumption.

The ULPMC10 implementation of the ARM Cortex−M3 processor contains all necessary peripherals and bus systems to provide a complete device optimized for battery powered sensor interface applications.

## Memories

### Flash Memory

512 kB flash is available for storage of application code and data. Flash memory can be written one or more words at a time. Each page must be erased between writes to a flash word. The flash memory can be erased as a set all at once or in individual 2 kB pages. An additional reserved block of flash memory is used to store factory calibration information provided by ON Semiconductor. This block cannot be written by the application. The ARM Cortex−M3 processor executes application code directly from flash with zero wait states when the system clock is lower than 20 MHz. Above 20 MHz wait states are inserted. To avoid wait states the application developer may choose to use the on−chip RAM cache.

### SRAM Memory

24 kB of low−power SRAM is available for storage of intermediate data as well as application code. A block of SRAM can be utilized for caching to avoid wait states at high clock frequencies.

## ROM

An on−chip ROM includes boot functionality as well as firmware routines supporting writing to flash in an application.

## External Interrupt Controller

Two configurable external interrupt sources may be connected to any two DIO pins on the device. This is in addition to the four possible interrupts for the wakeup controller. Each interrupt may be individually configured for positive edge triggering, negative edge triggering, high level triggering, or low level triggering.

## DMA

A flexible DMA unit supports low overhead data exchange between system blocks. Memory−to−Peripheral, Peripheral−to−Memory, and Memory−to−Memory modes are available. Four simultaneous DMA channels can be established with configurable sources and sinks.

The DMA can be used with the UART, SPI, I$^2$C, and PCM interfaces, as well as the ADC.

The DMA operates in the background allowing the ARM Cortex−M3 processor to execute other applications or to reduce its operating frequency to conserve power.

## General−Purpose Timers

The device contains two general−purpose timers. Each timer features a 12−bit countdown mode, an external interrupt to the ARM Cortex−M3 processor, a dedicated prescaler, and the ability to poll the counter value. These four general−purpose timers are in addition to the 24−bit SYSTICK timer included as part of the ARM Cortex−M3 processor.

## CRC Engine

A 16−bit hardware CRC engine is available. The CRC engine may be used to ensure data integrity of application code and data. The CRC engine's input port and output port are directly accessible from the ARM Cortex−M3 processor. The starting vector may be set to any value. Subsequently, data words of multiple bit lengths can be added to the CRC. The 16−bit CRC−CCITT polynomial is used.

## Watchdog Timer

The device contains a digital watchdog timer. The watchdog timer is intended to prevent an indefinite system hang when an application error occurs. The application must periodically refresh the watchdog counter during operation. If a watchdog timeout occurs an initial alert interrupt is generated. If a subsequent watchdog timeout occurs, a system reset is generated. The initial alert may be used to gracefully shut down the system.

**IP Protection**

The device contains an optional lock mechanism to prevent access to Flash, memory and registers via the JTAG port. Note, if this feature is enabled the application must implement a "backdoor" in software to regain access to the device. Otherwise, the lock mechanism is irreversible.

**Digital I/O (DIO) Interface**

All the interfaces available in ULMPC10 for communications with external devices don't have dedicated pins. It is necessary to configure the DIO pads (Digital Input/Outputs) to be able to use them. The only exception is the JTAG interface which has dedicated pads as well as a dedicated SPI port.

By default, all the DIOs are configured as input pins.

In standby, sleep and shutdown modes the DIO configuration is kept if not explicitly disabled by software.

**Dual UART**

Two general–purpose UART interfaces are available. The UARTs support the standard RS232 protocol and baud rates at the VDDD voltage level. The UART format is fixed at one start bit, eight data bits, and one stop bit. The baud rate is configurable over a wide range of baud rates up to 250 kbaud using a 1 MHz source clock.

The UART interfaces may be used either directly from the ARM Cortex–M3 processor or through the DMA Controller.

**Dual SPI**

Two SPI interfaces (beyond a dedicated SPI port that is not brought out to pins on the sample package) are available supporting both master and slave operation. Each interface provides a clock, chip select, serial data in, and serial data out connection. The SPI interfaces can be used to interface with external devices such as non–volatile memories, displays, and wireless transceivers. The SPI interfaces can

be used either directly from the ARM Cortex–M3 processor or through the DMA Controller.

**I$^2$C**

The I$^2$C interface supports both master and slave operation. The interface operates at normal speed (100 kbits/sec) and high speed (400 kbit/sec). On–chip pull–up resistors are available on the SDA and SCL pins.

The I$^2$C interface can be used either directly from the ARM Cortex–M3 processor or through the DMA Controller. The I$^2$C slave address is programmable by the application.

**PCM**

The pulse–code modulation (PCM) interface provides a data connection between the device and external devices such as Bluetooth or audio processors. The PCM interface can operate both in master and slave mode. The master device of a PCM transfer generates the frame signal.

The PCM interface can be used either directly from the ARM Cortex–M3 processor or through the DMA controller. Two DMA channels are used with the PCM interface – one for RX, and one for TX.

The PCM interface supports a wide variety of interface protocols by reconfiguring the frame type and width, word size and clock polarities. The PCM interface supports the I2S data format directly for connecting to an I2S compatible audio device. Audio data can be streamed to and from the audio device over the PCM interface in I2S mode.

**GPIO**

Any DIO pin can be configured as GPIO input or output.

**Pulse Width Modulators (PWM)**

Two, independent pulse width modulators are available on the device. These can be used to drive external actuators or sensors.

# ULPMC10

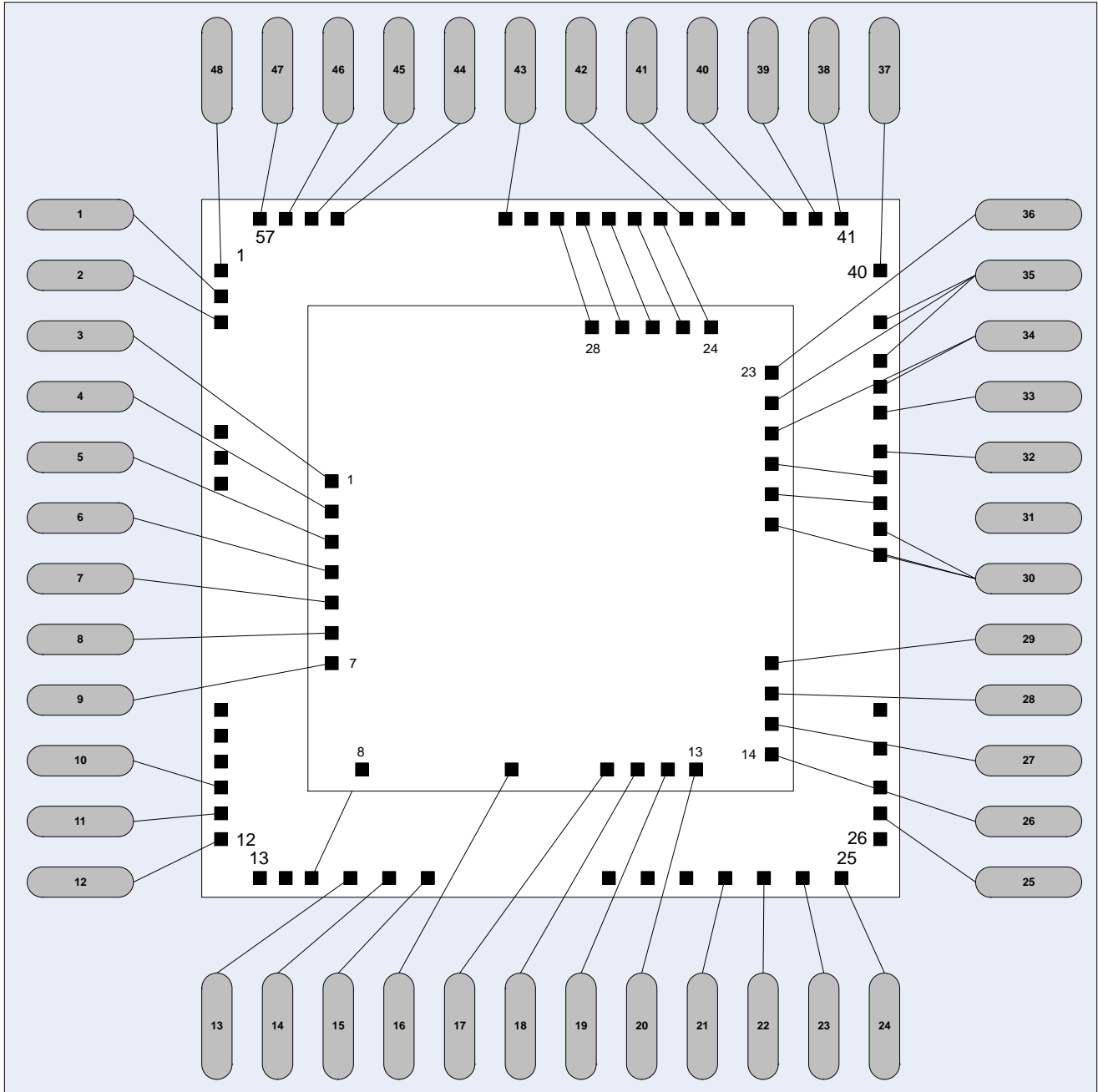**ULPMC10 QFN48 Example Production Package with Stacked Custom ASIC**



Figure 2. ULPMC10 QFN48 Example Production Package Overview with Stacked Custom ASIC

# ULPMC10

## ULPMC10 QFN48 Example Production Package Pin with Custom ASIC Overview

### Table 1. PIN OUT

| Pin# | Pad Name | Description | Domain | I/O | POR Direction | A/D | PU/PD |
|------|----------|-------------|--------|-----|---------------|-----|-------|
| 1 | DIO1 | Digital Input Output | VDDO | I/O | I | D | PU |
| 2 | DIO2 | Digital Input Output | VDDO | I/O | I | D | PU |
| 3 | CUSTOM | – | | – | – | – | – |
| 4 | CUSTOM | – | | – | – | – | – |
| 5 | CUSTOM | – | | – | – | – | – |
| 6 | CUSTOM | – | | – | – | – | – |
| 7 | CUSTOM | – | | – | – | – | – |
| 8 | CUSTOM | – | | – | – | – | – |
| 9 | CUSTOM | – | | – | – | – | – |
| 10 | DIO3 | Digital Input Output | VDDO | I/O | I | D | PU |
| 11 | DIO4 | Digital Input Output | VDDO | I/O | I | D | PU |
| 12 | DIO5 | Digital Input Output | VDDO | I/O | I | D | PU |
| 13 | AUX0_DIO27 | Digital Input Output configuration LSAD channel 0 configuration | VDD | I/O AI | I | D A | PU |
| 14 | AUX1_DIO28 | Digital Input Output configuration LSAD channel 1 configuration | VDD | I/O AI | I | D A | PU |
| 15 | AUX2 | LSAD channel 2 configuration | VDD | AI | I | A | |
| 16 | CUSTOM | – | | – | – | – | – |
| 17 | CUSTOM | – | | – | – | – | – |
| 18 | CUSTOM | – | | – | – | – | – |
| 19 | CUSTOM | – | | – | – | – | – |
| 20 | CUSTOM | – | | – | – | – | – |
| 21 | VDDA | Analog supply | VDD | | | A | |
| 22 | VSSA | Analog ground | VDD | | | P | |
| 23 | VDDD | Digital core supply | VDD | | | A | |
| 24 | VDD | Power supply 1 | VDD | | | P | |
| 25 | VDDC | Power supply 2 / CP output | VDD | | | A | |
| 26 | CUSTOM | – | | – | – | – | – |
| 27 | CUSTOM | – | | – | – | – | – |
| 28 | CUSTOM | – | | – | – | – | – |
| 29 | CUSTOM | – | | – | – | – | – |
| 30 | RESET | External reset signal | VDD | I | I | D | PD |
| 31 | DIO6 | Digital Input Output | VDDO | I/O | I | D | PU |
| 32 | DIO7 | Digital Input Output | VDDO | I/O | I | D | PU |
| 33 | VDDO | IO supply | VDDO | | | A | |
| 34 | RESERVED | Tie to VSS | – | – | – | – | – |
| 35 | VSSO | IO ground | VDDO | | | P | |
| 36 | CUSTOM | – | | – | – | – | – |
| 37 | SWDIO | Digital JTAG debug (Data IO) | VDDO | I/O | I | D | PU |
| 38 | SWCLK | Digital JTAG debug (Clk) | VDDO | I/O | I | D | PU |

**Table 1. PIN OUT**

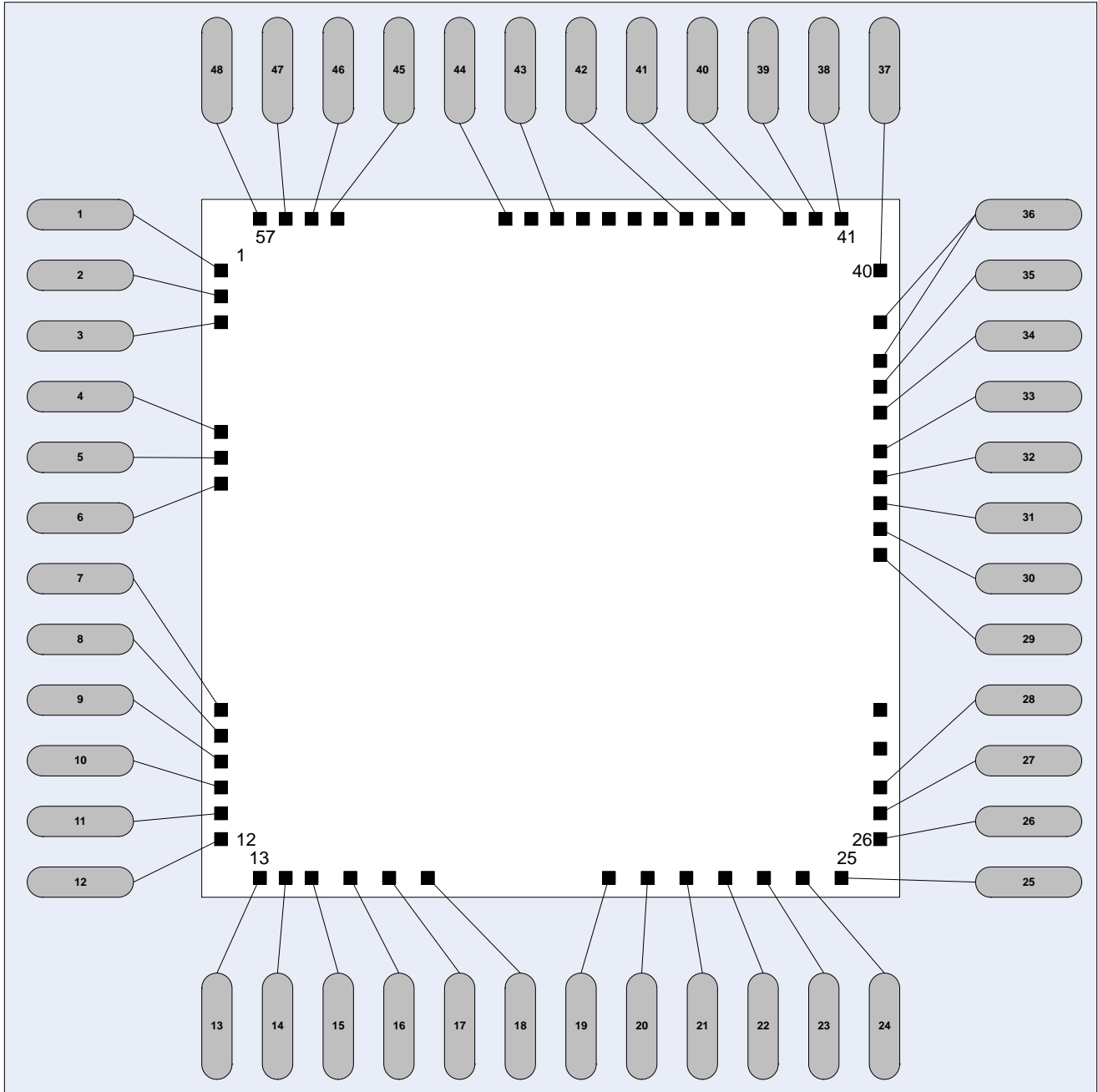| Pin# | Pad Name | Description | Domain | I/O | POR Direction | A/D | PU/PD |
|------|----------|-------------|--------|-----|---------------|-----|-------|
| 39 | DIO8 | Digital Input Output | VDDO | I/O | I | D | PU |
| 40 | DIO9 | Digital Input Output | VDDO | I/O | I | D | PU |
| 41 | DIO10 | Digital Input Output | VDDO | I/O | I | D | PU |
| 42 | DIO11 | Digital Input Output | VDDO | I/O | I | D | PU |
| 43 | DIO12 | Digital Input Output | VDDO | I/O | I | D | PU |
| 44 | DIO13 | Digital Input Output | VDDO | I/O | I | D | PU |
| 45 | DIO14 | Digital Input Output | VDDO | I/O | I | D | PU |
| 46 | DIO15 | Digital Input Output | VDDO | I/O | I | D | PU |
| 47 | DIO16 | Digital Input Output | VDDO | I/O | I | D | PU |
| 48 | DIO0 | Digital Input Output | VDDO | I/O | I | D | PU |

**ULPMC10 QFN48 Sample Package**



**Figure 3. ULPMC10 QFN48 Sample Package**

# ULPMC10

## ULPMC10 QFN48 Sample Package Overview

### Table 2. PIN OUT

| Pin# | Pad Name | Description | Domain | I/O | POR Direction | A/D | PU/PD |
|------|----------|-------------|--------|-----|---------------|-----|-------|
| 2 | DIO1 | Digital Input Output | VDDO | I/O | I | D | PU |
| 3 | DIO2 | Digital Input Output | VDDO | I/O | I | D | PU |
| 10 | DIO3 | Digital Input Output | VDDO | I/O | I | D | PU |
| 11 | DIO4 | Digital Input Output | VDDO | I/O | I | D | PU |
| 12 | DIO5 | Digital Input Output | VDDO | I/O | I | D | PU |
| 16 | AUX0_DIO27 | Digital Input Output configuration LSAD channel 0 configuration | VDD | I/O AI | I | D A | PU |
| 17 | AUX1_DIO28 | Digital Input Output configuration LSAD channel 1 configuration | VDD | I/O AI | I | D A | PU |
| 18 | AUX2 | LSAD channel 2 input | VDD | AI | I | A | PU |
| 22 | VDDA | Analog supply | VDD | | | A | |
| 23 | VSSA | Analog ground | VDD | | | P | |
| 24 | VDDD | Digital core supply | VDD | | | A | |
| 25 | VDD | Power supply 1 | VDD | | | P | |
| 27 | VDDC | Power supply 2 / CP output | VDD | | | A | |
| 29 | RESET | External reset signal | VDD | I | I | D | PD |
| 32 | DIO6 | Digital Input Output | VDDO | I/O | I | D | PU |
| 33 | DIO7 | Digital Input Output | VDDO | I/O | I | D | PU |
| 34 | VDDO | IO supply | VDDO | | | A | |
| 35 | EN_TEST | Test enable | VDDO | I | I | D | PD |
| 36 | VSSD | Digital ground | VDDO | | | P | |
| 36 | VSSO | IO ground | VDDO | | | P | |
| 37 | SWDIO | Digital JTAG debug (Data IO) | VDDO | I/O | I | D | PU |
| 38 | SWCLK | Digital JTAG debug (Clk) | VDDO | I/O | I | D | PU |
| 39 | DIO8 | Digital Input Output | VDDO | I/O | I | D | PU |
| 40 | DIO9 | Digital Input Output | VDDO | I/O | I | D | PU |
| 41 | DIO10 | Digital Input Output | VDDO | I/O | I | D | PU |
| 42 | DIO11 | Digital Input Output | VDDO | I/O | I | D | PU |
| 44 | DIO12 | Digital Input Output | VDDO | I/O | I | D | PU |
| 45 | DIO13 | Digital Input Output | VDDO | I/O | I | D | PU |
| 46 | DIO14 | Digital Input Output | VDDO | I/O | I | D | PU |
| 47 | DIO15 | Digital Input Output | VDDO | I/O | I | D | PU |
| 48 | DIO16 | Digital Input Output | VDDO | I/O | I | D | PU |
| 1 | DIO0 | Digital Input Output | VDDO | I/O | I | D | PU |
| 30 | EXT_CLK | External clock for MMCU | VDD | I/O | I | D | PD |
| 31 | WAKEUP | Wakeup Interrupt | VDD | I | I | D | PD |
| 43 | DIO17 (CLK_OUT) | Digital Input Output, ADC clock output | VDDO | I/O | O | D | PU |
| 4 | DIO18 | Digital Input Output | VDDO | I/O | I | D | PU |
| 5 | DIO19 | Digital Input Output | VDDO | I/O | I | D | PU |
| 6 | DIO20 | Digital Input Output | VDDO | I/O | I | D | PU |

# ULPMC10

**Table 2. PIN OUT**

| Pin# | Pad Name | Description | Domain | I/O | POR Direction | A/D | PU/PD |
|------|----------|-------------|--------|-----|---------------|-----|-------|
| 7 | DIO21 | Digital Input Output | VDDO | I/O | I | D | PU |
| 8 | DIO22 | Digital Input Output | VDDO | I/O | I | D | PU |
| 9 | DIO23 | Digital Input Output | VDDO | I/O | I | D | PU |
| 13 | DIO24 | Digital Input Output | VDDO | I/O | I | D | PU |
| 14 | DIO25 | Digital Input Output | VDDO | I/O | I | D | PU |
| 15 | DIO26 | Digital Input Output | VDDO | I/O | I | D | PU |
| 19 | VDD_XTAL | XTAL Power supply | VDD | | | P | |
| 20 | XTAL_OUT | External crystal | VDD | AO | O | A | |
| 21 | XTAL_IN | External crystal | VDD | AI | I | A | |
| 26 | CP2 | Charge Pump cap pin 2 | VDD | | | A | |
| 28 | CP1 | Charge Pump cap pin 1 | VDD | | | A | |

**Pin Connections**

The following table describes the required and recommended external connections and components. These connections and components are required to ensure proper device operation and performance.

**Table 3. REQUIRED AND RECOMMENDED EXTERNAL CONNECTIONS AND COMPONENTS**

| Comp | Function | Typ. Value | Tolerance |
|------|----------|------------|-----------|
| Cap (VDD−VSS) | VDD decoupling | 4.7 μF | ± 20% |
| Cap (VDDO−VSS) | VDDO decoupling | 4.7 μF | ± 20% |
| Cap (VDDD−VSS) | VDDD decoupling | 4.7 μF | ± 20% |
| Cap (VDDC−VSS) | VDDC decoupling | 1 μF | ± 20% |
| Cap (VDDA−VSSA) | VDDA decoupling | 2.2 μF | ± 20% |
| Cap (CMP1−CMP2) | Charge pump cap | 1 μF | ± 20% |
| Cap (VDD_XTAL−VSS) | VDD_XTAL decoupling | 1 μF | ± 20% |
| Res (VDD_XTAL−VDD) | VDD_XTAL RC filtering | 1 μF | ± 20% |
| XTAL | XTAL oscillator | 32.768 kHz | |

**Table 4. ABSOLUTE MAXIMUM RATINGS**

| Parameter | Symbol | Min | Max | Units |
|-----------|--------|-----|-----|-------|
| Input Voltage on any Digital Pin | | −0.3 | 3.8 | V |
| Input Voltage on any Analog Pin | | −0.3 | 3.8 | V |
| Input Voltage on any Supply Pin | | −0.3 | 3.8 | V |
| Current on any Digital Pin | | | ± 5 | mA |
| Current on any Analog Pin | | | ± 10 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 5. RECOMMENDED OPERATING CONDITIONS**

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Supply Applied to VDD (Note 1) | VDD | 1.8 | 3.3 | 3.5 | V |
| Internal Oscillator Clock Frequency | | 1 | | 20 | MHz |
| Externally−Supplied Clock Frequency | | | | 40 | MHz |
| Ambient Operating Temperature Range | Ta | −40 | | 85 | °C |
| Junction Temperature Range | Tj | | | 75 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
1. Operation with Flash Read to down 1.3 V supported. For Flash Write a minimum VDD of 1.8 V required.

**Table 6. ESD AND LATCH−UP CHARACTERISTICS**

| Parameter | Conditions | Max | Units |
|---|---|---|---|
| ESD – Human Body Model | JEDEC JS−001−2010, all pins | 2000 | V |
| ESD – Charged Device Model | JESD22−C101−E, all pins | 750 | V |
| ESD – Machine Model | JESE22−A115−C, all pins | 250 | V |
| Latch−Up | JEDEC STD−78, all pins | ± 100 | mA |

## ELECTRICAL CHARACTERISTICS

**Typical Values**

Unless otherwise noted, Typ values specify the typical values based on design and characterization data under normal operating conditions. Normal operating conditions include a supply voltage (VDD) of 3.3 V and an operating temperature of 25°C. For specific blocks, the details of the normal operation conditions are described in their respective sections.

**Minimum and Maximum Values**

Unless otherwise noted, Min and Max values specify the designed range or measurement range and are guaranteed by design and/or characterization.

Min and Max values specified may be based on factory production test limits, design, or characterization data.

**Normal Operating Conditions**

Unless otherwise noted, normal operating conditions indicate an ambient temperature Ta = 25°C and a supply voltage VDD = 3.3 V. VDDD and VDDA and the Internal Oscillator (PLL) are calibrated to their preset factory calibration settings and correspond to their respective Typ values. VDDO are powered externally from the VDDD Digital Supply Regulator. No external loads are applied to digital I/O or analog pins.

### Table 7. SYSTEM DC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C, VDD = 3.3 V, VDDO = VDDD = 1.8 V, 16–bit/32–bit mixed instructions, 66% execution from flash memory, data access from SRAM, peripherals disabled) unless otherwise noted)

| Parameter | | Symbol | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| Main Supply Voltage Range | | VDD | | | 1.3 | 1.8 | 3.6 | V |
| Run Mode Current | Run_Fast Mode Current | IDD | Typical application, read from flash, analog disabled | 1 MHz | | 0.4 | | mA |
| | | | | 2 MHz | | 0.8 | | |
| | | | | 5 MHz | | 2 | | |
| | | | | 10 MHz | | 4 | | |
| | | | | 20 MHz | | 8 | | |
| | | | Typical application, execution from SRAM | 1 MHz | | 0.3 | | |
| | | | | 2 MHz | | 0.6 | | |
| | | | | 5 MHz | | 1.5 | | |
| | | | | 10 MHz | | 3 | | |
| | | | | 20 MHz | | 6 | | |
| | Run_Slow Mode Current (Note 2) | IDD | Typical application, read from flash, analog disabled | 1 MHz (VDDD = 1.3 V) | | 0.2 | | mA |
| | | | Typical application, read from flash, analog disabled | 5 MHz (VDDD = 1.3 V) | | 1 | | mA |
| Deep Standby Mode Current | | IDD | | | | 0.5 | | μA |
| Sleep Mode Current | | IDD | | | | 0.2 | | μA |
| Shutdown Mode Current | | IDD | | | | 0.05 | | μA |

2. VDDD = VDDC = 1.3 V when in Run_Slow Mode.

### Table 8. DIGITAL I/O PINS (DIO, SPI, SWD) DC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C, VDDO = VDDD, Pull–up/Pull–down Enabled) unless otherwise noted)

| Parameter | Symbol | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| VDDO Supply Voltage Range | VDDO | | | 1.8 | | 3.6 | V |
| Output Low Level | $V_{ol}$ | $I_{ol}$ = 4 mA | | | | 0.2 x VDDO | V |
| Output High Level | $V_{oh}$ | $I_{ol}$ = −4 mA | | 0.8 x VDDO | | | V |
| Input Low Level | $V_{il}$ | | | | | 0.2 x VDDO | V |
| Input High Level | $V_{ih}$ | | | 0.8 x VDDO | | | V |
| Pull − Up Resistance | $R_{pu}$ | Non−$I^2C$ | VDDO = 1.8 V | | 10 | 250 | kΩ |
| | | | VDDO = 3.3 V | | 10 | 250 | |
| | | $I^2C$ | VDDO = 1.8 V | | 10 | 250 | |
| | | | VDDO = 3.3 V | | 10 | 250 | |
| Pull − Down Resistance | $R_{pd}$ | VDDO = 1.8 V | | | 250 | | kΩ |
| | | VDDO = 3.3 V | | | 250 | | |
| Pin Capacitance | $C_{pd}$ | | | | 5 | | pF |
| Maximum Output Current | $I_{ol}$, $I_{oh}$ | | | | | ± 4 | mA |
| Input Leakage Current | $I_l$ | | | | | ± 1 | μA |

### Table 9. WAKEUP, EXTCLK, RESET I/O PINS DC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C, Pull − up / Pull − down Enabled, GPIO mode) unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| WAKEUP, EXTCLK, RESET Supply Voltage Range | VDD | | 1.8 | | 3.6 | V |
| Output Low Level | $V_{ol}$ | $I_{ol}$ = 4 mA | | | 0.2 x VDD | V |
| Output High Level | $V_{oh}$ | $I_{ol}$ = −4 mA | 0.8 x VDD | | | V |
| Input Low Level | $V_{il}$ | | | | 0.2 x VDD | V |
| Input High Level | $V_{ih}$ | | 0.8 x VDD | | | V |
| Pull − Up Resistance | $R_{pu}$ | VDD = 1.8V | | 10 | 250 | kΩ |
| | | VDD = 3.3 V | | 10 | 250 | |
| Pull − Down Resistance | $R_{pd}$ | VDD = 1.8V | | 250 | | kΩ |
| | | VDD = 3.3 V | | 250 | | |
| Pin Capacitance | $C_p$ | | | 5 | | pF |
| Maximum Current | | | | | ± 4 | mA |

### Table 10. FLASH MEMORY DC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C) unless otherwise noted. All parameters in this section are obtained through qualification and characterization and are not tested in production)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | VDDD | Flash Read Only | 1.3 | 1.8 | 1.98 | V |
| | | Flash Write | 1.62 | 1.8 | 1.98 | |
| Write Endurance | | | 20000 | | | cycles |
| Data Retention | | | 100 | | | years |
| Programming Time (per word) | | | | 20 | | μs |
| Erase Time | | Single page | 20 | | | ms |
| | | Entire array | 20 | | | |

### Table 11. LF RC OSCILLATOR DC & AC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C) unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | | 1.3 | | 3.6 | V |
| Frequency Range | f | | | 32 | | kHz |
| Frequency Accuracy | | | −50 | | +50 | % |

### Table 12. 32.768 kHz XTAL CLOCK DC & AC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C), unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | | 1.3 | | 3.6 | V |
| Supply Current | | CL = 3.5 pF | | 0.2 | | μA |
| Frequency | f | | | 32768 | | Hz |
| Duty Cycle | | | | 50 | | % |
| Startup Time | | | | | 3 | s |

# ULPMC10

## Table 13. PLL DC & AC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C) unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | VDDD | | 1.1 | 1.8 | 1.98 | V |
| | VDDA | | 1.62 | 1.8 | 2 | |
| Reference Clock | f | Non–divided | 0.02 | | 65.536 | MHz |
| Reference Clock | | Divided | 32 | | 512 | kHz |
| Reference Clock Duty Cycle | | | 10 | | 90 | % |
| Output Frequency Range | | | 2 | | 20 | MHz |
| Startup Time | | | | | 100 | μs |
| Lock Time | | Ref Clock of 32.768 kHz | | | 10 | ms |
| Tracking Range | | Reference Clock Drift | –2 | | 2 | % |
| VCO Frequency Range | | Before Multiplication | 2 | | 20 | MHz |
| VCO Frequency Range | | After Multiplication | 2 | | 80 | MHz |
| VCO Frequency Precision | | After Trim | –1 | | 1 | % |
| VCO Frequency Drift | | 0C–50C | –1.5 | | 1.5 | % |
| VCO Jitter | | | | | 400 | ps |
| VCO Output Duty Cycle | | Multiplier 1x or 2x | 45 | | 55 | % |
| | | Multiplier 3x | 25 | | 75 | |
| | | Multiplier 4x | 40 | | 60 | |

## Table 14. VDDA REGULATOR DC & AC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C), unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | | 2.2 | | 3.6 | V |
| Output Voltage | VDDA | CL = 2.2 μF | | 2 | | V |
| Load Current | | | | | 4 | mA |
| Load Regulation | | | | 5 | | mV/mA |
| Line Regulation | | | | 20 | | mV/V |
| PSRR | | @ 1 kHz unloaded | 20 | | | dB |

## Table 15. VDDD REGULATOR DC & AC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C), unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | | 1.8 | | 3.6 | |
| Output Voltage | VDDD | After Trim, CL = 4.7 μF | 1.3 | 1.8 | | V |
| | VDDD | Standby Mode | | 1.5 | | V |
| Trim Step | | | | 20 | | mV |
| Load Current | | | | | 15 | mA |
| Load Regulation | | | | | 10 | mV/mA |
| Line Regulation | | | | | 20 | mV/V |
| PSRR | | | 20 | | | dB |

### Table 16. VDDC CHARGE PUMP DC & AC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C), unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | | 2.6 | | 3.6 | V |
| Output Voltage | VDDC | | 1.3 | | 1.8 | V |
| Drive Circuit Current | | | | 100 | | nA/kHz |
| Frequency | | Normal Mode | 32 | | 500 | kHz |
| | | Low Power Mode | 1 | | 32 | |
| Load Regulation | | VDD > 2.6 V, f = 100 kHz | | | 20 | mV/mA |
| | | VDD < 2.6 V, f = 100 kHz | | | 50 | |
| | | VDD > 2.6 V, f = 1 kHz | | | 30 | |
| Efficiency | | | 95 | | | % |
| | | f = 1 kHz | 75 | | | |
| Stabilization Time | | f = 100 kHz | | | 5 | ms |
| | | f = 1 kHz | | | 20 | |

### Table 17. A/D CONVERTER DC & AC ELECTRICAL CHARACTERISTICS

(Typical operating conditions (Ta = 25°C), unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | VDDA | | | 2 | | V |
| Resolution | | | | 12 | | Bits |
| Input Signal Level | | | 0 | | 2 | V |
| Input Impedance | | | | 1 | | MΩ |
| Sampling Frequency | | f = 128 kHz | | 0.8 | | kHz |
| INL | | | −4 | | 4 | LSB |
| DNL | | | −2 | | 2 | LSB |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Electrostatic Discharge (ESD) Device**

**WARNING:** ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

**Packaging Options**

The ULPMC10 device is intended for use in stacked packages where the customer purchases a proprietary ASIC from ON, which combines to form a miniature, low−power processing system. ON Semiconductor recommends a QFN48 package for this purpose; however, the exact pin out requirements from both ULPMC10 and a proprietary ASIC will determine the package used. To allow customers to prototype a stacked package system before actually making this, ULPMC10 is available standalone in a QFN48 sample package.

**Ordering Information**

To order ULPMC10 QFN48 packages for prototyping or to discuss how to engage with ON Semiconductor in developing a proprietary ASIC to meet specific circuit needs, please contact your ON Semiconductor Sales Representative.

**Development Tools**

An advanced, easy−to−use tool chain is available from IAR Systems. The tool chain including in−circuit debugging probes are available directly from IAR.

ON Semiconductor markets a miniature development board that connects easily to an in−circuit debugging probe from IAR (see: Figure 4).

**Figure 4. Miniature Development Board**

The development board, together with documentation that can be downloaded from ON Semiconductor's website, allows for quick evaluation and application prototyping. To order the development board, please contact your ON Semiconductor Sales Representative.

# ULPMC10

## PACKAGE DIMENSIONS

**QFN48 6x6, 0.4P**
CASE 485AN
ISSUE O



**TOP VIEW**

**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**

**DETAIL B**
**ALTERNATE CONSTRUCTION**

EXPOSED Cu    MOLD CMPD

**SIDE VIEW**

NOTE 4

**BOTTOM VIEW**
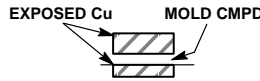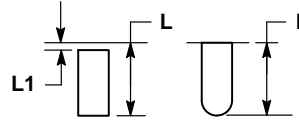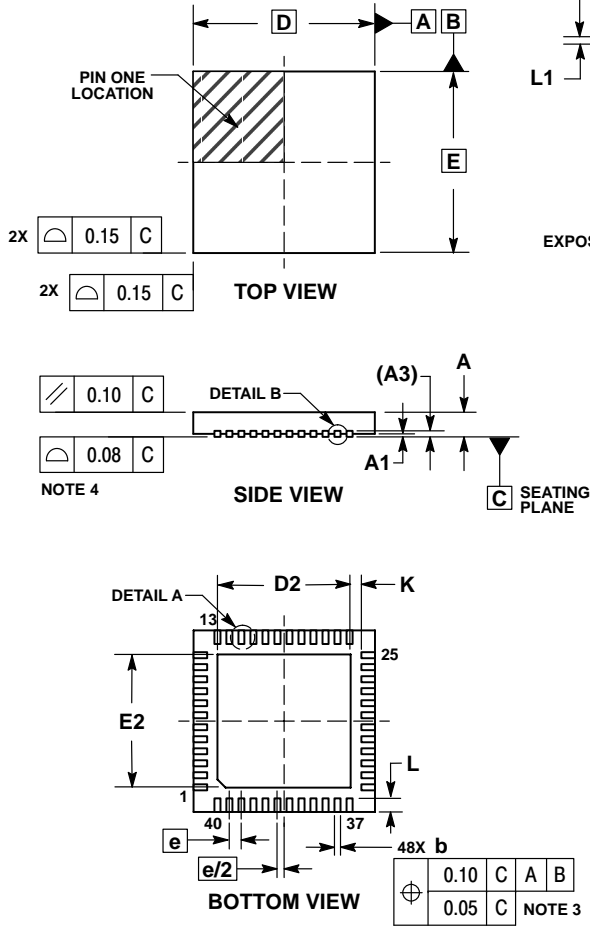
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
| --- | --- | --- |
| | **MIN** | **MAX** |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.15 | 0.25 |
| D | 6.00 BSC | |
| D2 | 4.25 | 4.55 |
| E | 6.00 BSC | |
| E2 | 4.25 | 4.55 |
| e | 0.40 BSC | |
| K | 0.20 MIN | |
| L | 0.35 | 0.55 |
| L1 | 0.00 | 0.15 |

### SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS
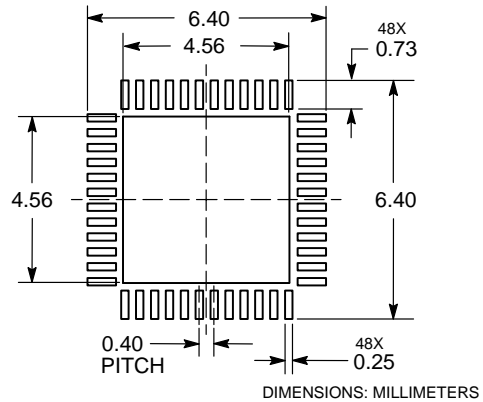
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ARM and Cortex are registered trademarks of ARM Holdings, plc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.

**ULPMC10/D**