UM10437

GreenChip 65 W TEA1738LT/T and TEA1703 demo board

Rev. 1 — 28 February 2011 | User manual

Document information

Info	Content
Keywords	Notebook adapter, TEA1738LT/T, TEA1703, fixed frequency, ultra-low standby power, high-efficiency, slim line
Abstract	This manual provides the specification, schematics and PCB layout of the 65 W TEA1738LT/T and TEA1703 demo board. For details on the TEA1738LT/T or TEA1703 IC please refer to the application note.

Revision history

Rev	Date	Description
v.1	20110228	first issue

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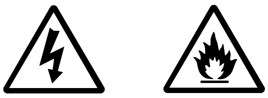
1. Introduction

WARNING

Lethal voltage and fire ignition hazard



The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire.

This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This 65 W TEA1738LT/T and TEA1703 demo board demonstrates the capabilities of the TEA1738LT/T Switched-Mode Power Supply (SMPS) controller and the TEA1703 standby controller. This manual provides the specification, schematics and PCB layout of the 65 W TEA1738LT/T and TEA1703 demo board.

Refer to the TEA1738LT/T *data sheet* and *application note* (AN10981) for details on the TEA1738LT/T. In addition, refer to the *TEA1703 datasheet* and *application note* (AN11012) for details on the TEA1703.

In Standby mode operation (no-load condition), the TEA1703 standby control IC monitors the output voltage and disables the primary controller until the output voltage has reached its lowest preset value. This ensures ultra-low standby power consumption.

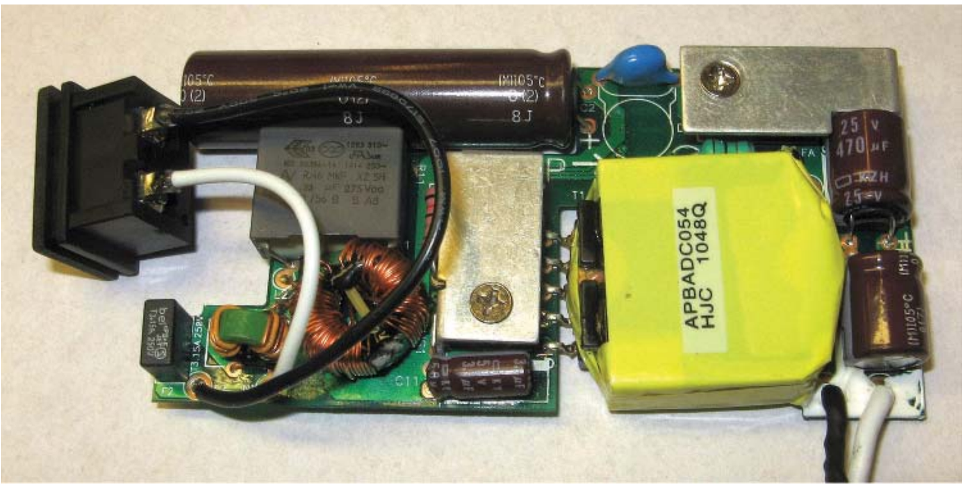


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Fig 1. TEA1738LT/T and TEA1703 65 W demo board

1.1 Features

- Universal mains supply operation
- OverCurrent Protection (OCP)
- OverPower Protection (OPP)
- Low ripple and noise
- Slim line transformer

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- Low-cost implementation
- Indicator LED
- Ultra low no-load standby power (< 50 mW at 230 V, 50 Hz)
- ENERGY STAR compliant
- EMI CISPR22 compliant

2. Power supply specification

Table 1. Input specification

Symbol	Description	Conditions	Specification	Unit
V_i	input voltage	-	90 to 264	V
f_i	input frequency	-	47 to 60	Hz
$P_{i(no\_load)}$	input power (no-load)	at 230 V; 50 Hz	< 50	mW

Table 2. Output specification

Symbol	Description	Conditions	Specification	Unit
V_o	output voltage	-	19	V
$V_{o(min)}$	Minimum output voltage	during standby mode operation	≥ 12	V
$V_{o(ripple)(p-p)}$	peak-to-peak output ripple voltage	20 MHz bandwidth	≤ 200	mV
I_o	output current	continuous	0 to 3.34	A
$I_{o(p)}$	peak output current	for 50 ms	5	A
P_o	output power	0 to 40 °C6	5	W
t_{holdup}	hold-up time	at 115 V; 60 Hz; full load	5	ms
-	line regulation	-	±1%	
-	load regulation	-	±2%	
$t_{startup}$	start-up time	at 115 V; 60 Hz	≤ 3s	
η	efficiency	according to ENERGY STAR (EPS 2)	≥ 87	%
-	EMI	CISPR22 compliant	pass	-

3. Perf ormance data

Performance figures based on the following PCB design:

- Schematic version: Tuesday 18 November 2010 rev. A

3.1 Efficiency

Efficiency measurements were made using an automated test program containing a temperature stability detection algorithm. The output voltage and current were measured using a 4-wire current sense configuration directly at the PCB connector. Measurements were performed for 115 V; 60 Hz and 230 V; 50 Hz.

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Table 3. Efficiency results[1][2]

Condition	ENERGY STAR 2.0 efficiency requirement (%)	Efficiency (%)							
		Average	100 % load	75 % load	50 % load	100 % load	1 W	0.5 W	0.25 W
115 V, 60 Hz	> 87	90.3	88.8	90.5	90.4	90.5	76.8	69.1	57.8
230 V, 50 Hz	> 87	91.6	91.6	92.1	91.7	90.9	74.8	66.4	54.3

[1] Warm-up time: 10 minutes

[2] There is an efficiency loss of 1 % (approximately) when measured at the end of a 1 m output cable.

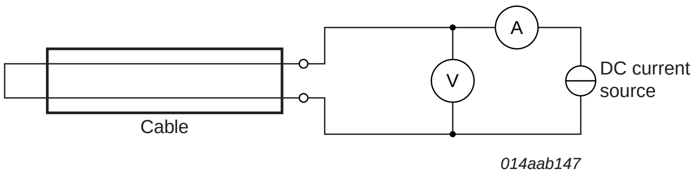

Fig 2. DC resistance output cable

DC resistance cable = voltage drop / current = 0.228 / 3.349 = 0.0681 Ω (2-way).

3.2 No-load power consumption

Power consumption performance of the total application board with no-load connected was measured using a Yokogawa WT210 digital power meter. Integration time was set to 6 minutes to calculate the average dissipated power. The output voltage variation results are shown in Table 4. Measurements were performed for 90 V; 60 Hz, 115 V; 60 Hz, 230 V; 50 Hz, and 264 V; 50 Hz.

Table 4. Output voltage and power consumption: no-load

Condition	ENERGY STAR 2.0 requirement (mW)	Output voltage high (V)	Output voltage low (V)	No-load power consumption (mW)
90 V; 60 Hz	≤ 300	19.8	14.2	8
115 V; 60 Hz	≤ 300	19.8	14.2	11
230 V; 50 Hz	≤ 300	19.8	14.2	39
264 V; 50 Hz	≤ 300	19.8	14.2	56

3.3 Minimum output current in normal operation

The minimum current required to leave Standby mode and enter normal operation was measured for 90 V; 60 Hz and 264 V; 50 Hz.

Table 5. Minimum current for normal operation

Condition	90 V; 60 Hz	264 V; 50 Hz
Current (mA)	2	5

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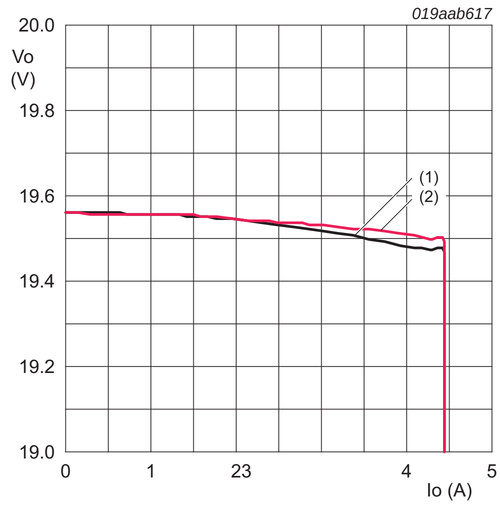
3.4 Output regulation

The output voltage as a function of load current was measured using a 4-wire current sense configuration directly at the PCB connector. Measurements were performed without probes attached to the application for 115 V; 60 Hz and 230 V; 50 Hz.



(1) V_o = 115 V (AC); 60 Hz.

(2) V_o = 230 V (AC); 50 Hz.

Fig 3. Output voltage regulation as function of current load

3.5 Line regulation

The output voltage as a function of mains input voltage was measured directly at the output connector for full load (3.34 A) condition.

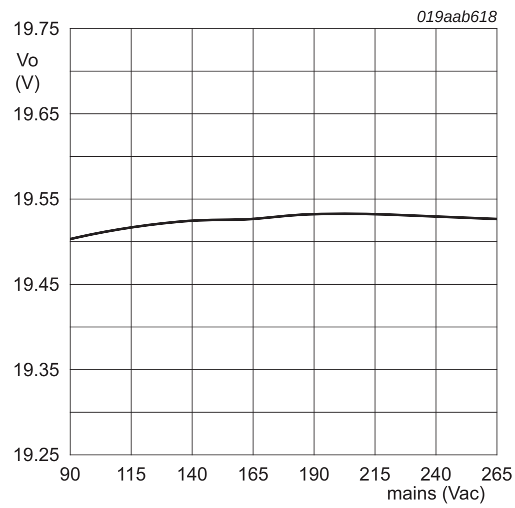


Fig 4. Output voltage as function of mains voltage

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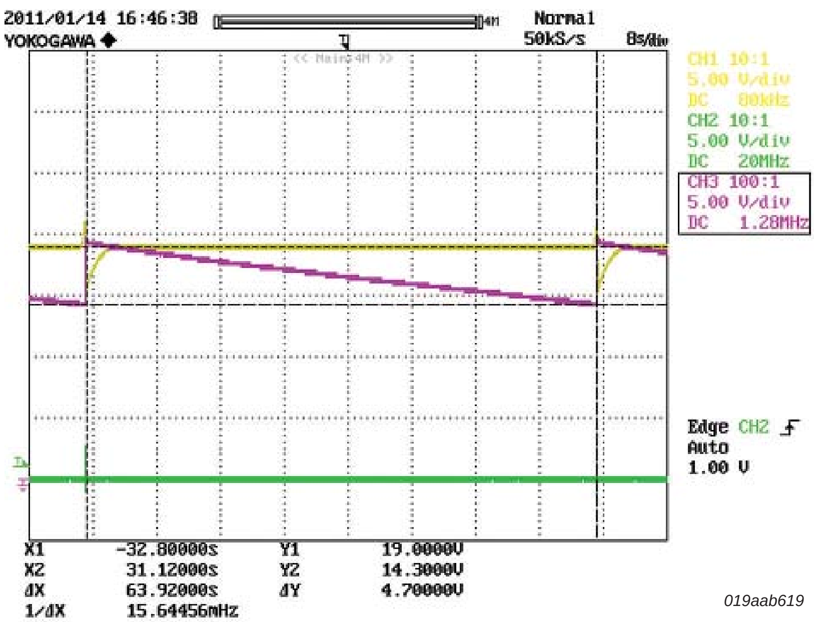
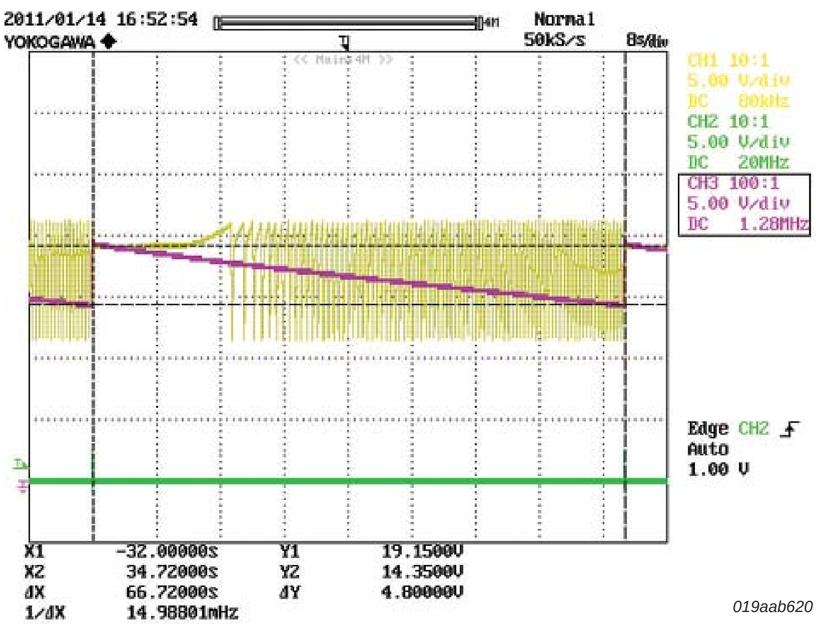
3.6 Output voltage regulation in Standby mode

The output voltage regulation during no-load operation was measured for 90 V; 60 Hz and 264 V; 50 Hz.



Chan1 (yellow): V_{CC}; Chan2 (green): Gate pulse; Chan3 (magenta): V_O

Fig 5. Output voltage regulation at no-load 90 V; 60 Hz



Chan1 (yellow): V_{CC}; Chan2 (green): Gate pulse; Chan3 (magenta): V_O

Fig 6. Output voltage regulation at no-load 264 V; 50 Hz

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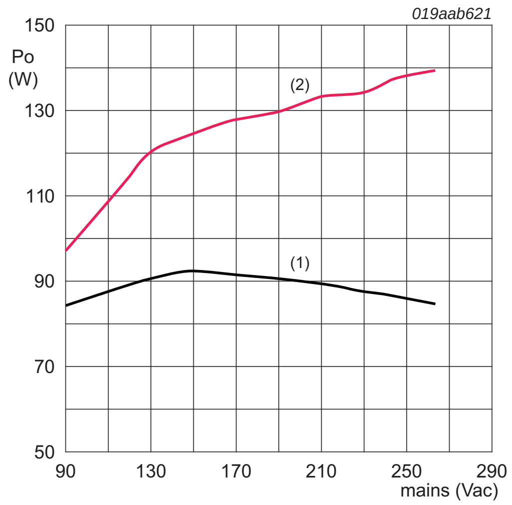
3.7 OverPower Protection (OPP)

Nominal and peak output power was measured directly at the output connector for various mains input voltages. Peak output power was measured after removing C18 and replacing R16 for 180 kΩ.



(1) Nominal power (W).

(2) Peak power (W).

Fig 7. Nominal and peak output power as function of mains voltage

3.8 VCC voltage

The IC VCC pin 1 voltage was measured for both no-load and full load (3.34 A) conditions.

Table 6. VCC voltage

Condition	115 V; 60 Hz	230 V; 50 Hz
No-load	18.9	19.0
Full load (3.34 A)	21	20.2

3.9 Brownout and start level

Brownout and start level was measured for no-load and full load (3.34 A) conditions.

Table 7. Brownout and start level results

Condition	Brownout V (AC)	Start level V (AC)
No-load	63	84
Full load (3.34 A)	78	85

3.10 OverVoltage Protection (OVP)

Applying a short-circuit across the opto-LED of the optocoupler (M5) creates an output overvoltage condition. The output voltage was measured directly at the output connector for both full load (3.34 A) and no-load condition. In no-load condition, the fault condition is processed when the primary controller is active.

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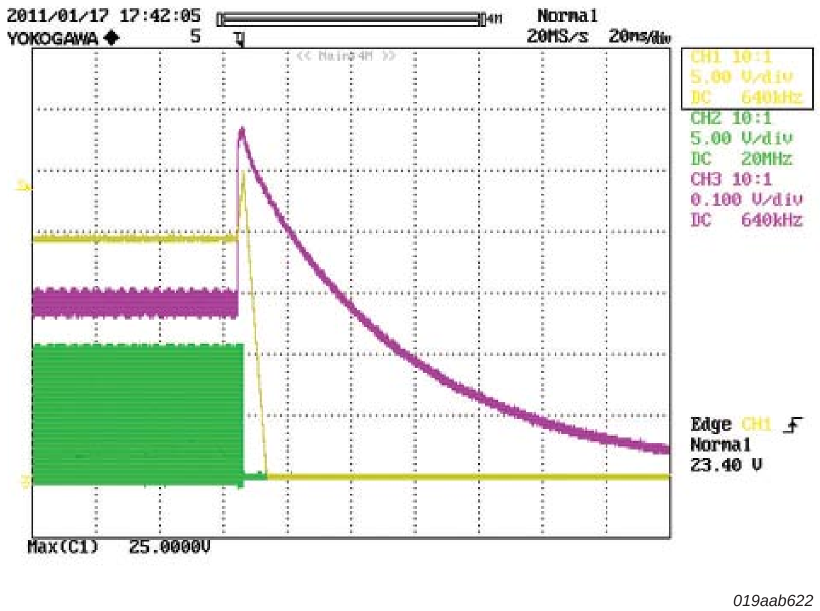
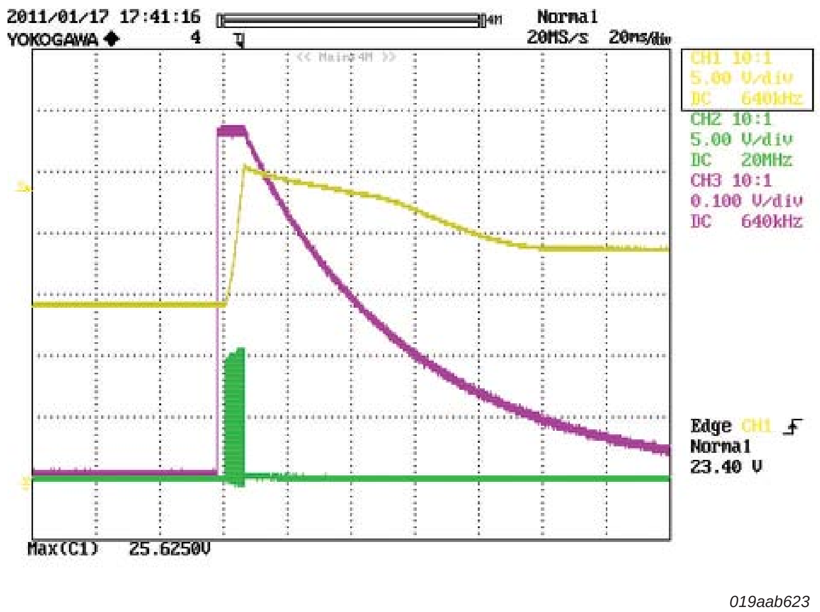
Table 8. Maximum output voltage in case of OVP

Condition	115 V (AC)	230 V (AC)
No-load	25.6	25.6
Full load (3.34 A)	25	25.2



Chan1 (yellow): V_O; Chan2 (green): Gate pulse; Chan3 (magenta): Ctrl voltage.

Fig 8. 230 V; 50 Hz; full load maximum output voltage when OVP is triggered



Chan1 (yellow): V_O; Chan2 (green): Gate pulse; Chan3 (magenta): Ctrl voltage.

Fig 9. 230 V; 50 Hz; no-load maximum output voltage when OVP is triggered

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3.11 Start-up time

Start-up time was measured for three mains input voltages and full load (3.34 A) condition. V_i input measured using a current probe (to avoid adding additional capacitance to the mains input). V_o was measured using a voltage probe grounded at the secondary side.

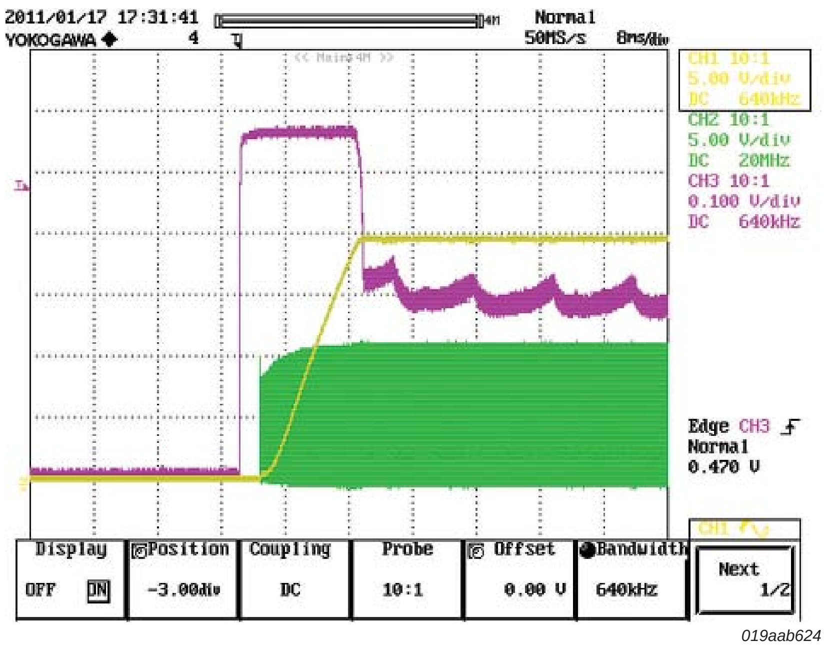
Table 9. Start-up time

Condition	Start-up time (s)
90 V; 60 Hz	3.2
115 V; 60 Hz	2.0
230 V; 50 Hz	0.8

If the start-up time is considered too long, it is advised to change the input circuit as described in *application note AN10981*.

3.12 Start-up profile

The shape of the output voltage was measured for three mains input voltages during start-up directly from the output connector under the full load (3.34 A) condition. V_o was measured using a voltage probe grounded at the secondary side.



Chan1 (yellow): V_O; Chan2 (green): Gate pulse; Chan3 (magenta): Ctrl voltage.

Fig 10. 90 V; 60 Hz; full load; start up profile

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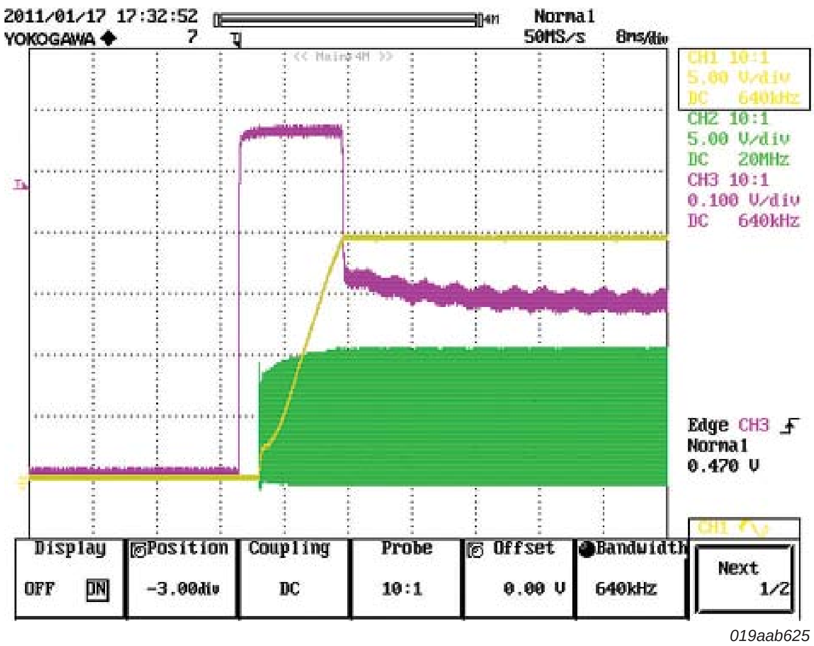

Chan1 (yellow): V_O; Chan2 (green): Gate pulse; Chan3 (magenta): Ctrl voltage.

Fig 11. 264 V; 50 Hz; full load; start up profile

Remark: The small discontinuity in the output voltage ramp at 264 V; 50 Hz is caused by the slow start function not limiting the primary current because it is hidden by the leading edge blanking period of 300 ns.

3.13 Hold-up time

Hold-up time is defined as the time between the following moments:

- After mains switch off; the moment that the lowest bulk cap voltage during a mains cycle is crossed
- The moment that the output voltage starts to drop

The hold-up time is measured for 115 V; 60 Hz under full load (3.34 A) condition. Output voltage duration was measured directly at the output connector.

The hold-up time at 115 V, 60 Hz is 10.9 ms.

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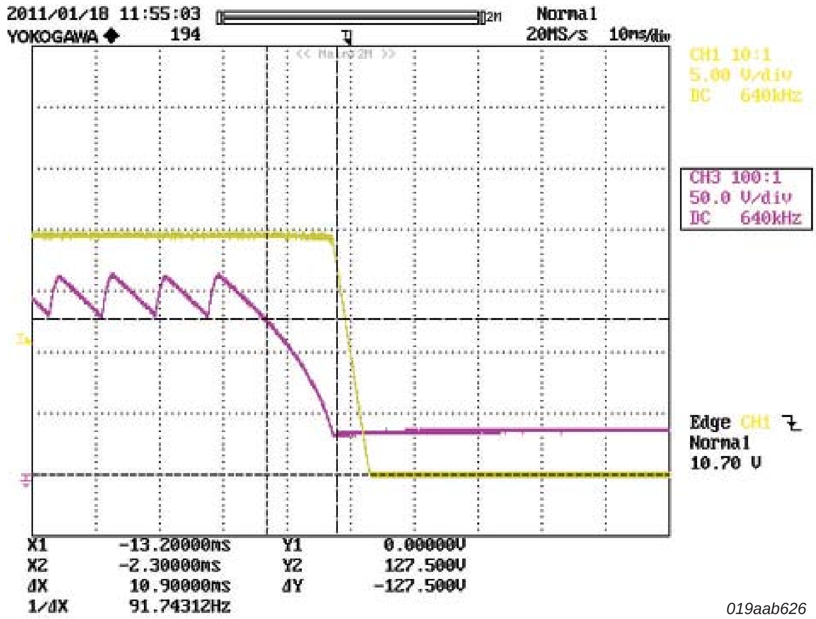

Chan1 (yellow): V_o; Chan3 (magenta): Bulk cap voltage.

Fig 12. full load; hold–up time at 115 V; 60 Hz

3.14 Dynamic loading

The output voltage was measured at the end of the cable. Both channels of the oscilloscope are set to DC mode.

Table 10. Dynamic loading test conditions and results

Condition	Loading	$V_{o(ripple)(p-p)}$ (mV)
90 V; 47 Hz	I_o: 0 % to 50 %, frequency 50 Hz; duty cycle 50 %	375
264 V; 63 Hz	I_o: 0 % to 50 %, frequency 50 Hz; duty cycle 50 %	375

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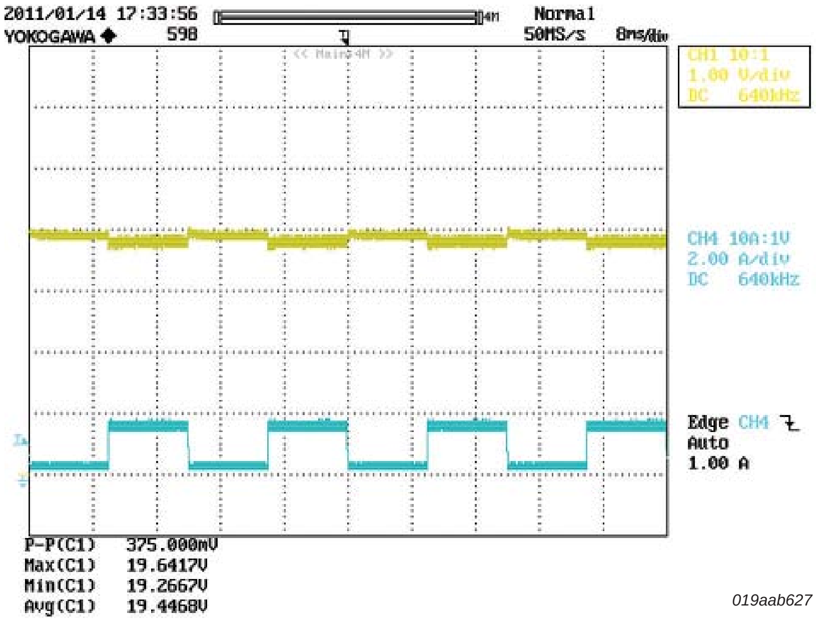
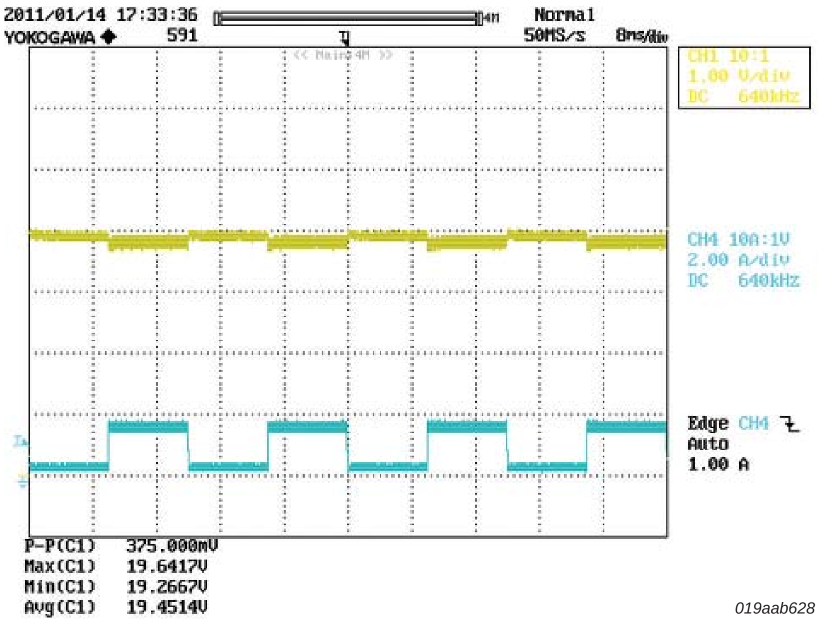


Chan1 (yellow): V_o; Chan4 (cyan): I_o.

Fig 13. Dynamic loading 90 V; 47 Hz



Chan1 (yellow): V_o; Chan4 (cyan): I_o.

Fig 14. Dynamic loading 264 V; 63 Hz

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3.15 Output ripple and noise

Output ripple and noise were measured at the end of the cable using the measurement set-up described in Figure 15. An oscilloscope probe connected to the end of the adapter cable using a probe tip. 100 nF and 1 μF capacitors were added between plus and minus to reduce the high frequency noise. Output ripple and noise were measured for mains voltages 90 V; 47 Hz and 264 V; 63 Hz, both at full load (3.34 A) output current.

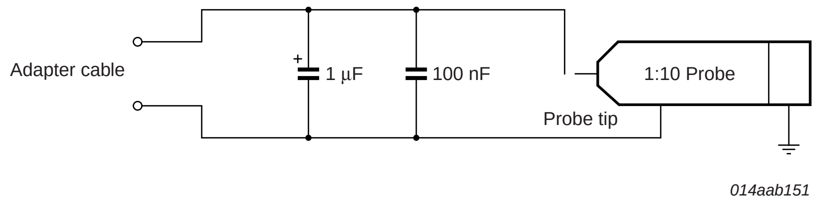
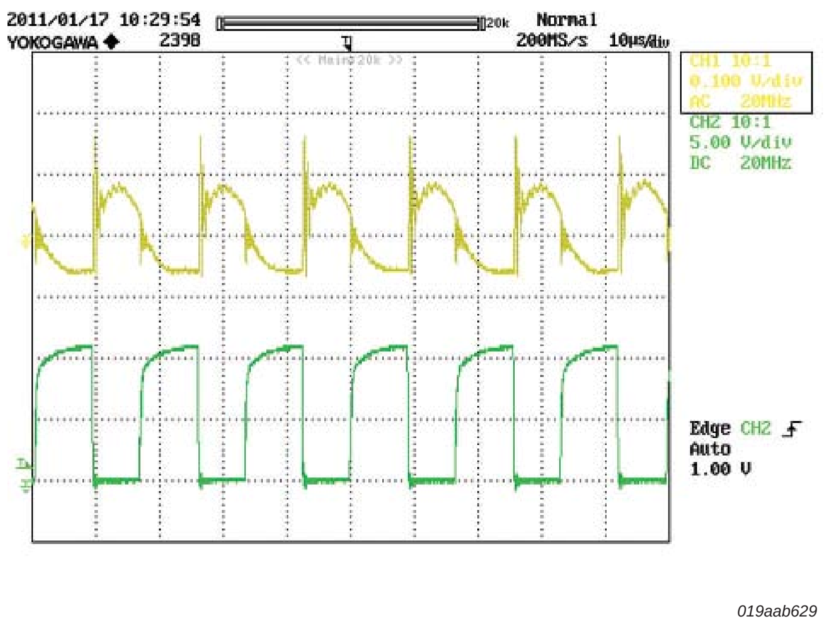


Fig 15. Output ripple and noise measurement set-up

Table 11. Output ripple and noise measurements

Condition	$V_{o(ripple)(p-p)}$ (mV)
90 V; 47 Hz	130
264 V; 63 Hz	110



Chan1 (yellow): V_o; Chan2 (green): Gate pulse

Fig 16. Output ripple and noise at 90 V; 47 Hz

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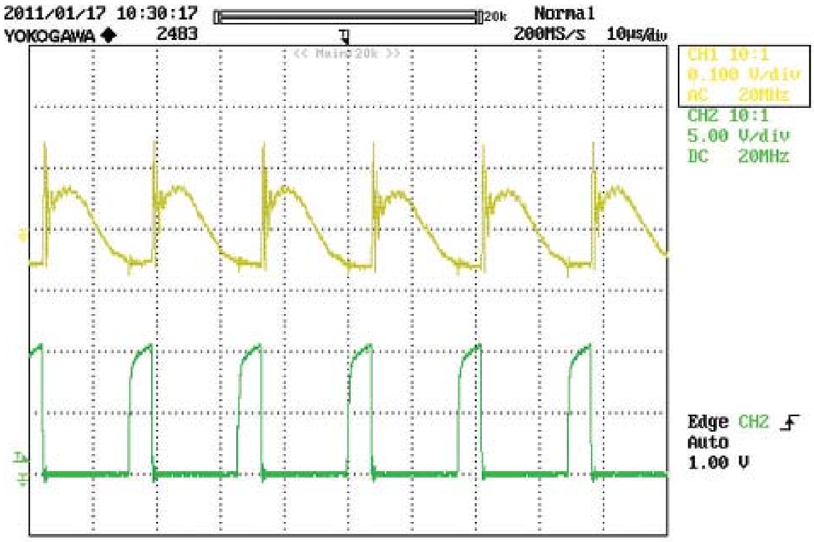

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Chan1 (yellow): V_o; Chan2 (green): Gate pulse

Fig 17. Output ripple and noise at 264 V; 63 Hz

3.16 EMI performance

Conditions:

- Type: conducted EMC measurement
- Frequency range: 150 kHz to 30 MHz
- Output power: full load condition
- Supply voltage: 110 V and 230 V (AC)
- Margin: 6 dB below limit
- Measurements performed by Cerpass technology corp. Taipei (Taiwan)

Remark: The displayed trace line in the following graphs is the quasi-peak measurement result

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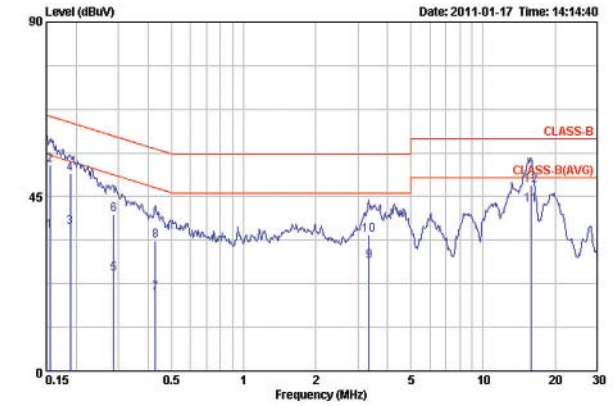

Item	Freq	Read Value	Factor	Result	Limit	Margin	Remark
	MHz	dBuV	dB	dBuV	dBuV	dBuV	
1	0.155	36.133	0.079	36.212	55.717	-19.505	Average
2	0.155	53.127	0.079	53.206	65.717	-12.511	QP
3	0.189	37.053	0.072	37.125	54.080	-16.955	Average
4	0.189	50.914	0.072	50.986	64.080	-13.094	QP
5	0.287	24.985	0.062	25.047	50.617	-25.570	Average
6	0.287	40.259	0.062	40.321	60.617	-20.296	QP
7	0.428	20.014	0.054	20.068	47.293	-27.225	Average
8	0.428	33.604	0.054	33.658	57.293	-23.635	QP
9	3.348	28.275	-0.029	28.246	46.000	-17.754	Average
10	3.348	35.121	-0.029	35.092	56.000	-20.908	QP
11	15.960	42.791	0.025	42.816	50.000	-7.184	Average
12	15.960	47.886	0.025	47.911	60.000	-12.089	QP

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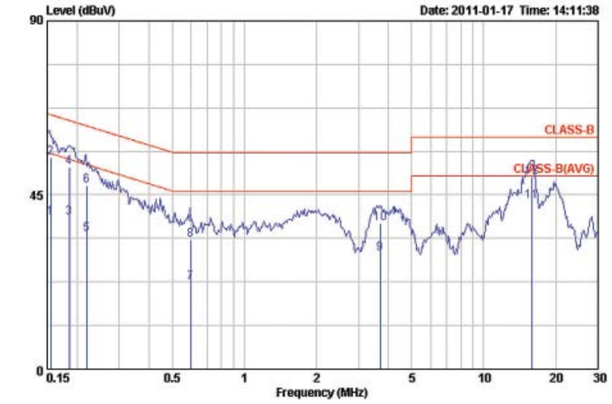
Fig 18. 115 V, 65 W TEA1738LT/T and TEA1703 demo board phase N



Item	Freq	Read Value	Factor	Result	Limit	Margin	Remark
	MHz	dBuV	dB	dBuV	dBuV	dBuV	
1	0.155	39.165	0.029	39.194	55.728	-16.534	Average
2	0.155	54.744	0.029	54.773	65.728	-10.955	QP
3	0.186	39.086	0.023	39.109	54.227	-15.118	Average
4	0.186	52.243	0.023	52.266	64.227	-11.961	QP
5	0.219	34.835	0.017	34.852	52.853	-18.001	Average
6	0.219	47.405	0.017	47.422	62.853	-15.431	QP
7	0.596	22.398	-0.016	22.382	46.000	-23.618	Average
8	0.596	33.289	-0.016	33.273	56.000	-22.727	QP
9	3.697	29.799	-0.073	29.726	46.000	-16.274	Average
10	3.697	37.628	-0.073	37.555	56.000	-18.445	QP
11	15.890	43.097	0.199	43.296	50.000	-6.704	Average
12	15.890	49.333	0.199	49.532	60.000	-10.468	QP

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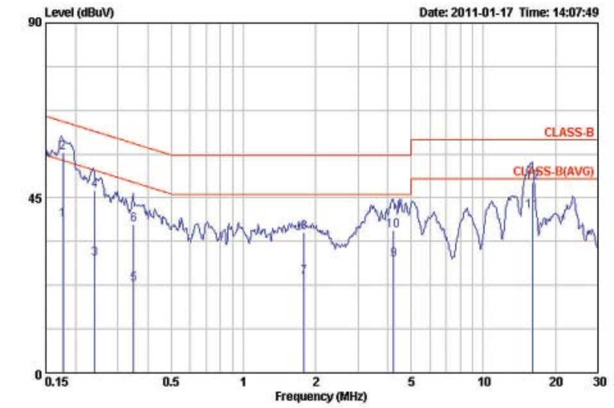
Fig 19. 115 V, 65 W TEA1738LT/T and TEA1703 demo board phase L



Item	Freq	Read Value	Factor	Result	Limit	Margin	Remark
	MHz	dBuV	dB	dBuV	dBuV	dBuV	
1	0.177	39.363	0.074	39.437	54.635	-15.198	Average
2	0.177	56.667	0.074	56.741	64.635	-7.894	QP
3	0.240	29.342	0.066	29.408	52.096	-22.688	Average
4	0.240	46.782	0.066	46.848	62.096	-15.248	QP
5	0.348	22.691	0.058	22.749	49.010	-26.261	Average
6	0.348	37.947	0.058	38.005	59.010	-21.005	QP
7	1.786	24.612	-0.005	24.607	46.000	-21.393	Average
8	1.786	36.186	-0.005	36.181	56.000	-19.819	QP
9	4.216	29.010	-0.034	28.976	46.000	-17.024	Average
10	4.216	36.541	-0.034	36.507	56.000	-19.493	QP
11	16.050	41.624	0.027	41.651	50.000	-8.349	Average
12	16.050	48.921	0.027	48.948	60.000	-11.052	QP

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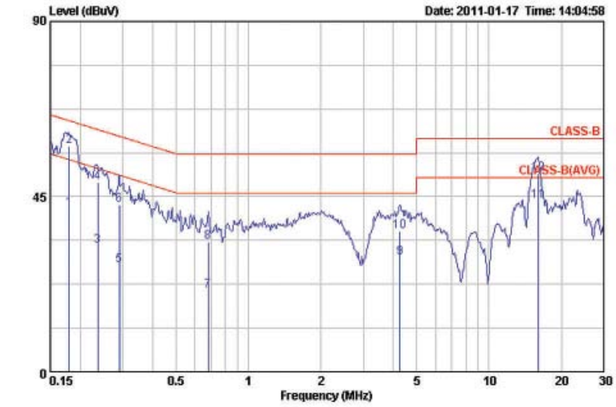
Fig 20. 230 V, 65 W TEA1738LT/T and TEA1703 demo board phase N



Item	Freq	Read Value	Factor	Result	Limit	Margin	Remark
	MHz	dBuV	dB	dBuV	dBuV	dBuV	
1	0.179	41.795	0.024	41.819	54.523	-12.704	Average
2	0.179	57.819	0.024	57.843	64.523	-6.680	QP
3	0.237	32.271	0.014	32.285	52.208	-19.923	Average
4	0.237	48.502	0.014	48.516	62.208	-13.692	QP
5	0.290	27.326	0.007	27.333	50.522	-23.189	Average
6	0.290	42.795	0.007	42.802	60.522	-17.720	QP
7	0.682	20.820	-0.022	20.798	46.000	-25.202	Average
8	0.682	33.328	-0.022	33.306	56.000	-22.694	QP
9	4.273	29.363	-0.068	29.295	46.000	-16.705	Average
10	4.273	36.293	-0.068	36.225	56.000	-19.775	QP
11	16.070	43.720	0.203	43.923	50.000	-6.077	Average
12	16.070	50.755	0.203	50.958	60.000	-9.042	QP

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Fig 21. 230 V, 65 W TEA1738LT/T and TEA1703 demo board phase L

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4. Schematic 65 W TEA1738LT/T and TEA1703 reference board

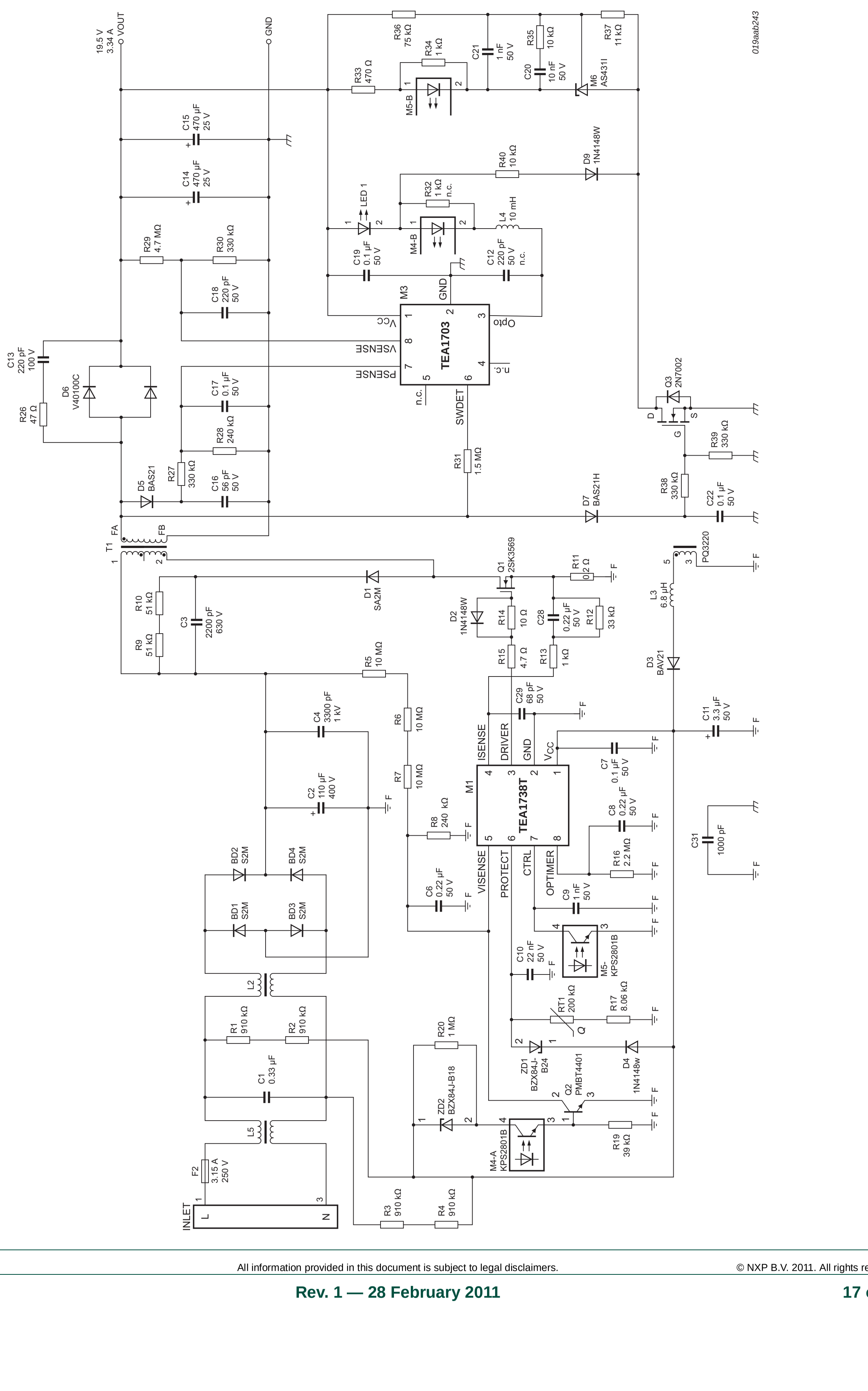

Fig 22. Schematic 65 W TEA1738LT/T and TEA1703 reference board

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5. Bill of materials

5.1 Component s list

Table 12. Bill of materials

Reference	Value	Description	Package
R1	910 kΩ; 1 %; 4 W	resistor; thin film chip	SMD 1206
R2	910 kΩ; 1 %; 4 W	resistor; thin film chip	SMD 1206
R3	910 kΩ; 1 %; 4 W	resistor; thin film chip	SMD 1206
R4	910 kΩ; 1 %; 4 W	resistor; thin film chip	SMD 1206
R5	10 MΩ; 1 %; 4 W	resistor; thin film chip	SMD 1206
R6	10 MΩ; 1 %; 4 W	resistor; thin film chip	SMD 1206
R7	10 MΩ; 1 %; 4 W	resistor; thin film chip	SMD 1206
R8	240 kΩ; 5 %; 8 W	resistor; thin film chip	SMD 0805
R9	51 kΩ; 1 %; 1 W	resistor; thin film chip	SMD 1206
R10	51 kΩ; 1 %; 1 W	resistor; thin film chip	SMD 1206
R11	0.2 Ω; 1 %; 1 W	resistor; MOF	axial lead
R12	33 kΩ; 1 %; 10 W	resistor; thin film chip	SMD 0603
R13	1 kΩ; 1 %; 1 W	resistor; thin film chip	SMD 0603
R14	10 Ω; 5 %; 8 W	resistor; thin film chip	SMD 0603
R15	4.7 Ω; 5 %; 8 W	resistor; thin film chip	SMD 0805
R16	2.2 MΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R17	8.06 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R19	39 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R20	1 MΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R26	4.7 Ω; 5 %; 8 W	resistor; thin film chip	SMD 0603
R27	330 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R28	240 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R29	4.7 MΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R30	330 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R31	1.5 MΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R32	-	not mounted	-
R33	470 Ω; 5 %; 8 W	resistor; thin film chip	SMD 0603
R34	1 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R35	10 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R36	75 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R37	11 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R38	330 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R39	330 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
R40	10 kΩ; 5 %; 10 W	resistor; thin film chip	SMD 0603
RT1	200 kΩ; 5 %	NTC resistor	SMD 0805
C1	330 μF; 400 V; 105 °C	X2-cap; Arcotronics	15 mm × 14.5 mm × 8.5 mm
C2	110 μF; 400 V; 105 °C	electric; ±20 %, NCC	50 mm × 11.5 mm

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Table 12. Bill of materials *...continued*

Reference	Value	Description	Package
C3	2200 pF; 630 V	MLCC; Z5U	SMD 1206
C4	3300 pF; 1 kV	MLCC; Z5U	SMD 1206
C6	0.22 μF; 50 V	±10 %; MLCC; X7R; lead free	SMD 0603
C7	0.1 μF; 50 V	±10 %; MLCC; X7R	SMD 0603
C8	0.22 μF; 50 V	±10 %; MLCC; X7R; lead free	SMD 0603
C9	1 nF; 50 V	±10 %; MLCC; X7R	SMD 0603
C10	22 nF; 50 V	±5 %; MLCC; X7R	SMD 0603
C11	3.3 μF; 50 V; 105 °C	electric, ±20 %; KY/NCC	5 mm × 11.5 mm
C12	-	not mounted	-
C13	220 pF; 100 V	±5 %; MLCC; NPO; KZH/NCC	SMD 0805
C14	470 μF; 50 V; 105 °C	electric, ±20 %; KZH/NCC	radial lead; 10 mm × 12.5 mm
C15	470 μF; 50 V; 105 °C	electric, ±20 %; KZH/NCC	radial lead; 10 mm × 12.5 mm
C16	56 pF; 50 V	±5 %; MLCC; X7R	SMD 0603
C17	0.1 μF; 50 V	±10 %; MLCC; X7R	SMD 0603
C18	220 pF; 50 V	±5 %; MLCC; X7R	SMD 0603
C19	0.1 μF; 50 V	±10 %; MLCC; X7R	SMD 0603
C20	10 nF; 50 V	±10 %; MLCC; X7R	SMD 0603
C21	1 nF; 50 V	±10 %; MLCC; X7R	SMD 0603
C22	0.1 nF; 50 V	±10 %; MLCC; X7R	SMD 0603
C28	0.22 nF; 50 V	±10 %; MLCC; X7R; lead free	SMD 0603
C31	1000 pF; 400 V (AC)	Y1-cap	-
BD1	2 A; 1 kV	general purpose diode; S2M; trr = 2 μS; MCCsemi	SMB
BD2	2 A; 1 kV	general purpose diode; S2M; trr = 2 μS; MCCsemi	SMB
BD3	2 A; 1 kV	general purpose diode; S2M; trr = 2 μS; MCCsemi	SMB
BD4	2 A; 1 kV	general purpose diode; S2M; trr = 2 μS; MCCsemi	SMB
D1	2 A; 1 kV	general purpose diode; S2M; trr = 2 μS; MCCsemi	SMT SMB
D2	0.15 A; 100 V	switching diode; 1N4148W; trr = 4 nS	SMT SOD123
D3	0.2 A; 250 V	diode; BAV21W/Vishay; trr = 50 nS	SMT SOD123
D4	0.15 A; 100 V	switching diode; 1N4148W; trr = 4 nS	SMT SOD123
D5	0.2 A; 250 V	diode; BAV21W/Vishay; trr = 50 nS	SMT SOD123
D6	40 A; 100 V	Schottky; V40100C; Vishay	TO220AB
D7	0.2 A; 250 V	diode; BAV21H/Vishay; trr = 50 nS; NXP	SMT SOD123
D8	0.15 A; 100 V	switching diode; 1N4148W; trr = 4 nS	SMT SOD123
D9	0.15 A; 100 V	switching diode; 1N4148W; trr = 4 nS	SMT SOD123
ZD1	24 V	Zener diode; BZX84J-B24; Vz = 23.5 V to 24.5 V; zt = 5 mA; Ir = 50 nA	SMT SOD323F
ZD2	24 V	Zener diode; BZX84J-B18; Vz = 17.6 V to 18.4 V; zt = 5 mA; Ir = 50 nA	SMT SOD323F

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Table 12. Bill of materials *...continued*

Reference	Value	Description	Package
ZD3	-	not mounted	-
Q1	15 A; 600 V; 0.5 Ω	MOSFET; n-channel; 2SK3569/Toshiba; R_{DSon} = 0.5 Ω; $V_{GS(on)}$ = 3 V; ID = 15 A; C_{iss} = 1600 pF; V_{DS} = 600 V; V_{GS} = ±30 V	SMT TO220
Q2	PMBT4401	NPN transistor 80 hFE; VCEO = 40 V; I_C = 600 mA	SMT TO220
Q3	15 A; 600 V; 0.5 Ω	MOSFET; n-channel; 2SK3569/Toshiba; R_{DSon} = 5.3 Ω; $V_{GS(on)}$ = 1 V; ID = 300 mA; C_{iss} = 40 pF; V_{DS} =6 0V ; V_{GS} = ±30 V	SMT SOT23
M1	TEA1738LT/T	GreenChip SMPS control IC; NXP Semiconductors	SO8
M3	TEA1703	GreenChip SMPS control IC; NXP Semiconductors	SO8
M4	KPS2801B	optocoupler; CTR = 130 % ~ 260 %; 1-channel; COSMO	4-pin SOP
M5	KPS2801B	optocoupler; CTR = 130 % ~ 260 %; 1-channel; COSMO	4-pin SOP
M6	AS431I	adjustable precision shunt regulator BCD	SMT SOT23
T1	Lp = 400 μH	transformer; Np : Ns : Naux = 36 : 6 : 6; JPP44A; A-core	ATQ28/11.2D
L2	choke	N1 : N2 = 52 : 52; JPH10F; A-core	D = 0.45 mm; 14 mm × 5–9C
L3	6.8 μHc	hoke; ±10 %; 275 μA; DCR = 1 Ω; WIS252018N-6R8K; Mingstar	SMT 2.5 mm × 2m m × 1.8 mm
L4	10 μH	choke	DIP
L5	choke	N1 : N2 = 7 : 7; JPZ10K; A-core	D = 0.45 mm; T8 mm × 4m m × 4–9C
F2	T3.15 A; 250 V	fuse; f7use; DIP; MST	8.35 mm × 4.3 mm × 7.7 mm
LED1	LED 5.0 V; blue	M02-0603QBC; Vr = 5 V; IF = 30 mA; Hi-light	SMD 0603; 1.6 mm × 0.8 mm × 0.8 mm
Inlet	inlet	-	2P
Cable	cable	16AWG/1571	L = 1200 mm

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6. T ransformer specification

6.1 T ransformer schematic diagram

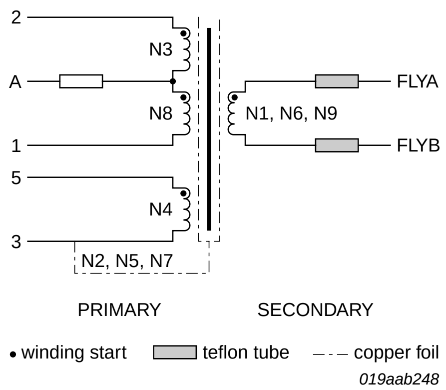

Fig 23. Transformer winding diagram

Table 13. Winding construction

Number	Layers	Turns	Wires	Copper/diameter	Type
9	secondary	6	2	0.32	triso
8c	primary	6	1	0.35	enamelled
8b	primary	6	1	0.35	enamelled
8a	primary	6	1	0.35	enamelled
7	Cu oil f	-	-	-	-
6	secondary	6	2	0.35	triso
5	Cu oil f	-	-	-	-
4	auxiliary	6	2	0.32	enamelled
3c	primary	6	1	0.15	enamelled
3b	primary	6	1	0.35	enamelled
3a	primary	6	1	0.35	enamelled
2	Cu oil f	-	-	-	-
1	secondary	6	2	0.32	triso

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6.2 W inding specification

Table 14. Winding table

Winding order		Pin		Wire	Turns	Layers	Turn/ Layer	Insulation after winding
		Start	Finish					
1	N1	FA	FB	0.32 mm ∅ × 2 mm[1]	6	1	6	tape 1 Ts[3]
2	S1	-	3[6]	0.025 mm × 7 mm[2]	1	1	1	tape 1 Ts[3]
3	N3	2	A	0.35 mm ∅ × 2 mm	18	3	6/3	tape 1 Ts[3]
4	N4	5	3[6]	0.15 mm ∅ × 2 mm	6	1	6	tape 1 Ts[3][5]
5	S2	-	3	0.025 mm × 7 mm[2]	1	1	1	tape 1 Ts[3]
6	N6	FA	FB	0.32 mm ∅ × 2 mm[1]	6	1	6	tape 1 Ts[3]
7	S3	-	3[6]	0.025 mm × 7 mm[2]	1	1	1	tape 1 Ts[3]
8	N8	A[4]	1	0.35 mm ∅ × 2 mm	18	3	6/3	tape 1 Ts[3]
9	N9	FA	FB	0.3 mm ∅ × 2 mm[1]	6	1	6	tape 1 Ts[3]

[1] Furkukawa.

[2] Copper foil.

[3] Spread winding.

[4] Intermediate connection A is not connected to a pin.

[5] Insulation tape 3M #1350 or #1298.

[6] Copper foil connected to pin 3 using 0.25 ∅ lead wire.

6.3 Electrical characteristics

Table 15. Electrical characteristics

Description	Pin	Specification	Remark
Inductance	1 to 2	700 μH ± 5 %	65 kHz; 1 V

6.4 Core and bobbin

Core: ATQ28/11.2D; A-Core, JPP44A

6.5 Marking

Main board: APBADC054

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7. Layout of the 65 W TEA1738LT/T and TEA1703 reference board

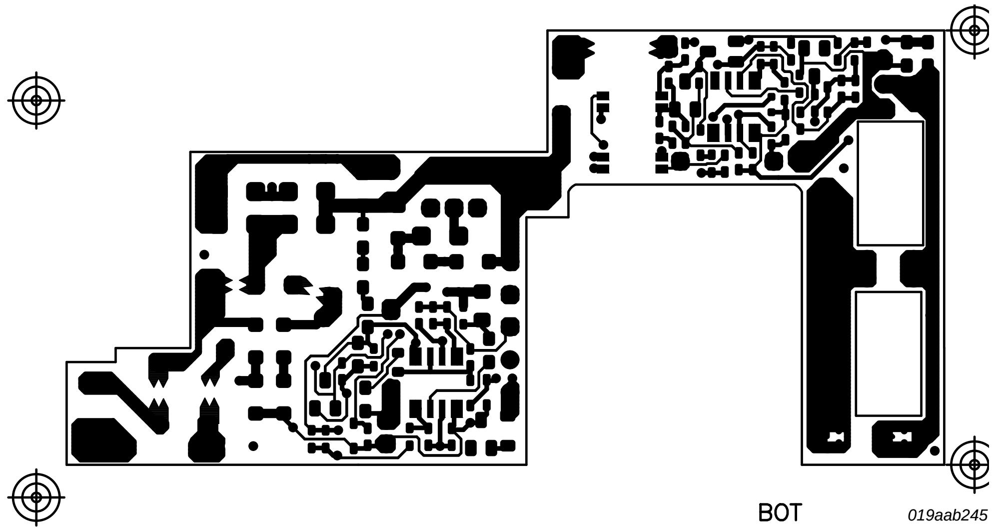

Fig 24. Copper layout bottom side (top view)

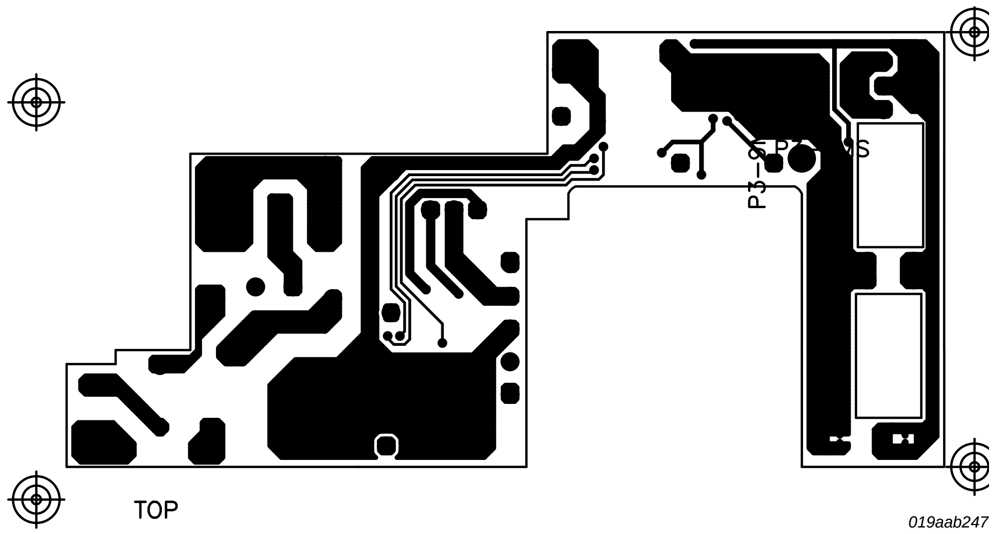

Fig 25. Copper layout top side (top view)

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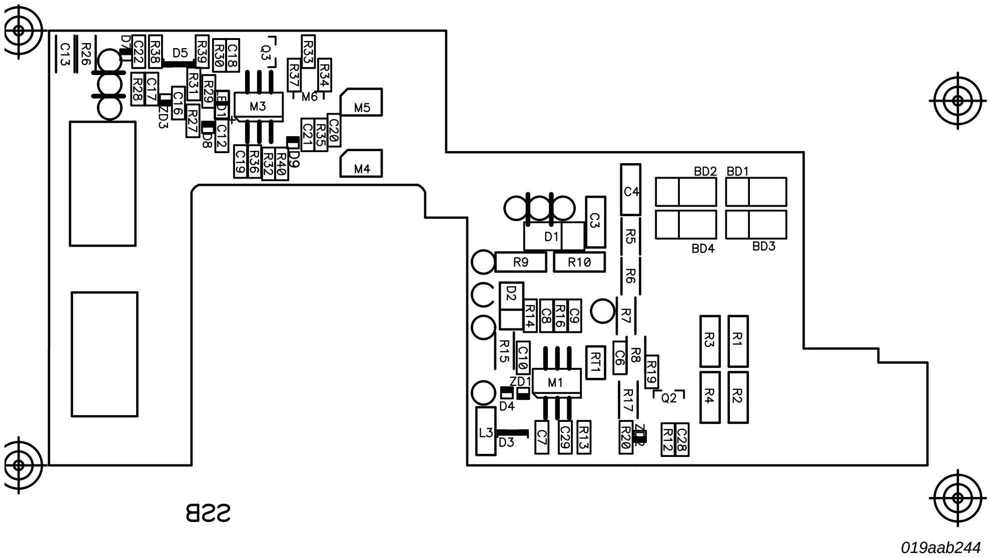

Fig 26. Component placement bottom side (bottom view)

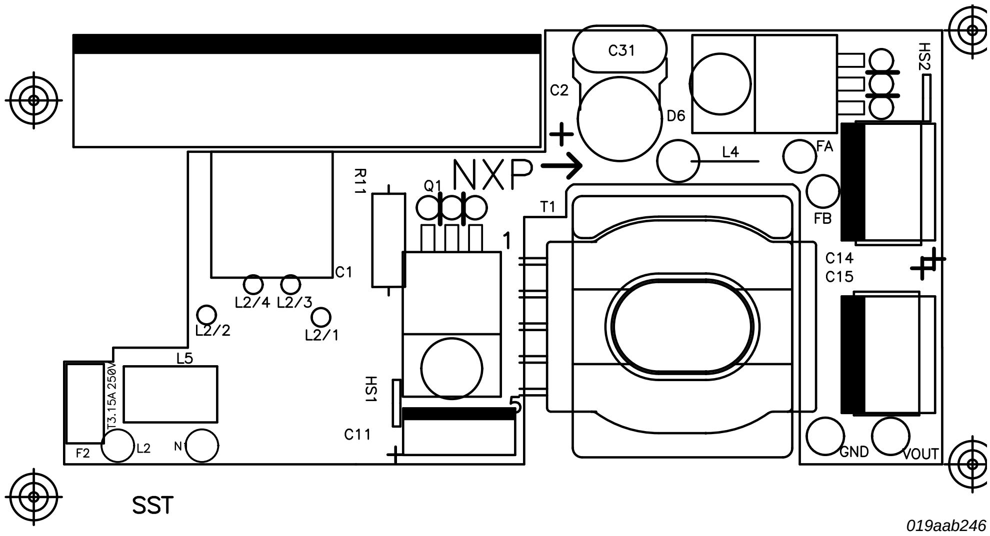

Fig 27. Component placement top side (top view)

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8. Alternative circuit options

8.1 Changing the output voltage

By changing the following components, the output voltage can be changed (±30 %). Refer to the *TEA1738(L)T application note* for additional information on this topic. Make sure that the Aux voltage remains within its operation limits (12.2 V – 30 V typical) and is high enough to start up (20.6 V typical).

R23/R24

The resistor divider R36 and R37 determine the output voltage based on $V_o = 2.5\ V \times (R36 + R37) / (R37)$.

C13/C14

The voltage rating of these electrolytic capacitors must be chosen to be higher than the output voltage. Decrease the value of the capacitors for applications with a lower output current.

8.2 TEA1703 adjustments

In this design the following items can be improved by changing the value of the inductor L4 to 4m7H. Currently the current through opto LED M4 is too low.

- Output power level threshold to enter Standby mode is very low
- The V_{CC} clamp cannot sink enough current for high mains. This causes the TEA1738 to restart in Standby mode at 264 V; 60 Hz. This behavior is not recommended

The minimum output voltage in Standby mode can be adjusted using resistor R30. By increasing resistor R30 from 330 kΩ to 420 kΩ, an additional < 2 mW can be saved and the minimum output voltage will drop to 9 V.

Refer to the TEA1703 application note for adjustment information.

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