UM2147

4K × 1 High Speed NMOS SRAM

Features

- 45 ns maximum access time
- No clocks or strobes required
- Automatic $\overline{CE}$ power down
- Identical cycle and access times
- Single +5V supply (± 10%)
- Pinout and function compatible to SY2147
- Total TTL compatible: All inputs and outputs
- Separate data input and output
- High density 18-pin package
- Three-state output

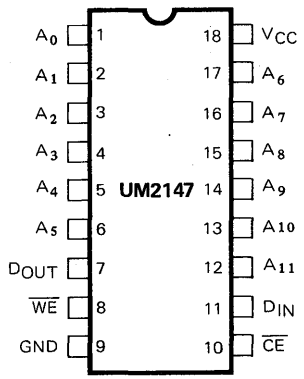
General Description

The UMC UM2147 is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using UMC's new scaled N-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

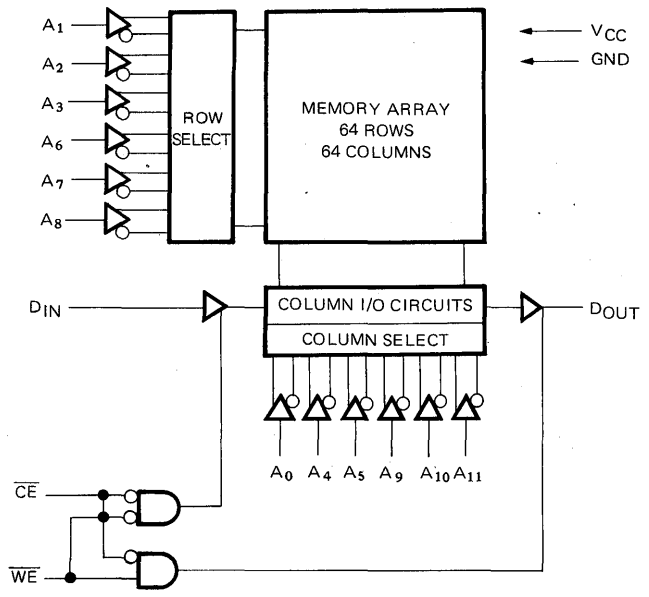
The UM2147 offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus deselecting the UM2147 the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remain high. This unique feature provides system level power savings as much as 80%.

The UM2147 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 85°C
Storage Temperature . . . . . −65°C to 150°C
Voltage on Any Pin with Respect to Ground . . . . . −3.5V to +7V
Power Dissipation 1.2W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10% Unless otherwise specified) (Note 8)

Symbol	Parameter	2147 /-1/-2		2147 L/L-1		Units	Conditions
		Min.	Max.	Min.	Max.		
I_{LI}	Input Load Current (All input pins)		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50		50	µA	$\overline{CE}$ = V_{IH}, V_{CC} = Max. V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		150		115	mA	T_A = 25°C; V_{CC} = Max. $\overline{CE}$ = V_{IL} Outputs Open
			160		125	mA	T_A = 0°C; V_{CC} = Max. $\overline{CE}$ = V_{IL} Outputs Open
I_{SB}	Standby Current		20		10	mA	V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}
I_{PO}	Peak Power-on Current (Note 9)		50		30	mA	V_{CC} = Gnd to V_{CC} Min; $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	−3.0	0.8	−3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −4.0mA

Capacitance

(T_A=25°C, f = 1.0 MHz)

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		6	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ±10% Unless otherwise specified) (Note 8, 10)

READ CYCLE

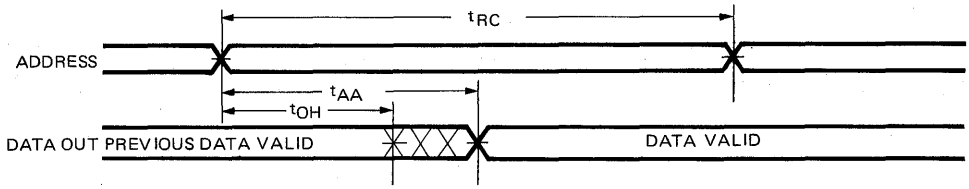
Symbol	Parameter	2147/L		2147-1/L-1		2147–2		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	70		55		45		ns	
t_{AA}	Address Access Time		70		55		45	ns	
t_{ACE1}	Chip Enable Access Time		70		55		45	ns	1
t_{ACE2}	Chip Enable Access Time		80		65		45	ns	2
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	10		10		5		ns	7
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	30	0	30	ns	7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		20		20	ns	

WRITE CYCLE

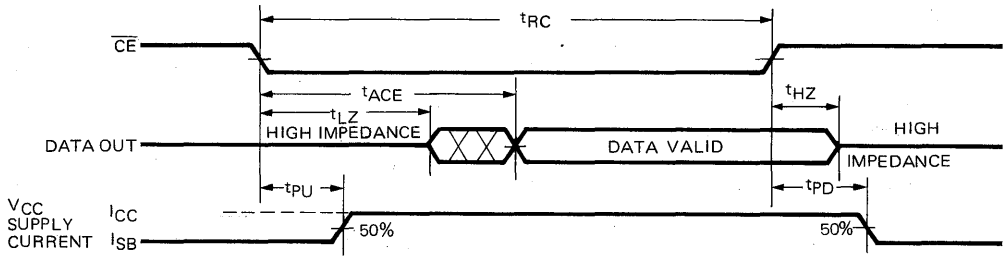
t_{WC}	Write Cycle Time	70		55		45		ns	
t_{CW}	Chip Enabled to End of Write	55		45		45		ns	
t_{AW}	Address Valid to End of Write	55		45		45		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	40		25		25		ns	
t_{WR}	Write Recovery Time	15		10		0		ns	
t_{DW}	Data Valid to End of Write	30		25		25		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	35	0	25	0	25	ns	7
t_{OW}	Output Active from End of Write	0		0		0		ns	7

Timing Diagrams

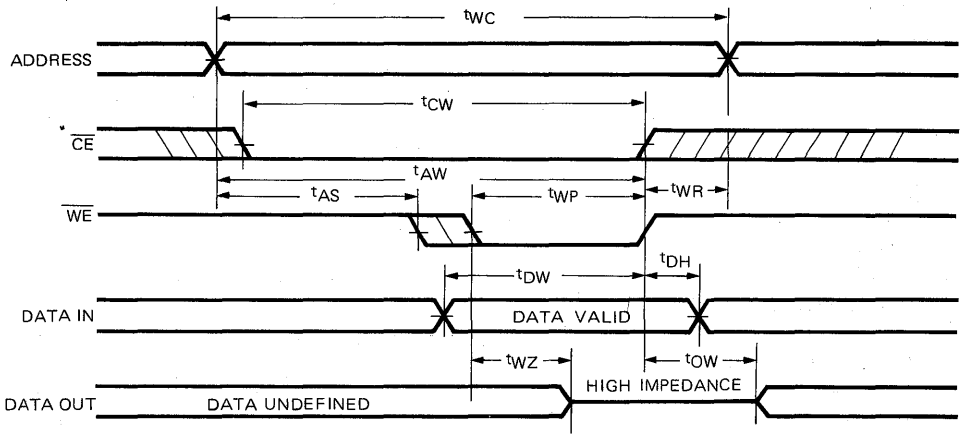
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)



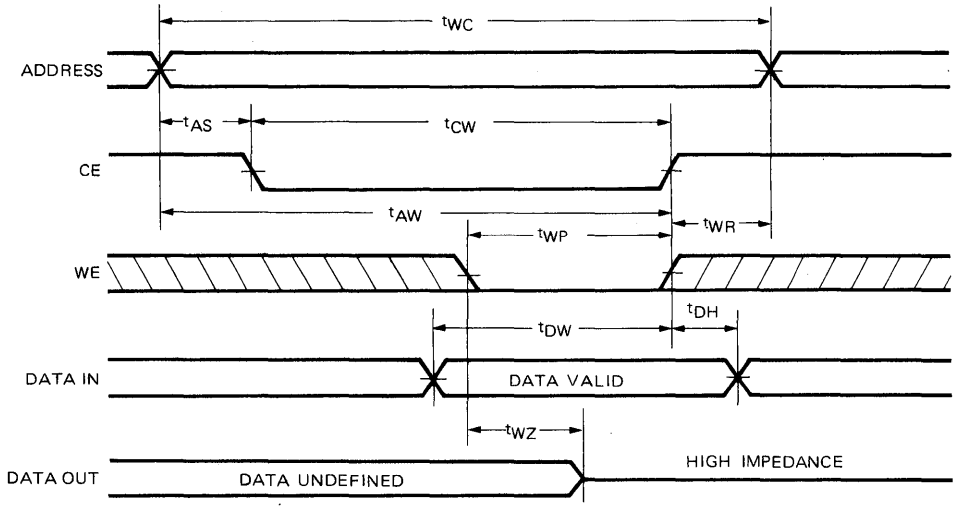
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 6)



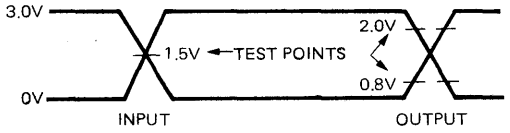
Notes:

1. Chip deselected for greater than 55 ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is Ons, the chip is by definition selected and access occurs according to Read Cycle No. 1.).
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CE} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
6. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
7. Transition is measured ± 500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
9. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.
10. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED) (NOTE 6)

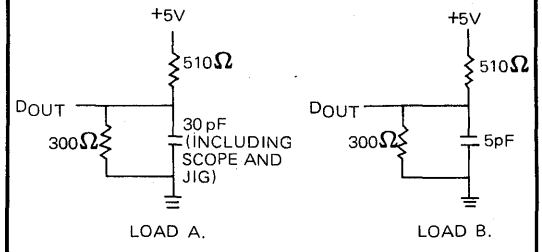


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Ordering Information

Part Number	Access Time (Max.)	Operating Current (Max.)	Stand by Current (Max.)	Package Type
UM2147	70 ns	160 mA	20 mA	Plastic
UM2147–1	55 ns	180 mA	30 mA	Plastic
UM2147–2	45 ns	180 mA	30 mA	Plastic
UM2147L	70 ns	140 mA	10 mA	Plastic
UM2147L–1	55 ns	125 mA	15 mA	Plastic