1K × 4 High Speed NMOS SRAM

Features

- 45 ns maximum address access
- Fully static operation:
  No clocks or strobes required
- Fast chip select access time: 20ns max.
- Identical cycle and access times
- Single +5V supply
- Industry standard 2114 pinout
- Totally TTL compatible:
  All inputs and outputs
- Common data input and outputs
- High density 18-pin package
- Three-state output

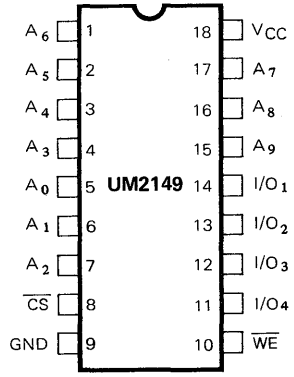
General Description

The UMC UM2149 is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using UMC's new N-channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

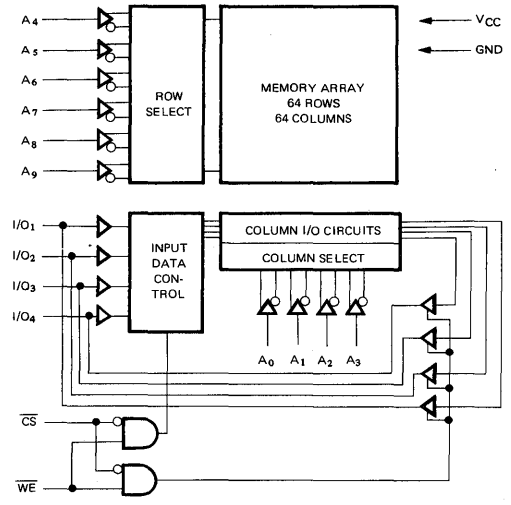
The UM2149 offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

The UM2149 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Temperature Under Bias . . . . . –10°C to 85°C
Storage Temperature . . . . . –65°C to 150°C
Voltage on Any Pin with Respect to Ground . . . . . –3.5V to +7V
Power Dissipation 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10% Unless otherwise specified) (Note 8)

Symbol	Parameter	2149/-1/-2		2149L/L-1		Units	Conditions	
		Min.	Max.	Min.	Max.			
I_{LI}	Input Load Current (All input pins)		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}	
$\lvert I_{LO} \rvert$	Output Leakage Current		50		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max. V_{OUT} = Gnd to 4.5V	
I_{CC}	Power Supply Current		140		115	mA	T_A = 25°C	V_{CC} = Max, $\overline{CS}$ = V_{IL} Outputs Open
			150		125	mA	T_A = 0°C	
V_{IL}	Input Low Voltage	–0.3	0.8	–0.3	0.8	V		
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V		
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8 mA	
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = –4.0 mA	
I_{OS}	Output Short Circuit Current		±200		±200	mA	V_{OUT} = GND to V_{CC} (Note 7)	

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10% Unless otherwise specified) (Note 6, 8)

READ CYCLE

Symbol	Parameter	2149		2149–1		2149–2		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	70		55		45		ns	
t_{AA}	Address Access Time		70		55		45	ns	
t_{ACS}	Chip Select Access Time		30		25		20	ns	
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	5		5		5		ns	Note 5
t_{HZ}	Chip Deselection to Output in High Z	0	15	0	15	0	15	ns	Note 5

WRITE CYCLE

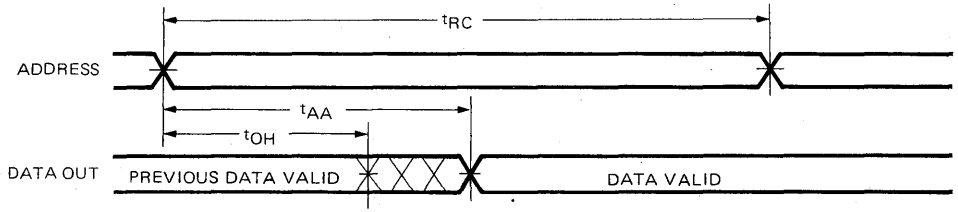
t_{WC}	Write Cycle Time	70		55		45		ns	
t_{CW}	Chip Selection to End of Write	65		50		40		ns	
t_{AW}	Address Valid to End of Write	65		50		40		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	50		40		35		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	25		20		20		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	25	0	20	0	15	ns	Note 5
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 5

(See following page for notes)

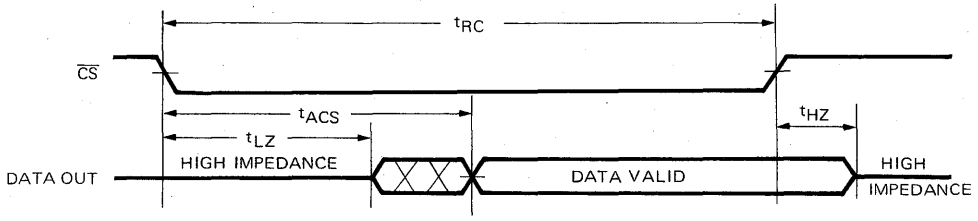
SRAM

Timing Diagrams

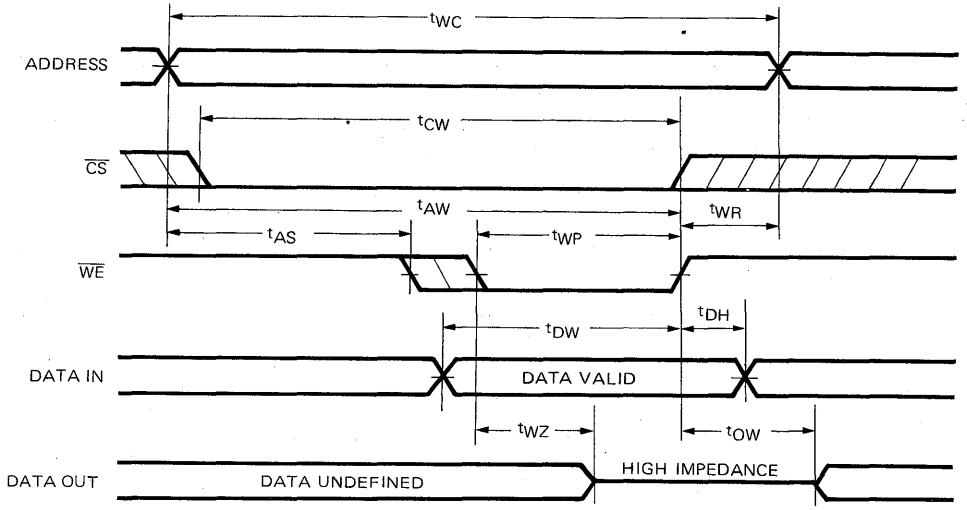
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)



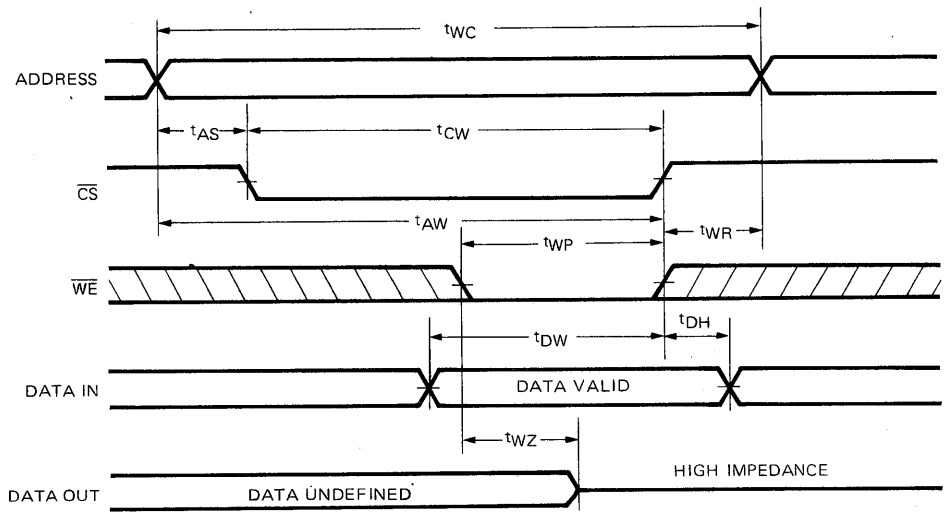
WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 4)



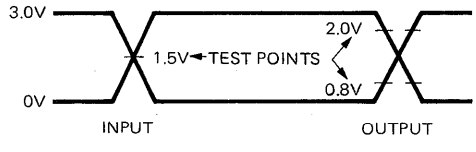
Notes:

1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid.
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ± 500 mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
7. Duration not to exceed one minute.
8. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 ($\overline{CS}$ controlled) (note 4)

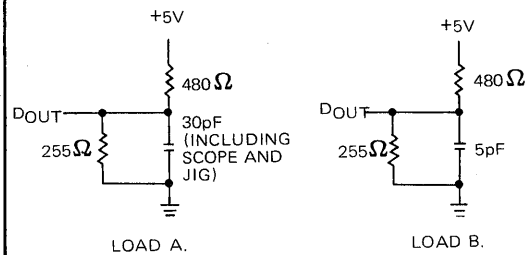


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Ordering Information

Order Number	Access Time (Max.)	Supply Current (Max.)	Package Type
UM2149	70 ns	150 mA	Plastic
UM2149–1	55 ns	150 mA	Plastic
UM2149–2	45 ns	150 mA	Plastic
UM2149L	70 ns	125 mA	plastic
UM2149L–1	55 ns	125 mA	Plastic