



UM23128 / UM23128A

16K × 8 NMOS ROM

Mask ROM

Features

- EPROM pin compatible
- 16,384 x 8 bit organization
- single +5 volt supply
- Access time — 200/300/450 ns (max)
- Totally static operation
- Completely TTL compatible
- 28 pin JEDEC approved pinout
- UM23128A — automatic power down (\overline{CE})
 - output enable function (\overline{OE})
 - one programmable chip select (CS)
- UM23128 — non power down version
 - three programmable chip selects (CS)
- Three state outputs for wire-OR expansion
- EPROMS accepted as program data input

Description

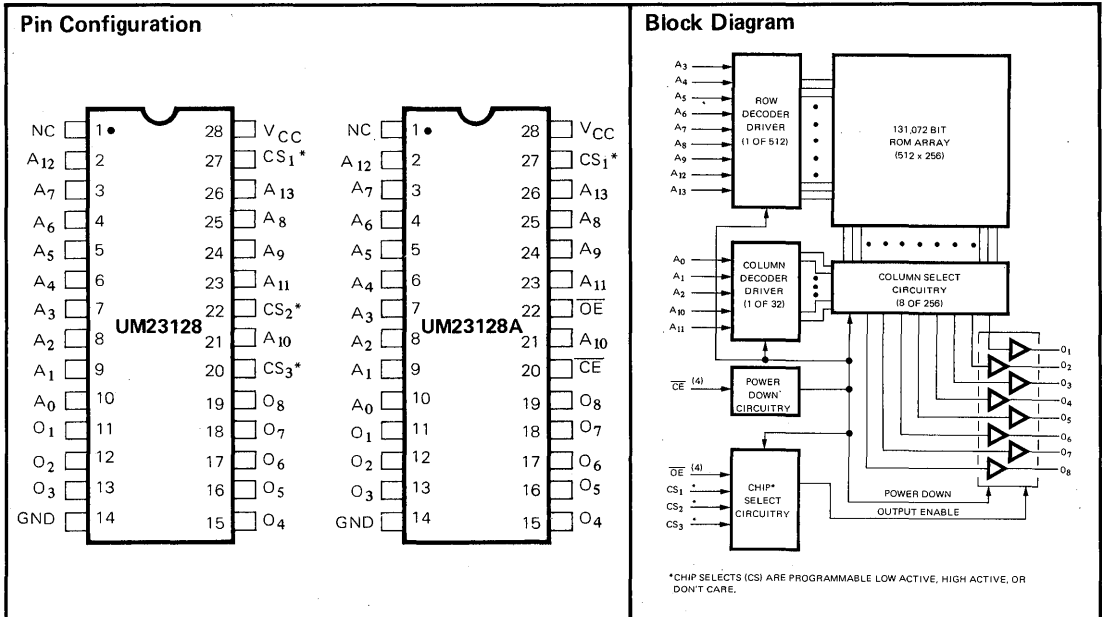
The UM23128 and UM23128A high performance Read Only Memories are organized 16,384 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 128K ROMs.

The UM23128 offers the simplest operation (no power down.) Its three programmable chip selects allow up to eight 128K ROMs to be OR-tied without external decoding.

The UM23128A offers an automatic power down feature.

Power down is controlled by the Chip Enable (\overline{CE}) input. When \overline{CE} goes high, the device will automatically power down and remain in a low power standby mode as long as \overline{CE} remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the UM23128A is the Output Enable (\overline{OE}) function. This eliminates bus contention in multiple bus microprocessor systems. The programmable chip select allows two 128K ROMs to be OR-tied without external decoding.

Both the UM23128 and UM23128A are pin compatible with EPROMs thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.



Absolute Maximum Ratings*

Temperature Under Bias	-10°C to 85°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-3.5V to +7V
Power Dissipation	1.0W
Electrostatic Discharge Rating (ESD)**	
Inputs to Ground	± 2000V

**Test Condition: MIL-STD-883B Method 3015.1

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	$I_{OH} = -1.0\text{ mA}$
V_{OL}	Output LOW Level			0.4	V	$I_{OL} = 3.2\text{ mA}$
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	-3.0		0.8	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0\text{V to } V_{CC}$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0\text{V to } V_{CC}$
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			10	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance

($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	$V_{IN} = 0\text{V}$
C_O	Output Capacitance		5	pf	$V_{OUT} = 0\text{V}$

Note: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

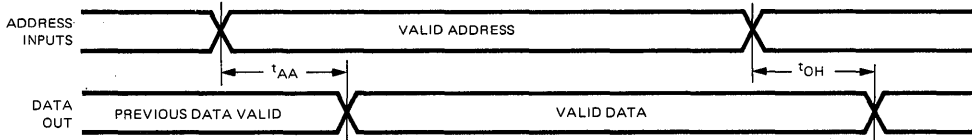
($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$) (Note 7)

Symbol	Parameter	UM23128-2 UM23128A-2		UM23128-1 UM23128A-1		UM23128 UM23128A		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Output LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		100		120		150	ns	Note 4

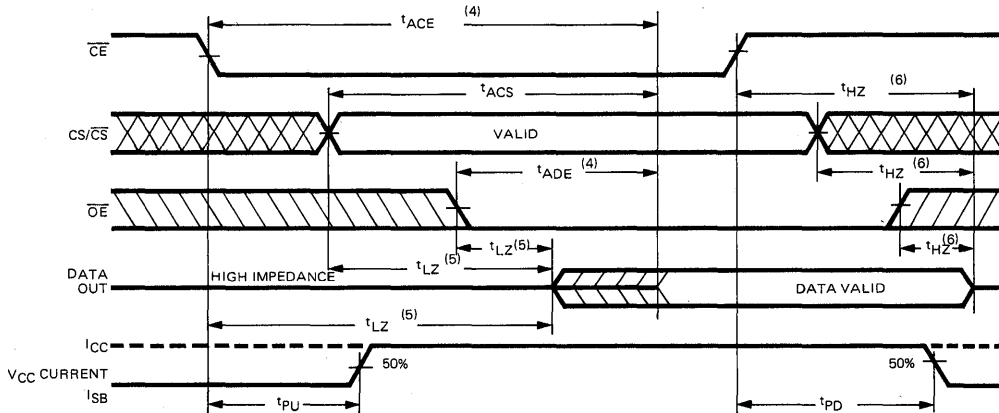
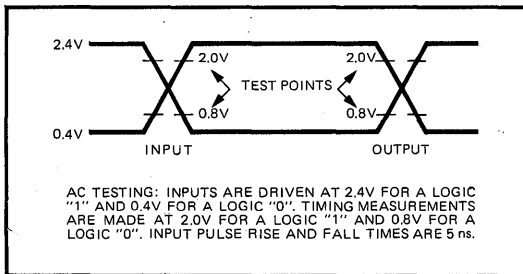
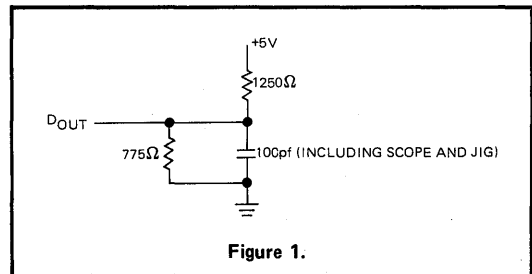
Notes:

1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $CE = 2.0\text{V}$.
3. For a duration not to exceed one second with $V_{OUT} = 0\text{V}$
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from \overline{CE} and \overline{OE} going low and CS going active, whichever occurs last.
6. Output high impedance delay (t_{HZ}) is measured from either \overline{CE} or \overline{OE} going high or CS going inactive, whichever occurs first.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Timing Diagrams

 Propagation Delay from Address ($\overline{CE} = \overline{OE} = \text{LOW}$, $\text{CS}/\overline{\text{CS}} = \text{Active}$)


Propagation Delay from Chip Enable, Chip Select (Address Valid)


A.C. Testing Input, Output Waveform

A.C. Testing Load Circuit

Programming Instructions

All UMC Read Only Memories (ROM) utilize computer assisted techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to UMC in a number of different ways. UMC can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your UMC sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Ordering Information

Part Number	Access Time	Operating Current	Standby Current	Package Type
UM23128	450 ns	100 mA	N.A.	Plastic
UM23128-1	300 ns	100 mA	N.A.	Plastic
UM23128-2	200 ns	100 mA	N.A.	Plastic
UM23128A	450 ns	100 mA	10 mA	Plastic
UM23128A-1	300 ns	100 mA	10 mA	Plastic
UM23128A-2	200 ns	100 mA	10 mA	Plastic

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