UM23256/UM23256A

32K × 8 NMOS ROM

Features

- EPROM pin compatible
- 32,768 x 8 bit organization
- Single +5 volt supply
- Access time–200/300/450ns (max)
- Totally static operation
- Completely TTL compatible
- 28 Pin JEDEC approved pinout
- UM23256A– automatic power down ($\overline{CE}$)
  – output enable function ($\overline{OE}$)
- UM23256 – non power down version
  – two programmable chip selects (CS)
- Three state outputs for wire-OR expansion
- EPROMs accepted as program data input

General Description

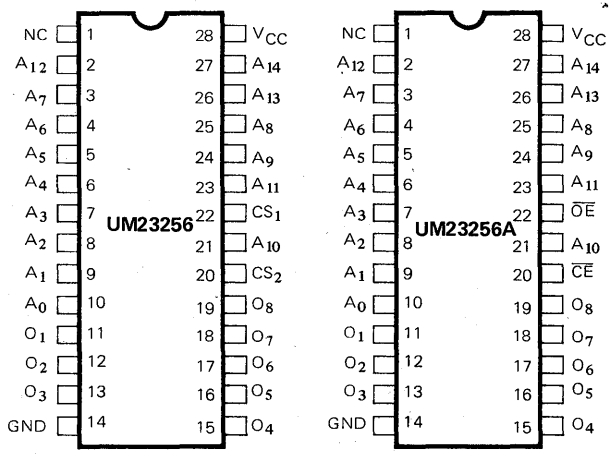
The UM23256 and UM23256A high performance Read Only Memories are organized 32,768 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 256K ROMs.

The UM23256 offers the simplest operation (no power down.) Its two programmable chip selects allow up to four 256K ROMs to be OR-tied without external decoding.

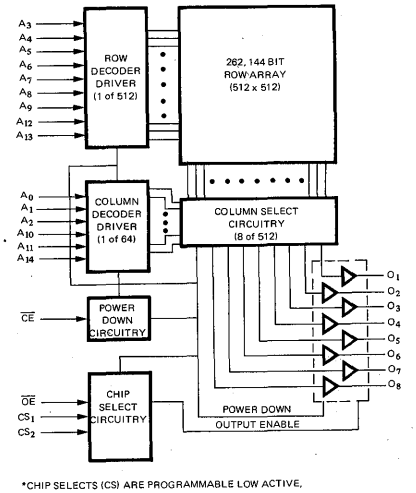
The UM23256A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power stand-by mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the UM23256A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems.

Both the UM23256 and UM23256A are pin compatible with EPROMs thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configuration



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DON'T CARE

Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 85°C

Storage Temperature . . . . . −65°C to 150°C

Voltage on Any Pin with Respect to Ground

. . . . . −3.5V to + 7V

Power Dissipation 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

(T_A = 0°C to + 70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	−3.0		0.8	V	
V_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			10	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = 0V
C_O	Output Capacitance		5	pf	V_{OUT} = 0V

Note: This parameter is periodically sampled and is not 100% tested.

A. C. Characteristics

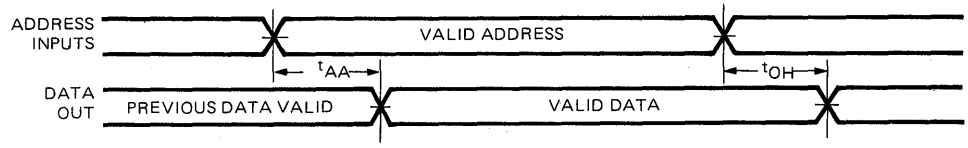
(T_A = 0°C to + 70°C, V_{CC} = +5V ± 10%) (Note 7)

Symbol	Parameter	23256-2 23256A-2		23256-1 23256A-1		23256 23256A		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Ouput LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		100		120		150	ns	Note 4

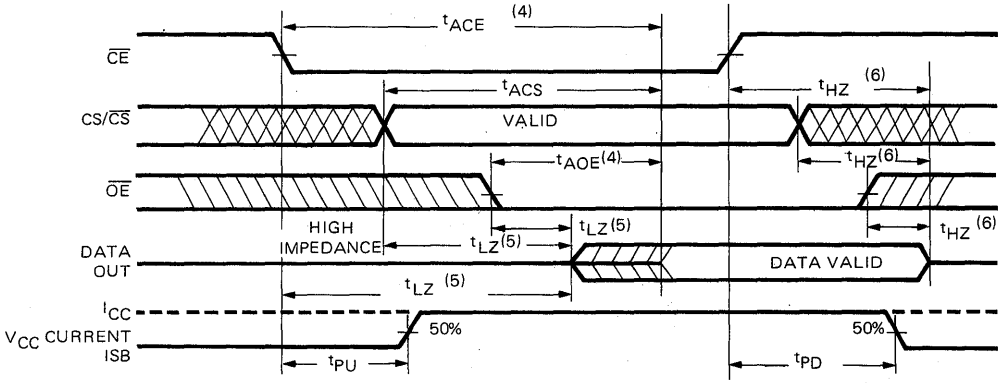
Notes:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V.
3. For a duration not to exceed one second with V_{OUT} = 0V.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low and CS going active, whichever occurs last.
6. Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Timing Diagrams

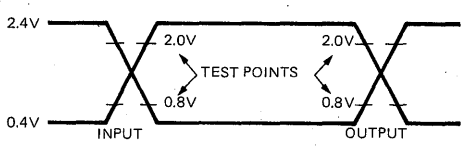
Propagation Delay from Address ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

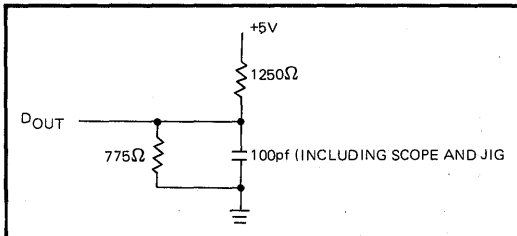


Figure 1.

Ordering Information

Part Number	Access Time	Operating Current	Standby Current	Package Type
UM23256	450 ns	100 mA	N.A.	Plastic
UM23256–1	300 ns	100 mA	N.A.	Plastic
UM23256–2	200 ns	100 mA	N.A.	Plastic
UM23256A	450 ns	100 mA	10 mA	Plastic
UM23256A–1	300 ns	100 mA	10 mA	Plastic
UM23256A–2	200 ns	100 mA	10 mA	Plastic