UM2364/UM2364A

8K × 8 NMOS ROM

Features

- 8192 x 8 Bit organization
- Single +5 Volt Supply
- Access Time – 200/300/450 ns (max.)
- Totally static operation
- Completely TTL compatible
- 24 Pin JEDEC approved pinout
- UM2364A – Automatic power down ($\overline{CE}$)
- UM2364 – non power down version
  – programmable chip select (CS)
- Three state outputs for wire-OR expansion
- EPROMs accepted as program data input
- 2564 EPROM compatible

General Description

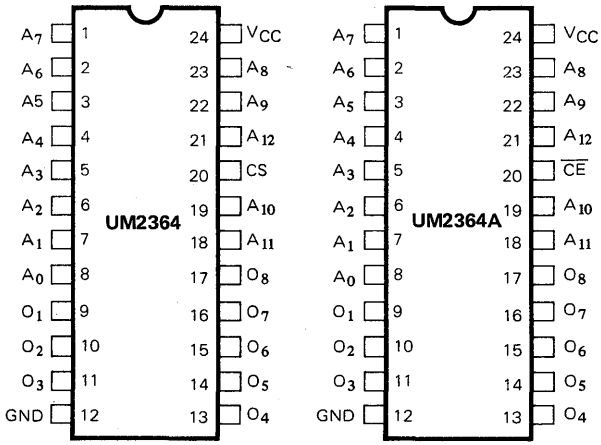
The UM2364 and UM2364A high performance Read Only Memories are organized 8192 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 24 pin 64K ROMs.

The UM2364 offers the simplest operation (no power down.) Its programmable chip select allows two 64K ROMs to be OR-tied without external decoding.

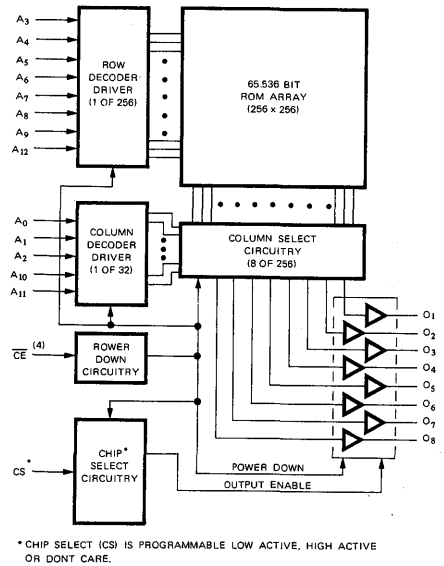
The UM2364A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%.

Both the UM2364 and UM2364A are pin compatible with the 2564 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configuration



Block Diagram



*CHIP SELECT (CS) IS PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DONT CARE.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . −10°C to 80°C
Storage Temperature . . . . . −65°C to 150°C
Voltage on Any Pin with Respect to Ground . . . . . −0.5V to +7V
Power Dissipation 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	−0.5		0.8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			12	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = 0V
C_O	Output Capacitance		5	pf	V_{OUT} = 0V

Note: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

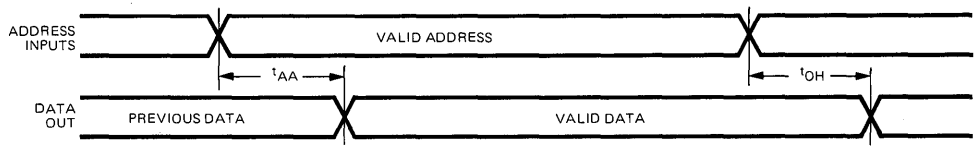
(T_A = 0°C to +70°C, V_{CC} = +5V ± 10%) (Note 7)

Symbol	Parameter	UM2364-2 UM2364A-2		UM2364-1 UM2364A-1		UM2364 UM2364A		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{LZ}	Ouput LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		85		100		150	ns	Note 4

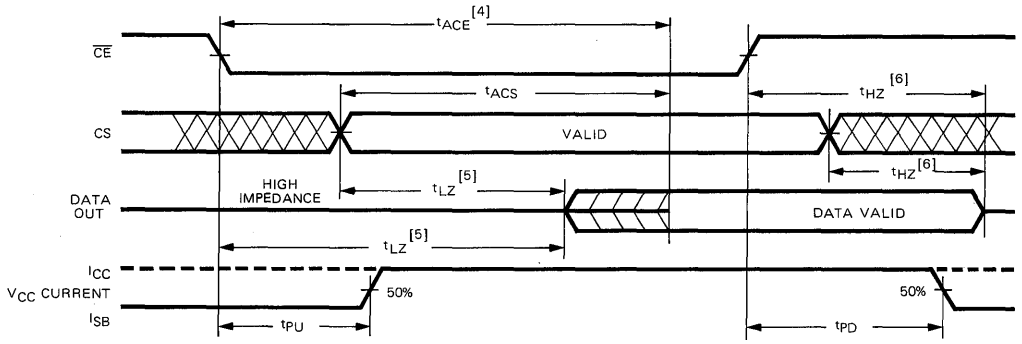
Notes:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V
3. For a duration not to exceed one second.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured form $\overline{CE}$ going low or CS going active.
6. Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ going high or CS going inactive.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Timing Diagrams

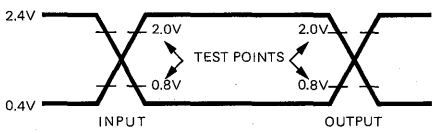
Propagation Delay from Address ($\overline{CE}$ LOW or CS = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

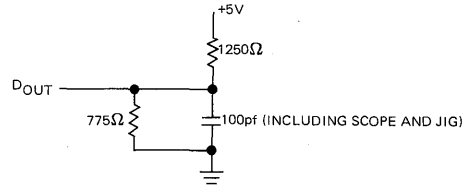


Figure 1.

Programming Instructions

All UMC Read Only Memories (ROM) utilize computer asided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to UMC in a number of different ways. UMC can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your UMC sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Package Availability

Ordering Information

Order Number	Access Time	Operating Current	Standby Current	Package Type
UM2364	450 ns	100 mA	N.A.*	Plastic
UM2364-1	300 ns	100 mA	N.A.	Plastic
UM2364-2	200 ns	100 mA	N.A.	Plastic
UM2364A	450 ns	100 mA	12mA	Plastic
UM2364A-1	300 ns	100 mA	12 mA	Plastic
UM2364A-2	200 ns	100 mA	12 mA	Plastic

* Not Applicable.