UMC

UM4501

512 × 9 Bit CMOS Parallel FIFO

Features

- First-in, first-out dual port memory
- 512 x 9 organization, 28-pin DIP
  Pin and functionally equivalent to MOSTEK MK4501
- Asynchronous and simultaneous read/write
- Empty and full warning flags
- Auto retransmit capability
- Multiple device expansion modes
- TTL-compatible interface
- Very low CMOS power consumption:
  Typical power consumption: 50 mW
  Average operating current: 10 mA
  Maximum standby current: 100 μA
- High performance architecture:
  High throughput dual port RAM architecture eliminates 1-2μsec fall-through delays of shift register type FIFOs
  10-28 MHz Operation: 35 – 100 ns access times
- 2μ CMOS double metal technology
  Electrostatic discharge tolerance to 2000V. Latch-up protection to 100 mA

General Description

The UM4501 is a dual port FIFO memory which implements first-in, first-out sequential storage of 512 nine-bit data words. The device supports asynchronous read and write operations. Full and empty flags are provided to prevent data overflow and underflow. Expansion control signals allow the FIFO to be easily cascaded, allowing multiple word widths and depths (i.e. 1024 x 9, 512 x 18, etc.).

The dual port RAM array is addressed internally using ring counter pointers. The Write pointer addresses the location where data is to be written next, and the Read pointer addresses the location to be read next.

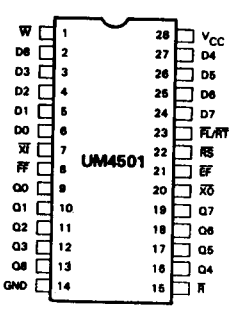
This high performance architecture reduces costly fall-through delays associated with shift register FIFOs. The worst-case fallthrough delay associated with this dual port RAM FIFO is the time required to update the pointers (35 – 100 ns), not the time required for data to propagate through the full depth of a shift register array (1-2μsec).

FIFO Architecture

The dual port memory within the FIFO allows independent and asynchronous operation of both inputs and outputs. The dual port RAM array is addressed internally using two ring counter pointers. The write pointer addresses the location where data is to be written next, and the read pointer addresses the location to be read next. Simultaneous read and write are supported. Comparators sense empty and full conditions, and control logic prevents memory overflow and underflow.

This high performance architecture eliminates costly fallthrough delays associated with shift register FIFOs. A word written to an initially empty shift register array must shift through the entire word depth before it is available for reading. As word depth increases, the number of clock cycles consumed shifting makes worst-case fall-through delay a significant factor (1-2μsec). The worst-case fallthrough delay in ring counter FIFOs represents the time required to update the pointers (35 – 100 ns), not the time required for data to propagate through the full depth of the shift register array.

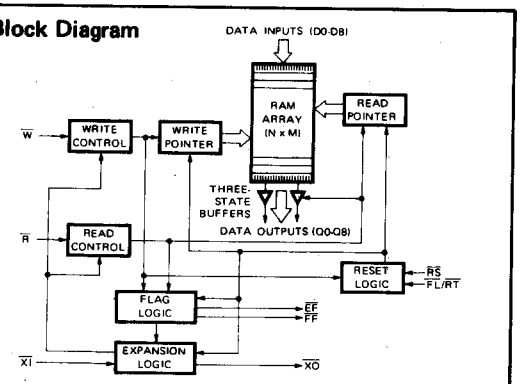
Pin Configuration



Pin Names

$\overline{W}$	= Write
$\overline{R}$	= Read
$\overline{RS}$	= Reset
$\overline{FL/RT}$	= First Load/Retransmit
D	= Data In
Q	= Data Out
$\overline{XI}$	= Expansion In
$\overline{XO}$	= Expansion Out
$\overline{FF}$	= Full Flag
$\overline{EF}$	= Empty Flag
V_{CC}	= Power Supply
GND	= Ground

Block Diagram



Absolute Maximum Ratings*

Terminal Voltage with Respect to GND
. . . . . −0.5 to + 7.0V
Operating Temperature . . . . . 0 − 70°C
Storage Temperature . . . . . −55 to + 125°C
Power Dissipation 1.0W
DC Output Current . . . . . 50 mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Characteristics

(V_{CC} = 5V ± 10%, T_A = 0 − 70°C)

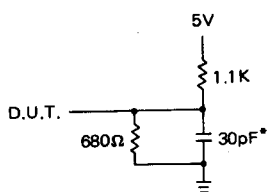
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
I_{IL}	Input Leakage Current (Any Input)	−1	–	1	μA	1
I_{OL}	Output Leakage Current	−10	–	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = −2mA	2.4	–	–	V	–
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	–	–	0.4	V	–
I_{CC1}	Average V_{CC} Power Supply Current	–	–	40	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	–	7	mA	3
I_{CC3}	Power Down Current (All Inputs = V_{CC} − 0.2V)	–	–	500	μA	3

Notes:
1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $R \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.
V_{CC}	Supply Voltage	4.5V	5.0V	5.5V
GND	Ground	0V	0V	0V
V_{IH}	High Voltage, All Inputs	2.0V	–	–
V_{IL}	Low Voltage, All Inputs	–	–	0.8V*

*1.5V undershoots are allowed for 10 ns, once per cycle.



*Includes jig and scope capacitances.

Figure 1.

FIFO Applications

Acting as temporary storage buffers, FIFOs allow data-rate matching between asynchronously timed data buses. Thus, data from an input device can load a FIFO at a different rate than the output device takes data from the FIFO.

FIFOs provide circuit savings and reduce system overhead by not requiring addresses for memory access. Because FIFOs do not utilize address and chip select inputs, they have been called "zero address RAMs".

FIFOs applications include data transfer rate matching between microprocessors and peripherals such as printers, disk drives, and streaming tape units. FIFOs are well suited in local-area network and communication protocol controller applications. They are also used to send and receive data to and from both D/A and A/D converters in digital signal processing applications. FIFOs are also used to decouple input data bursts from memories in high speed graphics processors, eliminating synchronization circuits.

AC Electrical Characteristics

(V_{CC} = 5V ± 10%, T_A = 0 – 70°C, Timings referenced as in AC Test Conditions)

Symbol	Parameters	UM4501/35		UM4501/50		UM4501/65		UM4501/80		UM4501/120		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cyle Time	45	–	65	–	80	–	100	–	140	–	ns	–
t_A	Access Time	–	35	–	50	–	65	–	80	–	120	ns	–
t_{RR}	Read Recovery Time	10	–	15	–	15	–	20	–	20	–	ns	–
t_{RPW}	Read Pulse Width	35	–	50	–	65	–	80	–	120	–	ns	1
t_{RLZ}	Read Pulse Low to Data Bus at Low Z	5	–	10	–	10	–	10	–	10	–	ns	2
t_{WLZ}	Write Pulse High to Data Bus at Low Z	10	–	15	–	15	–	20	–	20	–	ns	2
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	ns	–
t_{RHZ}	Read Pulse High to Data Bus at High Z	–	20	–	30	–	30	–	30	–	35	ns	2
t_{WC}	Write Cycle Time	45	–	65	–	80	–	100	–	140	–	ns	–
t_{WPW}	Write Pulse Width	35	–	50	–	65	–	80	–	120	–	ns	1
t_{WR}	Write Recovery Time	10	–	15	–	15	–	20	–	20	–	ns	–
t_{DS}	Data Setup Time	18	–	30	–	30	–	40	–	40	–	ns	–
t_{DH}	Data Hold Time	2	–	5	–	10	–	10	–	10	–	ns	–
t_{RSC}	Reset Cycle Time	45	–	65	–	80	–	100	–	140	–	ns	–
t_{RS}	Reset Pulse Width	35	–	50	–	65	–	80	–	120	–	ns	1
t_{RSR}	Reset Recovery Time	10	–	15	–	15	–	20	–	20	–	ns	–
t_{RTC}	Retransmit Cycle Time	45	–	65	–	80	–	100	–	140	–	ns	–
t_{RT}	Retransmit Pulse Width	35	–	50	–	65	–	80	–	120	–	ns	1
t_{RTR}	Retransmit Recovery Time	10	–	15	–	15	–	20	–	20	–	ns	–
t_{EFL}	Reset to Empty Flag Low	–	45	–	65	–	80	–	100	–	140	ns	–
t_{REF}	Read Low to Empty Flag Low	–	30	–	45	–	60	–	70	–	110	ns	–
t_{RFF}	Read High to Full Flag High	–	30	–	45	–	60	–	70	–	110	ns	–
T_{WEF}	Write High to Empty Flag High	–	30	–	45	–	60	–	70	–	110	ns	–
t_{WFF}	Write Low to Full Flag Low	–	30	–	45	–	60	–	70	–	110	ns	–

Notes:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

Capacitance

Symbol	Item	Conditions	Maximum	Notes
C_{IN}	Input Capacitance	V_{IN} = 0V	7 pF	3
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12 pF	2,3

Notes:
1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.

SIGNAL DESCRIPTIONS

Data Inputs

Data IN (D0 – D8)

These data inputs accept nine-bit data words for sequential storage in the FIFO during the Write cycle.

Control Signals and Flags

Reset ($\overline{RS}$)

This active-low control line input resets both the internal Read and Write pointers to their initial state (the first word location). An $\overline{RS}$ signal is required after power-up, before a Write operation can occur. Both the READ ENABLE ($\overline{R}$) and the WRITE ENABLE (W) must be in the inactive high state during RESET.

Read Enable ($\overline{R}$)

The falling edge of the READ ENABLE ($\overline{R}$) signal initiates a Read cycle, as long as the EMPTY FLAG ($\overline{EF}$) is not set. Data words are accessed on a first-in, first-out basis. Current read addresses are generated internally by ring counter logic, Read cycle timing is listed in "AC Electrical Characteristics", and is shown in Figure 3.

Read operations are independent of Write operations. After the read cycle, READ ENABLE ($\overline{R}$) goes inactive-high, causing the Data Outputs (D0 – D8) to go into high impedence (high-Z) state until the next Read operation.

When all of the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) goes active-low, and subsequent Read operations are inhibited. The flag is cleared upon completion of a valid write operation (after Twef).

Write Enable ($\overline{W}$)

The falling edge of the active-low WRITE ENABLE ($\overline{W}$) signal initiates a Write cycle, as long as the FULL FLAG ($\overline{FF}$) is not set. Data words are stored in the RAM array sequentially. Current write addresses are generated internally by ring counter logic. Write operations are independent of Read operations.

To be valid, data being written to the FIFO must meet setup and hold time requirements with respect to the rising edge of the WRITE ENABLE ($\overline{W}$) signal. Write Cycle timing is listed in "AC Electrical Characteristics", and shown in Figure 4.

When the word capacity of the FIFO has been reached, the FULL FLAG ($\overline{FF}$) goes active-low to prevent data overflow. The FULL FLAG ($\overline{FF}$) is cleared upon the completion of a valid Read operation (after Trff).

Expansion In ($\overline{XI}$)

This input pin serves two purposes. When grounded, it indicates that the FIFO is being operated in Single Device Mode (see Operating Modes).

In Multiple Device Mode, it is connected to the EXPANSION OUT ($\overline{XO}$) line of the previous device when the FIFO is configured in Depth Expansion or Daisy Chain Mode.

Expansion Out ($\overline{XO}$)

The EXPANSION OUT signal provides a pulse to the next device in the Daisy Chain when the last world location has been reached in order to access the next FIFO.

Firstload/Retransmit ($\overline{FL}/\overline{RT}$)

The output pin serves two purposes. In Single Device Mode, the pin serves as the RETRANSMIT ENABLE ($\overline{RT}$) signal. In Multiple Device Mode (see Operating Modes), the pin is the FIRST LOAD ($\overline{FL}$) pin.

When this line is pulsed active-low in Single Device Mode, a Retransmit operation is enabled. Retransmit resets the internal Read pointer to the first location, but does not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be inactive (high) during Retransmit. RETRANSMIT ENABLE ($\overline{RT}$) is generally used when less than 512 writes are performed between resets. This feature can not be used in Multiple Device Mode.

When used in Multiple Device Mode, the FIRST LOAD ($\overline{FL}$) pin on the first FIFO in the Daisy Chain to be loaded with data is grounded (see Operating Modes). The remaining $\overline{FL}$ pins in the Daisy Chain are tied to V_{CC}.

Full Flag ($\overline{FF}$)

When the word capacity of the FIFO has been reached, the FULL FLAG ($\overline{FF}$) goes active-low when the Write pointer is one word location from the Read pointer, to prevent data overflow. The signal inhibits Write operations and is cleared when a valid Read operation completes (after Trff). Both the FULL FLAG ($\overline{FF}$) and the EMPTY FLAG ($\overline{EF}$) may be used as clock-enables to control asynchronous timing.

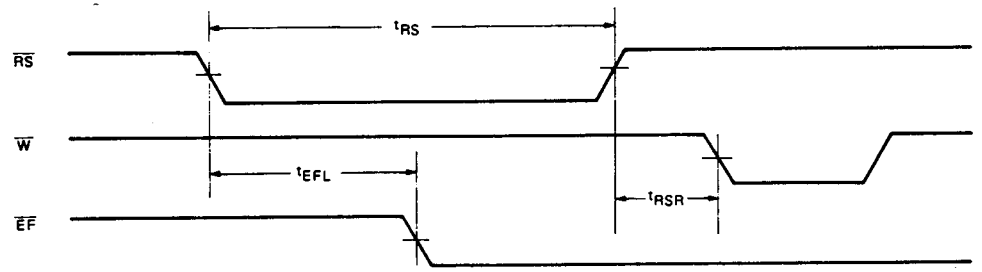
Empty Flag ($\overline{EF}$)

When all of the data has been read from the device, the EMPTY FLAG ($\overline{EF}$) goes active-low (when the Read pointer is one word location from the Write pointer). The EMPTY FLAG ($\overline{EF}$) inhibits Read operations by causing the Data Outputs to go into high-Z state. It is cleared when a valid Write operation completes (after Twef).

Data Outputs

Data Outputs (Q0 – Q8)

These nine lines are the data-word output. These lines are in high-Z state whenever READ (R) is inactive.



Notes:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET (RS)

Figure 2. Reset

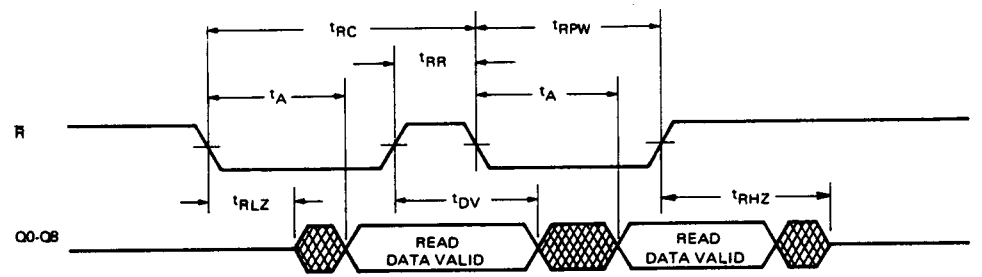


Figure 3. Asynchronous Read Operation

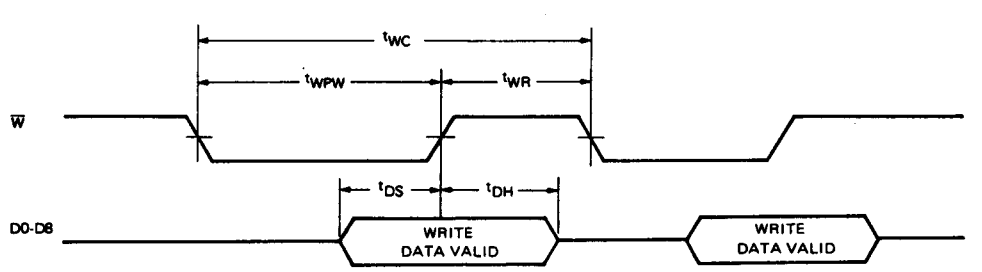


Figure 4. Asynchronous Write Operation

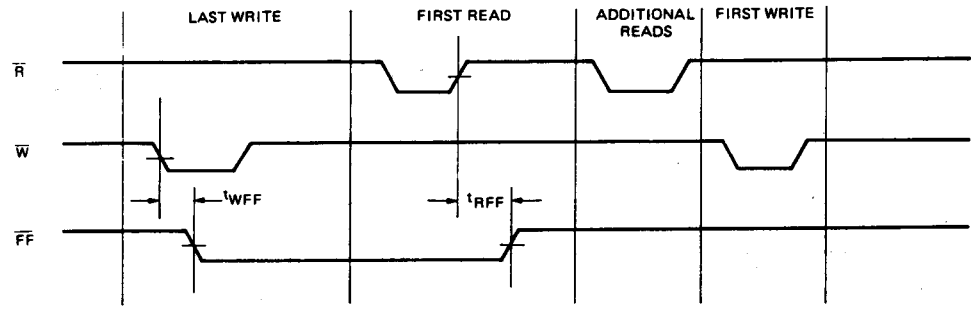


Figure 5. Full Flag from Last Write to First Read

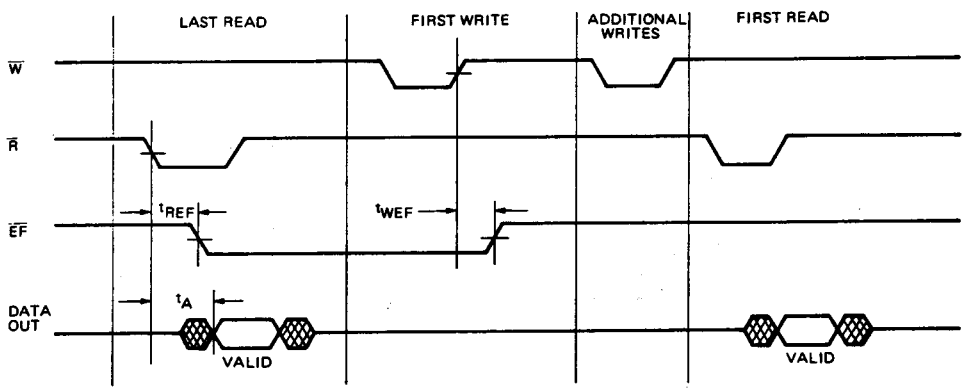
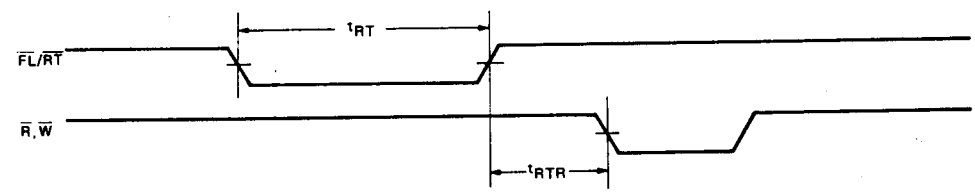


Figure 6. Empty Flag from Last Read to First Write



Notes:
1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. EF and FF may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7. Retransmit

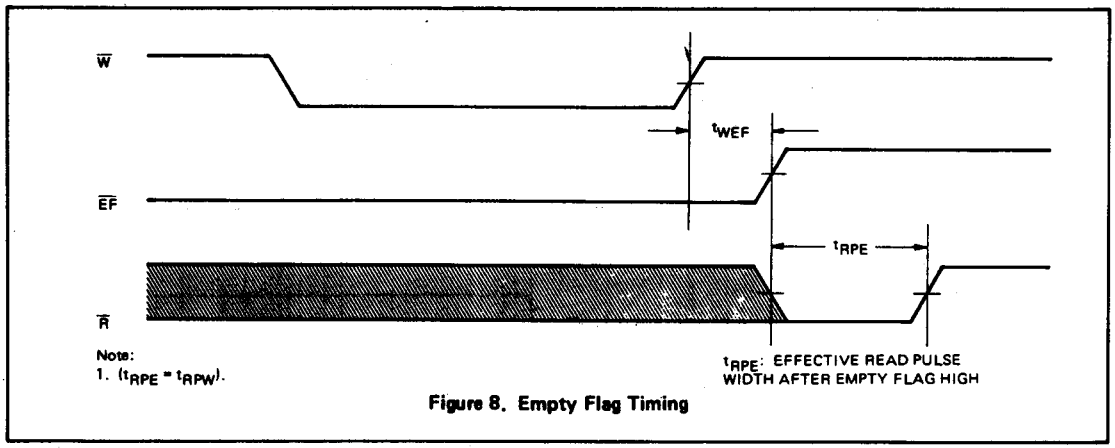


Figure 8. Empty Flag Timing

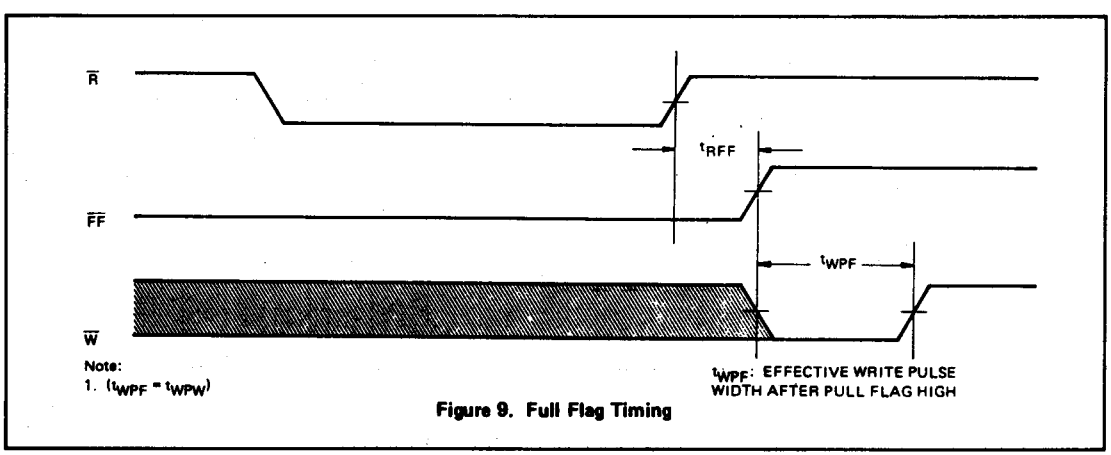


Figure 9. Full Flag Timing

Operating Modes

Single Device Mode

When one UM4501 is used standalone in Single Device Mode, the Expansion In ($\overline{XI}$) control input pin must be grounded. See Figure 10.

Width Expansion Mode

Word width may be expanded by connecting the corresponding control input signals of multiple devices together. The EMPTY FLAG and FULL FLAG ($\overline{EE}$ and $\overline{FF}$) can be detected by any particular device. Figure 11 shows an 18-bit wide configuration using two devices. They may be configured to any word width in this manner.

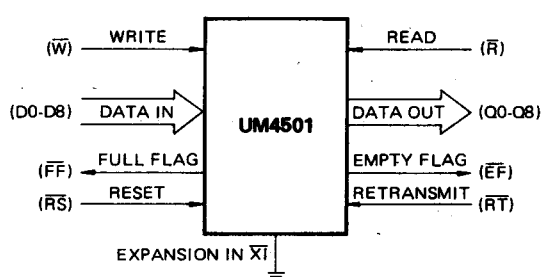


Figure 10. Single Device Mode

Depth Expansion (Daisy Chain) Mode

Word depths may be expanded in multiples of 512 words by Daisy Chaining the devices together as follows:

1. The FIRST LOAD ($\overline{FL}$) control signal of the first device must be grounded. This FIFO represents word 1-512.

2. All other devices in the Daisy Chain must have the FIRST LOAD ($\overline{FL}$) control signal tied to V_{CC}, in the inactive-high state.

3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be connected to the EXPANSION IN ($\overline{XI}$) pin of the next device as shown in Figure 13.

4. External logic is required to generate a common FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$) signal by ORing all of the $\overline{FF}$s together and ORing all of the $\overline{EF}$s together.

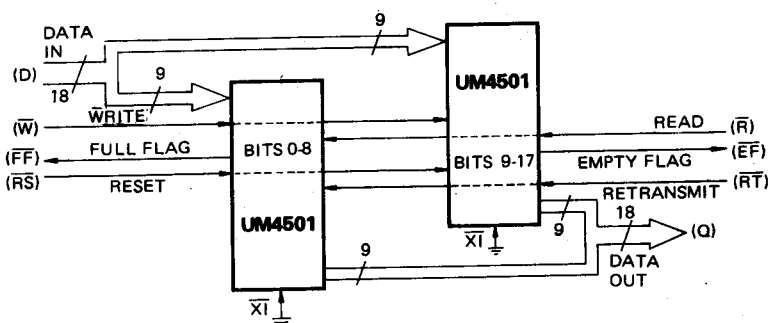
5. The RETRANSMIT ($\overline{RT}$) function is not available in Daisy Chain Mode.

Bidirectional Mode

Data buffering between two systems can be achieved by pairing two FIFO arrays as shown in Figure 12. This allows each system to READ and WRITE shared data. The FULL FLAG ($\overline{FF}$) must be monitored on the FIFO where WRITE ENABLE ($\overline{W}$) is used, and the EMPTY FLAG ($\overline{EF}$) must be monitored on the FIFO where READ ENABLE ($\overline{R}$) is used. Both Width Expansion and Depth Expansion Modes may be used in combination with Bidirectional Mode.

Compound Expansion Mode

Both Width Expansion Mode and Depth Expansion (Daisy Chain) Mode can be used together to configure a large FIFO array (See Figure 11 and 13).



Notes:
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$, on device used in the Width Expansion Mode.
Do not connect output control signals together.

Figure 11. Width Expansion Mode

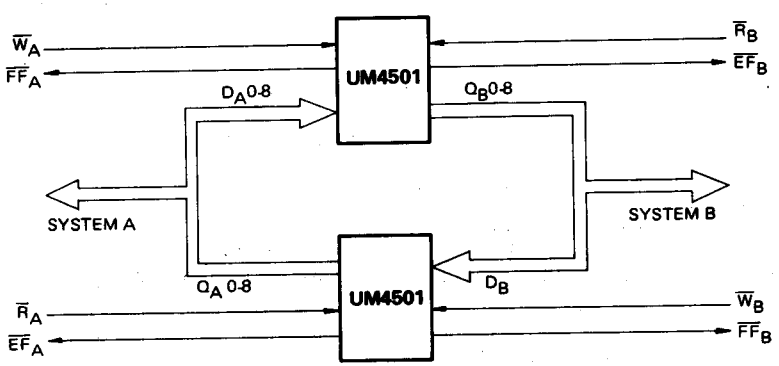


Figure 12. Bidirectional FIFO Mode

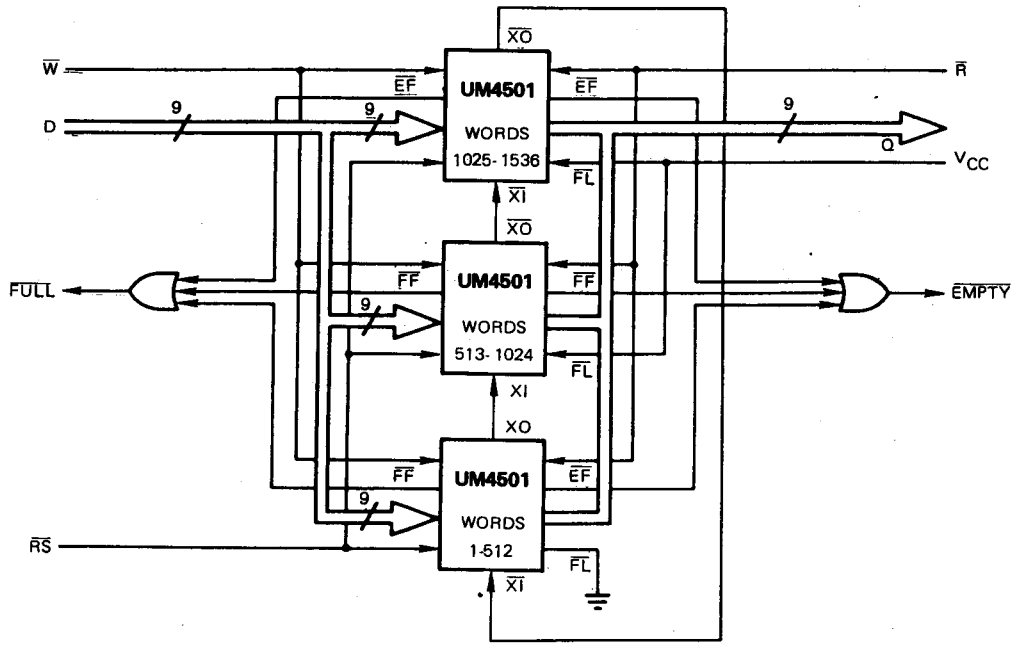


Figure 13. Block Diagram of a 1536 x 9 FIFO Memory (Depth Expansion)

Truth Tables

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Table 1. Reset and Retransmit

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset	0	X	0	Location Zero	Location Zero	0	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X

Note:
1. Pointer will increment if flag is high.

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Table 2. Reset and Firstload

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

Notes:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 13.
$\overline{RS}$ = Reset Input. $\overline{FL}/\overline{RT}$ = First Load/Retransmit. $\overline{EF}$ = Empty Flag Output. $\overline{FF}$ = Full Flag Output. $\overline{XI}$ = Expansion Input.

Ordering Information

Part Number	Access Time	Package*
UM4501-120P	120ns	Plastic
UM4501- 80P	80ns	Plastic
UM4501- 50P	50ns	Plastic
UM4501- 35P	35ns	Plastic

*CERDIP, PLCC packaging are available on customer request.